

## 3-Channel Breathing LED Driver with IIC Interface

### FEATURES

- 3-channel constant current LED drivers
  - 4-level  $I_{MAX}$  selections: 3/6/12/25.5mA
  - 256 current levels setting for each LED
  - Supports 256\*256\*256 color-mixing
- 256-level PWM dimming, 12-bit PWM resolution
- Automatic breathing light with flexible pattern configuration and running mode
  - three independent pattern controllers
  - pulses repeating, multiple colors alternative
  - multiple patterns running successively or cyclically
- 400kHz fast I<sup>2</sup>C interface, 1.8V ~ 3.3V
- Single power supply, 2.4V~5.5V
- Low power consumption
  - Less than 1 $\mu$ A in shut down mode
  - Less than 10 $\mu$ A in standby mode
- DFN 1.5mmx1.5mmx0.45mm-8L package

### GENERAL DESCRIPTION

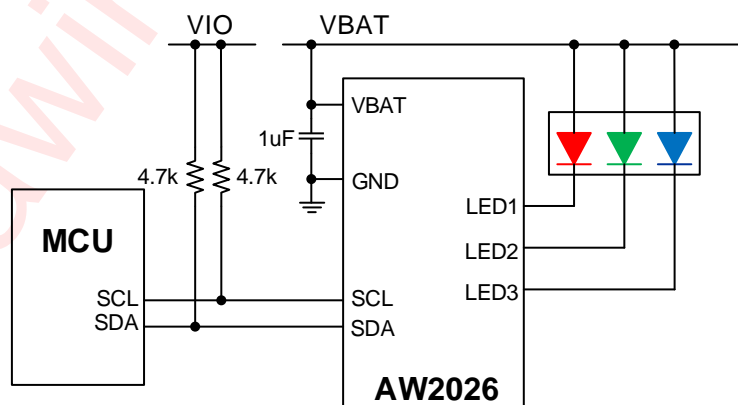
AW2026 is a three channels constant current LED driver. The max output current is 4-level selectable among 3mA, 6mA, 12mA and 25.5mA. Each LED is 256 current levels configurable so as to achieve 256\*256\*256 color mixing. The 256-level dimming and 12 bits PWM resolution create fine and smooth dimming effect even in low brightness.

In shut down mode, AW2026 turns off all internal circuit and the consumption is less than 1 $\mu$ A. In standby mode, I<sup>2</sup>C interface works and the consumption is less than 10 $\mu$ A.

The device requires only 2.4V~5.5V single power supply. An I<sup>2</sup>C compatible interface in 400kHz fast mode is provided, the device address is 64h.

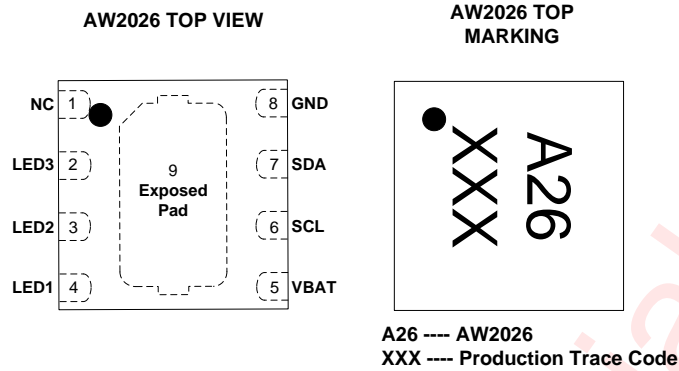
AW2026 is available in a DFN 1.5mmx1.5mmx0.45mm-8L package.

### TYPICAL APPLICATION CIRCUIT



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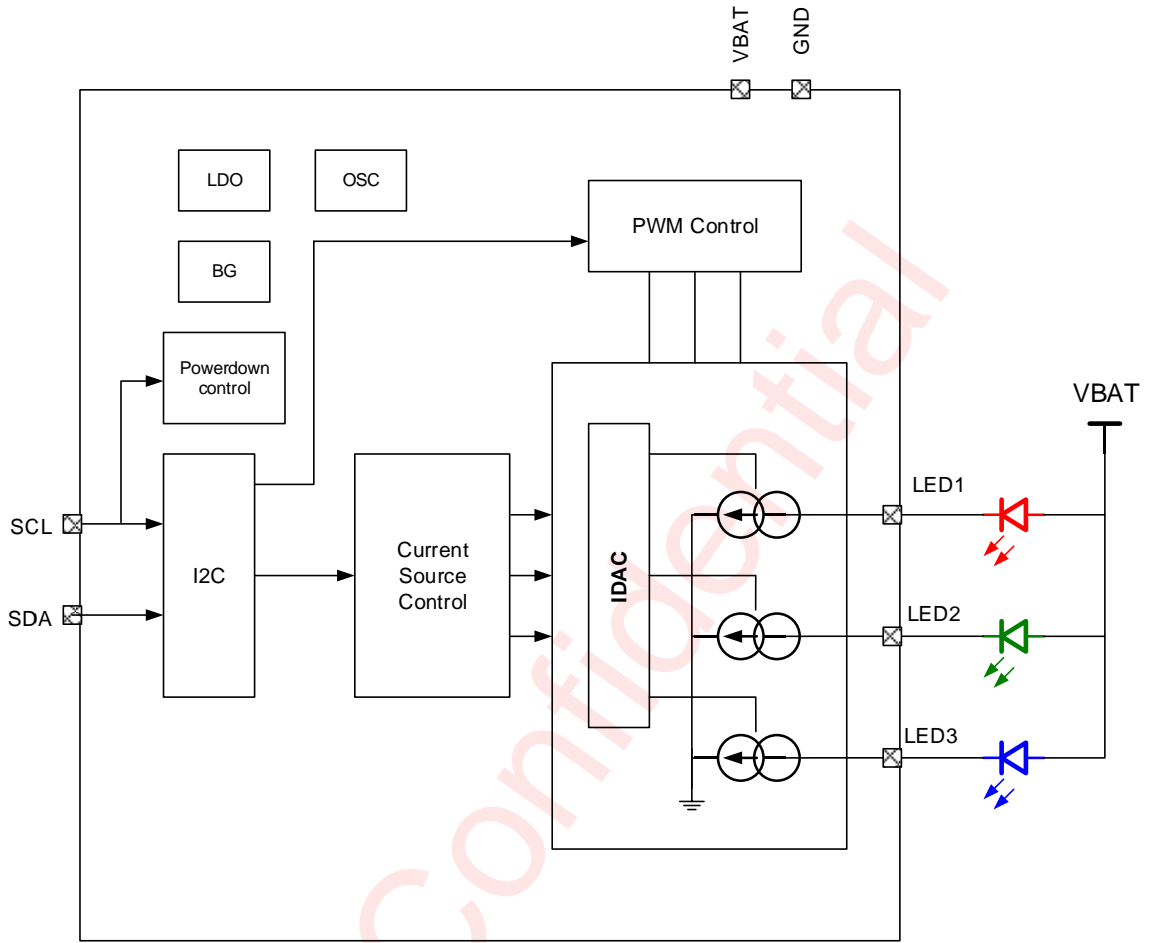
## PIN CONFIGURATION AND TOP MARK



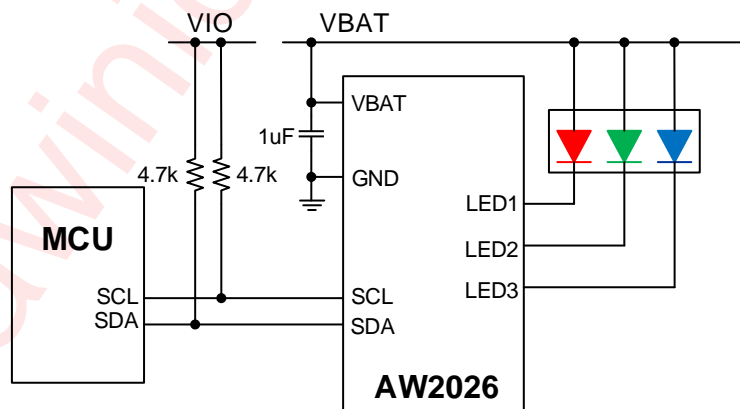
## PIN DEFINITION

No.	NAME	DESCRIPTION
1	NC	Not connected
2	LED3	LED3 Cathode Driver, anode connected to VBAT
3	LED2	LED2 Cathode Driver, anode connected to VBAT
4	LED1	LED1 Cathode Driver, anode connected to VBAT
5	VBAT	Power Supply (2.4V-5.5V)
6	SCL	Serial Clock Input for I <sup>2</sup> C Interface
7	SDA	Serial Data I/O for I <sup>2</sup> C Interface
8	GND	GND
9	Exposed Pad	Exposed pad, should be connected to GND.

## FUNCTIONAL BLOCK DIAGRAM

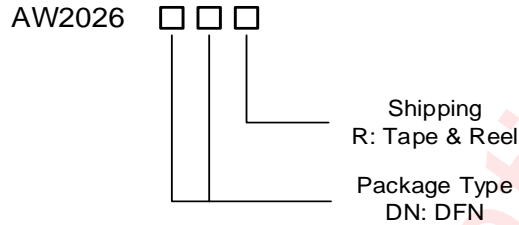


## TYPICAL APPLICATION CIRCUITS



## ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW2026DNR	-40°C~85°C	DFN1.5mm×1.5mm ×0.45mm-8L	A26	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel



## ABSOLUTE MAXIMUM RATINGS (NOTE 1)

PARAMETERS		RANGE
Supply voltage range $V_{BAT}$		-0.3V to 6.0V
Input voltage range	SCL, SDA,	-0.3V to 6.0V
	LED1~LED3	-0.3V to 6.0V
Output voltage range	SDA	-0.3V to 6.0V
Junction-to-ambient thermal resistance $\theta_{JA}$		121.6°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum Junction temperature $T_{JMAX}$		150°C
Storage temperature $T_{STG}$		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD <sup>(NOTE 2)</sup>		
HBM (human body mode)		±2000V
CDM (charge device mode)		±1500V
MM (machine mode)		±300V
Latch-up		
Test Condition: JEDEC JESD78F-2022		±300mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

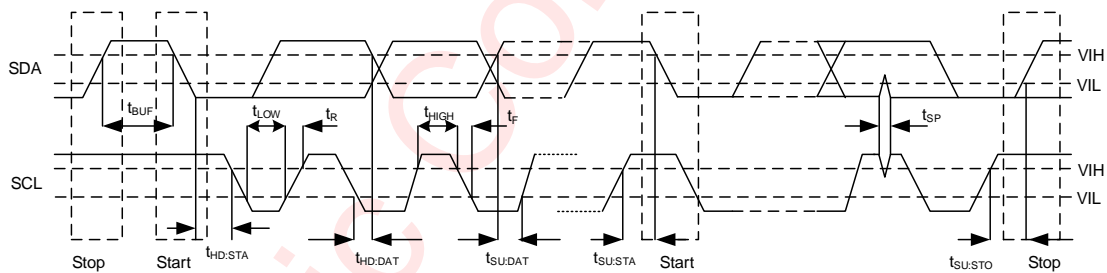
NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017(HBM). ESDA/JEDEC JS-002-2018(CDM).

**ELECTRICAL CHARACTERISTICS**V<sub>BAT</sub>=3.8V, T<sub>A</sub>=25°C for typical values (unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
<b>Power supply</b>						
V <sub>BAT</sub>	Input operation voltage		2.4		5.5	V
I <sub>SHUTDOWN</sub>	Current in Shutdown mode	SCL/ SDA =0V (over 130ms)		0.1	1	μA
I <sub>STANDBY</sub>	Current in Standby mode	SCL/SDA=1.8V		5	10	μA
I <sub>Q</sub>	Quiescent Current in Active mode	register CHIPEN=1 all LED off		80	100	μA
I <sub>ACTIVE</sub>	Current in Active mode	All channel set to 25.5mA		565		μA
		LED1 set to 25.5mA LED2, LED3 off		277		
		All channel set to 25.5mA T <sub>RISE</sub> =2.1s, T <sub>ON</sub> =0.04s T <sub>FALL</sub> =2.1s, T <sub>OFF</sub> =1s		181		
		LED1 set to 25.5mA LED2, LED3 off T <sub>RISE</sub> =2.1s, T <sub>ON</sub> =0.04s T <sub>FALL</sub> =2.1s, T <sub>OFF</sub> =1s		121		
<b>Digital Logical Interface</b>						
V <sub>IL</sub>	Logic input low level	SDA,SCL			0.4	V
V <sub>IH</sub>	Logic input high level	SDA,SCL	1.3			V
I <sub>IL</sub>	Low level input current	SDA,SCL		5		nA
I <sub>IH</sub>	High level input current	SDA,SCL		5		nA
V <sub>OL</sub>	Logic output low level	SDA, I <sub>OUT</sub> =3mA			0.4	V
I <sub>L</sub>	Output leakage current	SDA open drain			1	nA
<b>I<sup>2</sup>C Interface</b>						
F <sub>SCL</sub>	I <sup>2</sup> C-BUS clock frequency				400	kHz
T <sub>DEGLITCH</sub>	SCL deglitch time			200		ns
	SDA deglitch time			250		ns
<b>LED Driver</b>						
I <sub>ACC</sub>	Current accuracy	I <sub>LED</sub> =25.5mA	-5%		+5%	%
I <sub>MATCH</sub>	Matching accuracy	I <sub>LED</sub> =25.5mA	-5%		+5%	%
V <sub>DROP</sub>	Dropout voltage	I <sub>LED</sub> =25.5mA		60	100	mV
F <sub>PWM</sub>	PWM frequency	Register PWM_F=0	115	122	128	Hz
		Register PWM_F=1	230	244	256	Hz

I<sup>2</sup>C INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
F <sub>SCL</sub>	Interface Clock frequency			400	kHz
T <sub>DEGLITCH</sub>	Deglitch time	SCL	200		ns
		SDA	250		ns
T <sub>HD:STA</sub>	(Repeat-start) Start condition hold time	0.6			μs
T <sub>LOW</sub>	Low level width of SCL	1.3			μs
T <sub>HIGH</sub>	High level width of SCL	0.6			μs
T <sub>SU:STA</sub>	(Repeat-start) Start condition setup time	0.6			μs
T <sub>HD:DAT</sub>	Data hold time	0			μs
T <sub>SU:DAT</sub>	Data setup time	0.1			μs
T <sub>R</sub>	Rising time of SDA and SCL			0.3	μs
T <sub>F</sub>	Falling time of SDA and SCL			0.3	μs
T <sub>SU:STO</sub>	Stop condition setup time	0.6			μs
T <sub>BUF</sub>	Time between start and stop condition	1.3			μs



## FUNCTIONAL DESCRIPTION

### POWER\_ON RESET

AW2026 provides a power-on reset feature that is controlled by VBAT supply voltage. When the VBAT supply voltage rises from 0V to 2.4V, the internal LDO starts to work. The reset signal will be generated to perform a power-on reset operation, which will reset all control circuits and configuration registers until the internal power voltage become stable.

The status bit STATUS.PUIS (register: 0x02 bit4) will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of STATUS register. Usually the STATUS.PUIS bit can be used to check whether an unexpected power-on event has taken place.

### OPERATING MODE

In AW2026, pin SCL provides power down control. There are three work modes available: Shut-down, Standby and Active mode.

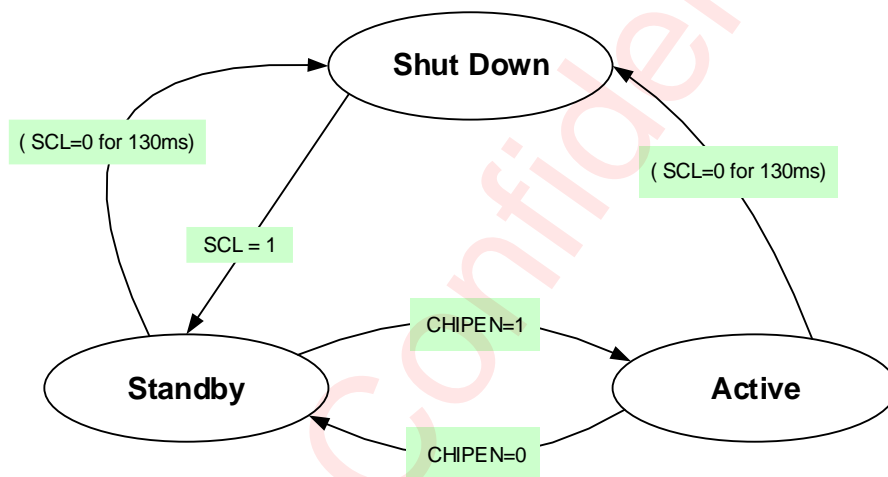


Figure 1 AW2026 operating modes transition

### SHUT-DOWN MODE

AW2026 enters into the shut-down mode when SCL level is pulled to low for over 130ms (prevents system against wrong resets caused by electromagnetically influences)

In shut-down mode, AW2026 will reset all internal circuits and configuration register, all blocks inside AW2026 are basically switched off except the power on reset circuit and the SCL level detect circuit, and the current consumption is very low ( $< 1\mu\text{A}$ ).

### STANDBY MODE

AW2026 enters into standby mode when SCL level is pulled high from shut-down mode or CHIPEN is 0 from active mode. In standby mode, only part of internal circuit can work, the OSC still keep closed so that there is not internal clock, the LDO operates in low power state. The current consumption is less than  $10\mu\text{A}$ .

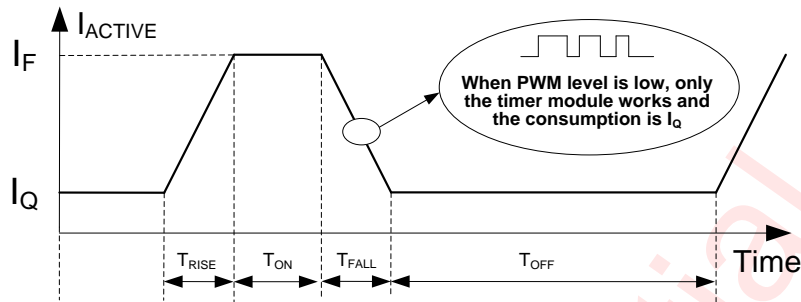
In stand-by mode, the I<sup>2</sup>C interface is accessible, but only registers RSTIDR and GCR can be operated.

### ACTIVE MODE

When bit CHIPEN of GCR register is set to 1 in standby mode, AW2026 enters into active mode.

In active mode, the internal OSC starts to work to provide clock signal. User can configure the device to produce the pre-defined pattern lighting effects in pattern mode or turn each LED on or off directly.

When PWM level is low in fade-in and fade-out, only the OSC module works and the consumption is about  $80\mu\text{A}(I_Q)$ . So, the average consumption of breathing is every low.



**Figure 2** AW2026 consumption in active mode

Refer the following detailed formula (LED1/LED2/LED3 on)

$$I_{\text{ACTIVE}} = (I_F - I_Q) * \frac{(T_{\text{RISE}} + T_{\text{FALL}}) * 25\% + T_{\text{ON}}}{T_{\text{RISE}} + T_{\text{ON}} + T_{\text{FALL}} + T_{\text{OFF}}} + I_Q$$

$I_{\text{MAX}}$	3mA	6.375mA	12.75mA	25.5mA
$I_F$	223 $\mu\text{A}$	272 $\mu\text{A}$	368 $\mu\text{A}$	565 $\mu\text{A}$
$I_Q$	80 $\mu\text{A}$	80 $\mu\text{A}$	80 $\mu\text{A}$	80 $\mu\text{A}$

## SOFTWARE RESET

Writing 0x55 to register RSTIDR (register: 0x00) via I<sup>2</sup>C interface will reset the AW2026 internal circuits and all configuration registers.

## I<sup>2</sup>C INTERFACE

AW2026 supports the I<sup>2</sup>C serial bus and data transmission protocol in fast mode at 400 kHz. AW2026 operates as a slave on the I<sup>2</sup>C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10k $\Omega$  and the typical value is 4.7k $\Omega$ . AW2026 can support different high level (1.8V~3.3V) of this I<sup>2</sup>C interface.

## DEVICE ADDRESS

The I<sup>2</sup>C device address (7-bit) of AW2026 is 0x64, followed by the R/W bit (Read=1/Write=0).

## DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

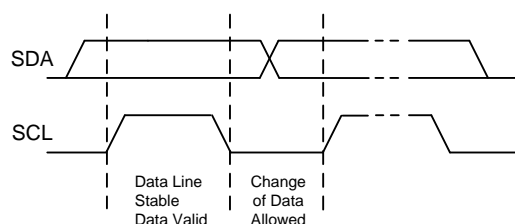
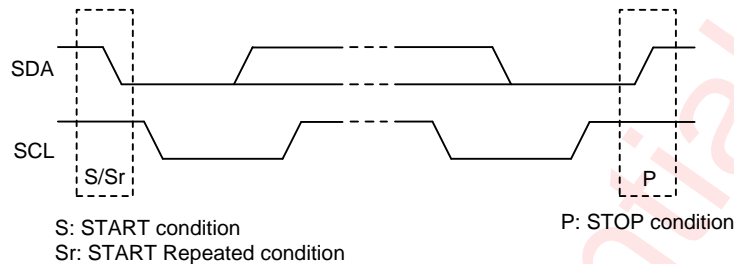


Figure 3 Data Validation Diagram

**I<sup>2</sup>C START/STOP**

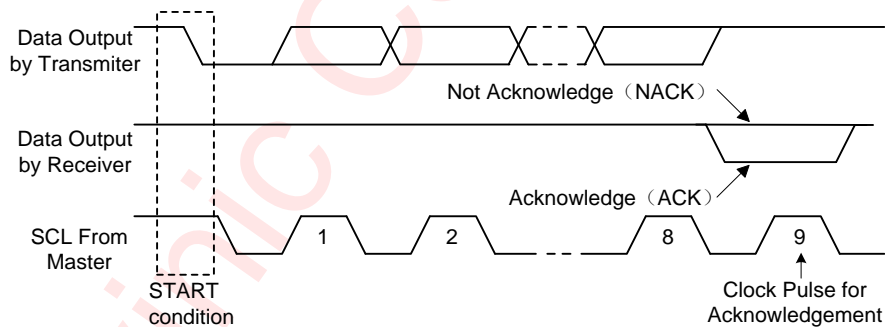
I<sup>2</sup>C start: SDA changes from high level to low level when SCL is high level.

I<sup>2</sup>C stop: SDA changes from low level to high level when SCL is high level.

Figure 4 I<sup>2</sup>C Start/Stop Condition Timing**ACK (ACKNOWLEDGEMENT)**

ACK means the successful transfer of I<sup>2</sup>C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I<sup>2</sup>C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I<sup>2</sup>C stop.

Figure 5 I<sup>2</sup>C ACK Timing**WRITE CYCLE**

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit ( $r/w = 0$ ).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit)
- Slave sends acknowledge signal
- Master sends data byte to be written to the addressed register
- Slave sends acknowledge signal
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6,7)
- Master generates STOP condition to indicate write cycle end



**Figure 6** I<sup>2</sup>C Write Byte Cycle

## READ CYCLE

In a read cycle, the following steps should be followed:

- Master device generates START condition
- Master device sends slave address (7-bit) and the data direction bit ( $r/w = 0$ ).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit)
- Slave sends acknowledge signal
- Master generates STOP condition followed with START condition or REPEAT START condition
- Master device sends slave address (7-bit) and the data direction bit ( $r/w = 1$ ).
- Slave device sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
- If the master device generates STOP condition, the read cycle is ended.

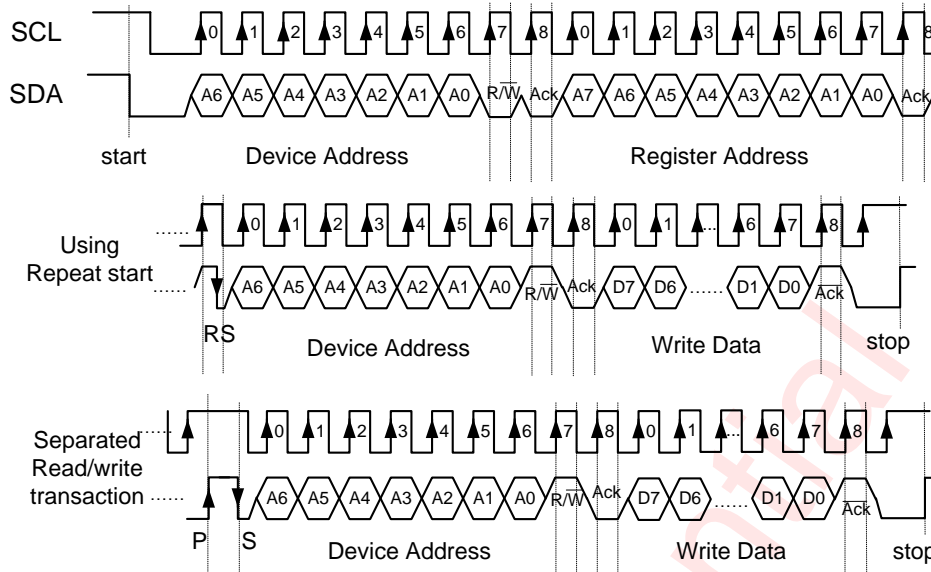


Figure 7 I<sup>2</sup>C Read Byte Cycle

## LED DRIVER

AW2026 has three LED drivers to drive one RGB LED or three single-color LEDs. Each LED is driven by common-anode mode constant current source with duty cycle controlled by PWM. Both current and PWM can be configured via I<sup>2</sup>C interface.

## LED CURRENT

Globally, the maximum output current for three LEDs is 4-level selectable among 3mA, 6mA, 12mA and 25.5mA via register IMAX (register: 0x03). In general, IMAX is used to set the max brightness of LED output.

For each LED, there is 256 current levels configurable via 8-bit register groups ILED<sub>x\_y</sub> (x=1~3, y=1~4). So in RGB application it is possible to combine into 256x256x256 color-mixing schemes totally to achieve so-called true-color effect.

Generally, the current level register is used to form specified LED color for RGB application. AW2026 has 4 groups pre-defined current registers capable of forming 4 dedicated colors in true-color pattern scheme, in which up to 4 pre-defined colors can be configured to represent 4 kinds of message, more than one color can flash one by one successively in the same pattern when it's necessary to transmit more than one messages.

## PWM DIMMING CONTROL

In AW2026, each LED current source is gated by a 256-level, 12bit resolution PWM signal to create fine dimming effect.

Each LED has an 8-bit PWM register PWM<sub>x</sub> (register: 0x1C/0x1D/0x1E) to control the duty cycle of constant current source. The ramp up and down are automatically implemented by PWM duty continuously adjusted to form a smooth LED current transition between ON and OFF state. The ramp slope, for rise and fall, are separately set via configuring the bit4~bit7 in pattern registers PAT<sub>x\_T1</sub> and PAT<sub>x\_T2</sub>.

The ramping can be configured as linear and logarithmic curve by setting bit0~1 (PWMLOG) in register LEDCTR (register 0x08).

## LED CONTROL

Each LED of AW2026 can be independently configured to work or not via control bit LEDxEN.

- LEDxEN = 0, LEDx channel is disabled and no current output.
- LEDxEN = 1, LEDx channel is enabled to output lighting effect in different work mode.

By register configuration, AW2026 provides two types of LED control modes:

- Pattern control mode.

AW2026 contains three independent pattern controller and three groups of pattern parameter register to generate user-defined breathing lighting effect. In RGB application, one pattern controller control 3 LED simultaneously to produce true-color breathing lighting, and three groups of pattern parameter can be executed successively or cyclically. For LED-independent application, three pattern controller are allocated to three different LEDs respectively, each operates with individual pattern parameter, user can start or stop each pattern independently

- Manual control mode.

User directly set the brightness level of each LED by configuring relative current level register and PWM level register via I<sup>2</sup>C interface. Usually it's recommended to modify the PWM level to set on or off. For each variation of PWM level register, the smoothly ramping effect is supported by setting FADE\_IN bit and/or FADE\_OUT bit in register LCFGx (x=1~3).

## PATTERN CONTROL MODE

### BREATHING LIGHTING CONTROL

When register bit LCFGx.LEDMD (register: 0x04/0x05/0x06 bit0) is set to 1, the corresponding LEDx operates in pattern mode.

User should configure the related pattern parameter registers according to actual timing requirements via I2C interface before starting pattern. The repeating times of pattern is configurable also, which may be 1~ 2048 or infinite according to setting of register PATx\_T5 (x=1~3).

### Single Pulse mode

Basically, one pattern contains only one blinking, it's called as single pulse mode. In single pulse mode, the pattern parameters include delay time, rise time, on time, fall time, off time and repeat times can be set by corresponding configuration registers (PATx\_T1~T5). The meanings of basic single-pulse pattern parameters are shown in Figure and table below.

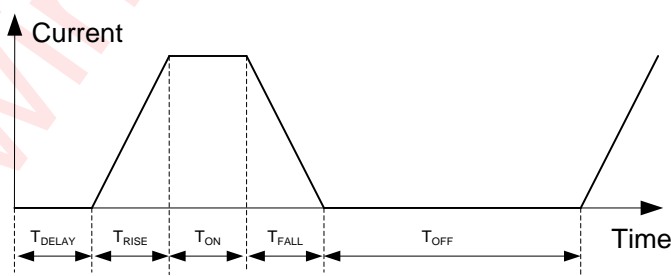


Figure 8 Basic single-pulse pattern parameter definition

Symbol	Parameters	Min	Typ.	Max	Unit
T <sub>DELAY</sub>	Delay time until pattern start	0		8.3	s
T <sub>RISE</sub>	Rise time for dimming up	0		8.3	s
T <sub>ON</sub>	On time	0.04		8.3	s
T <sub>FALL</sub>	Fall time for dimming down	0		8.3	s
T <sub>OFF</sub>	Off time	0.04		8.3	s

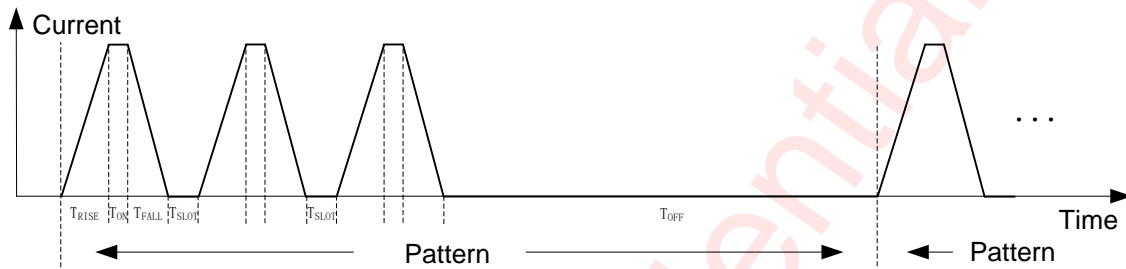
**Multi-pulse mode**

A serial fast pulse blinking can be used to transmit message different from that carried by single pulse. In multi-pulse mode, up to 4 pulses are allowed during one color blinking. Besides the basic timing parameter defined in single-pulse mode, there are 2 additional parameters need to be set:

The number of multi-pulse is defined by setting bit4~5 (MPULSE) in register PATx\_T4 (register: 0x33/0x38/0x3D), the actual blinking times is MPULSE+1.

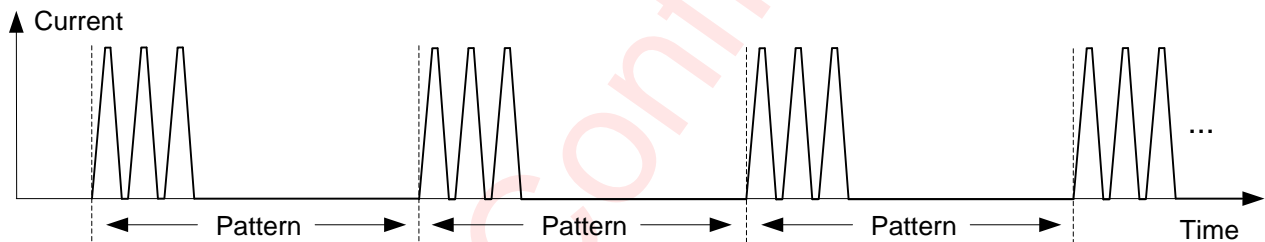
The interval time between two adjacent pulses is defined by T<sub>SLOT</sub>, bit4~6 in PATx\_T3 (register: 0x32/0x37/0x3C).

Symbol	Parameter	Min	Typ.	Max	Unit
T <sub>SLOT</sub>	Pause time between multiple pulses	0		1.024	s



**Figure 9** Multi-pulse pattern parameter definition

An example of multi-pulse pattern is shown below:



**Figure 10** Multi-pulse pattern example

**Multi-color mode**

Blinking with multiple different colors is allowed in one pattern period in RGB LED application, if different color is expected to carry different message.

In AW2026, the LED color is defined by LED current configure register ILEDx\_y (x=1~3, y=1~4), there are 4 RGB current combination to generate 4 pre-defined colors for display. More than one of the 4 pre-defined colors can be chosen by setting CE1~CE4, bit0~bit3 in PATx\_T4 (register:0x33/0x38/0x3D), when CEx is set to 1, the color#x is allowed to be displayed in current pattern.

If the color setting on CE1~CE4 is modified during current pattern is running, the updating of new color setting will not occur until present pattern period is over.

If both multi-pulse and multi-color is enabled simultaneously, every selected color will blink specified times before switching to another color, and the display order of color is always from color #1 to color #4.

An example of 4-color /single-pulse pattern is shown below, in which the CE1~CE4 are changed twice during pattern is running.

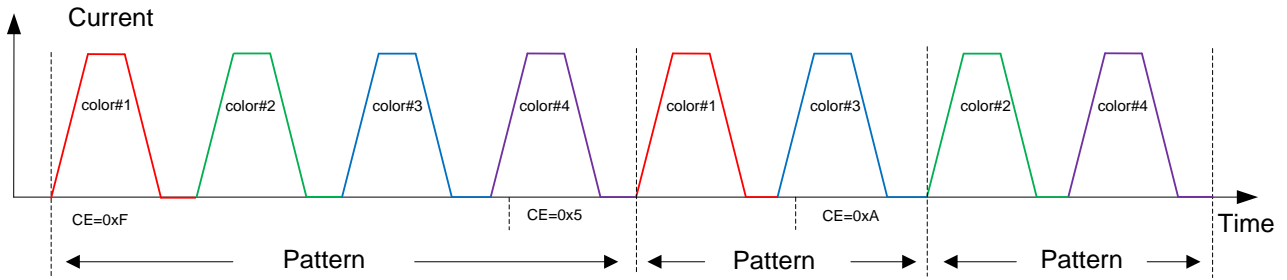


Figure 11 Example of multi-color mode and color scheme modification

**TRUE –COLOR BREATHING LIGHTING**

In true-color breathing lighting application, the LEDMD, bit0 in LCFGx (register: 0x04/0x05/0x06), and the SYNC, bit3 in LEDCTR (register: 0x08 bit3) should be set to 1, three LED output share the same pattern controller to generate PWM dimming simultaneously. Multi-pulse, multi-color and multi-pattern modes are supported fully in this mode.

The RGB color is defined by LED current setting register ILEDx\_y (x=1~3, y=1~4), there are 4 RGB current combination to generate 4 pre-defined color for display.

In true-color mode (SYNC=1), 3 groups of pattern timer parameters could be applied to defined 3 different breathing lighting effects, which can be executed successively or keep looping forever, without external processor involved to control every pattern switching. For each pattern, if PATx\_T4. PAT\_SW (register: 0x33/0x38/0x3D) is set to 1, the next pattern parameter will be loaded and started automatically after current pattern has finished.

The following table gives the current, pattern and the start/stop control source for each LED channel in true-color pattern mode.

Channel	Current Configuration Register	Pattern used	Pattern Start	Pattern Stop
LED1	ILED1_y	pattern #1, pattern #2, pattern #3	Write 1 to register PATRUN bit0	Write 1 to register PATRUN bit4
LED2	ILED2_y			
LED3	ILED3_y			

Note: Y=1~4, denotes 4 pre-defined color code (color #1, color #2, color #3 and color #4).

An example of single pulse and color pattern repeating in true-color pattern mode is depicted in the figure below.

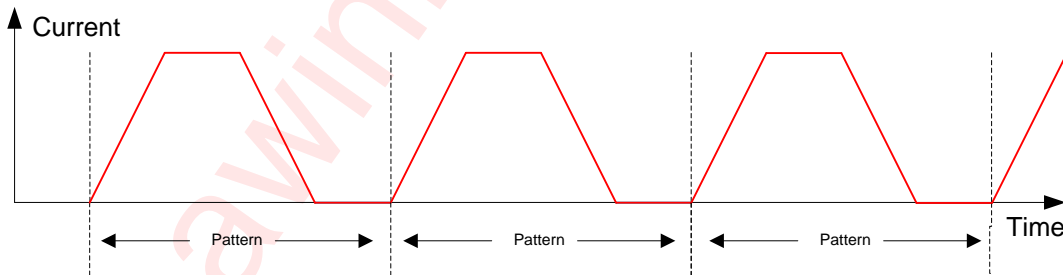
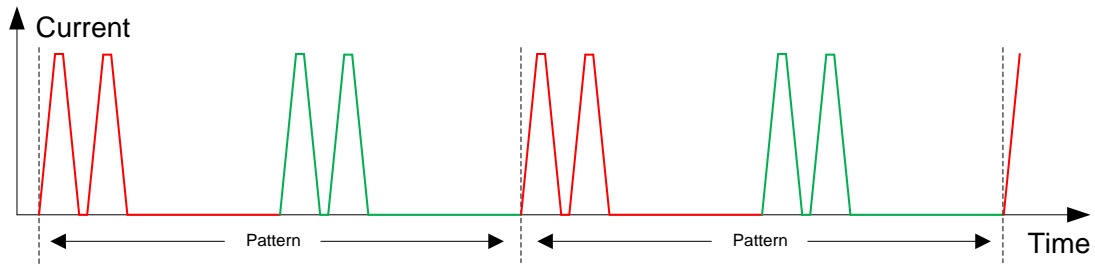


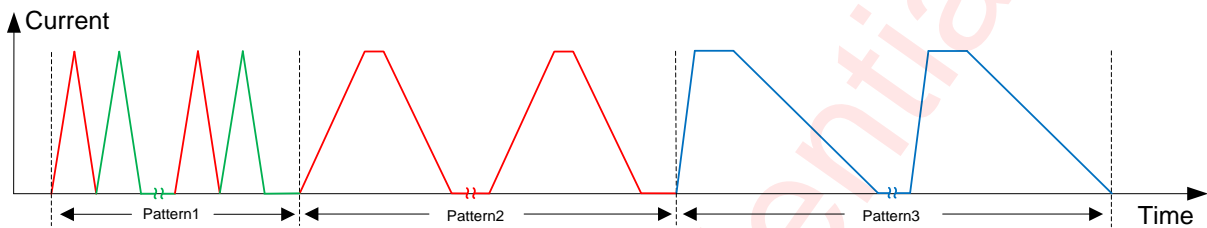
Figure 12 Example of single-pulse/single-color true-color pattern

The following figure is an example of multi pulse and multi-color pattern repeating in true-color pattern mode.



**Figure 13** Example of 2-pulse/2-color in true-color pattern

The following figure is another example of three patterns running successively in true-color pattern mode.



**Figure 14** Example of 3 pattern running successively in true-color mode

## INDIVIDUAL BREATHING LIGHTING

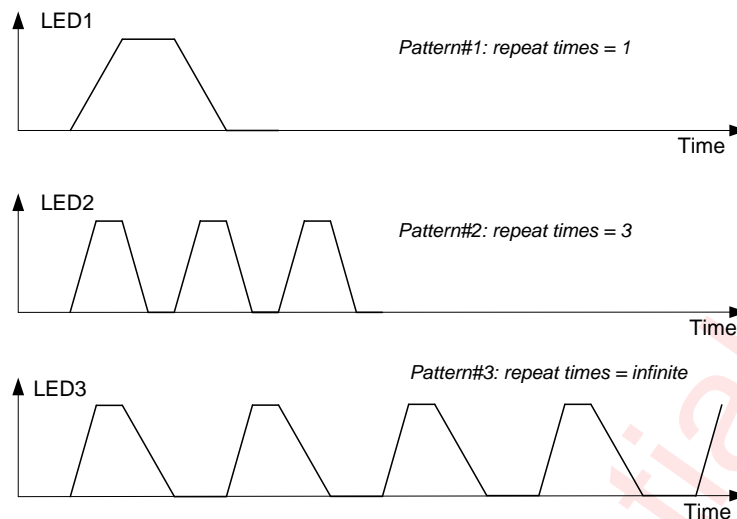
In some application where three LED need blinking individually. When register bit LCFGx.LEDMD (register: 0x04/0x05/0x06 bit0) is set to 1, the corresponding LEDx operates in pattern mode. If register bit LEDCTR.SYNC (register: 0x08 bit3) is 0, all pattern run in individually. In this mode, the 3 internal pattern controllers and 3 groups of pattern parameters are distributed to 3 LED channel respectively. Each LED can be controlled independently to blink according to its own pattern definition.

In this mode, multi-pulse pattern is supported, but multi-color is not supported, the bits CE1~CE4 in register PATx\_T4 are ignored. Only registers ILEDx\_1 is active for LED current setting, the other register including ILEDx\_2, ILEDx\_3 and ILEDx\_4 are all useless.

The following table gives the current, pattern parameter and the start/stop control source selection for each LED channel in individual breathing lighting mode.

Channel	Current Setting Register	Pattern used	Pattern Start	Pattern Stop
LED1	ILED1_1 (register: 0x10)	pattern #1	write 1 to PATRUN bit0	write 1 to PATRUN bit4
LED2	ILED2_1 (register: 0x11)	pattern #2	write 1 to PATRUN bit1	write 1 to PATRUN bit5
LED3	ILED3_1 (register: 0x12)	pattern #3	write 1 to PATRUN bit2	write 1 to PATRUN bit6

The following figure shows an example of 3 patterns run individually with different pattern parameters.



**Figure 15** Example of Individual Pattern Mode

## MANUAL CONTROL MODE

When control bit LCFGx.LEDMD (register: 0x04/0x05/0x06 bit0) is set to 0, the corresponding LEDx is work in manual control mode.

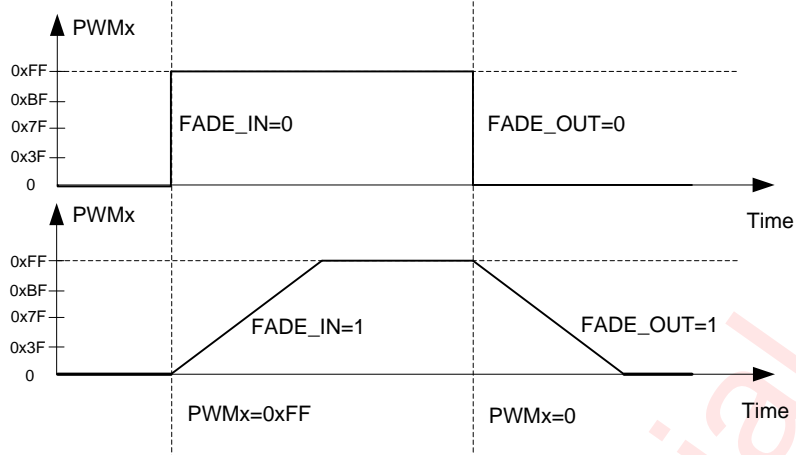
In manual control mode, the LED lighting effects including color-mixed and brightness is directly configured by setting current/ PWM level register via I2C interface.

When LEDCTR.SYNC (register: 0x08, bit3) is set to 0, three LEDs are controlled individually, the PWM level and current for each is defined by PWM1/PWM2/PWM3 (register: 0x1C/0x1D/0x1E) and ILEDx\_1 (register 0x10/0x11/0x12) respectively.

When LEDCTR.SYNC (register: 0x08, bit3) is set to 1, the output currents of three LED are defined by register ILEDx\_1 respectively, but their PWM level are determined commonly by register PWM1. So user can change the brightness of all LED simultaneously by modifying the value of register PWM1 only.

Channel	Current	Brightness		Trise and Tfall time	
		SYNC=0	SYNC=1	SYNC=0	SYNC=1
LED1	ILED1_1	PWM1	PWM1	PAT1_T1/T2	PAT1_T1/T2
LED2	ILED2_1	PWM2		PAT2_T1/T2	
LED3	ILED3_1	PWM3		PAT3_T1/T2	

In manual control mode, auto dimming is supported. If LCFGx.FADE\_OUT (register: 0x04, 0x05 0x06 bit2) is set to 1, automatic fade-out is enabled. If LCFGx.FADE\_IN (register: 0x04, 0x05, 0x06 bit1) is set to 1, automatic fade-in is enabled. If a new value is set on PWMx register and auto dimming is enabled, the brightness of LED output ramp up/down smoothly, with its Trise and Tfall time defined by corresponding pattern configuration (PATx\_T1 and PATx\_T2).

**Figure 16** Manual Control Mode

## REGISTER DESCRIPTION

## REGISTER LIST

Addr (Hex)	Name	R/W	7	6	5	4	3	2	1	0	
00	RSTIDR	R/W	0	0	1	1	0	0	0	1	
01	GCR	R/W	-	-	-	-	-	PWM_F	RESERVE	CHIPEN	
02	STATUS	R	-	-	-	PUIS	-	LS2	LS1	LS0	
03	IMAX	R/W	-	-	-	-	-	-	IMAX		
04	LCFG1	R/W	-	-	-	-	-	FADE_OUT	FADE_IN	LEDMD	
05	LCFG2	R/W	-	-	-	-	-	FADE_OUT	FADE_IN	LEDMD	
06	LCFG3	R/W	-	-	-	-	-	FADE_OUT	FADE_IN	LEDMD	
07	LEDEN	R/W	-	-	-	-	-	LED3EN	LED2EN	LED1EN	
08	LEDCTR	R/W	-	-	-	-	SYNC	-	PWMLOG		
09	PATRUN	R/W	-	STOP3	STOP2	STOP1	-	RUN3	RUN2	RUN1	
10	ILED1_1	R/W	ILED1_1								
11	ILED2_1	R/W	ILED2_1								
12	ILED3_1	R/W	ILED3_1								
13	ILED1_2	R/W	ILED1_2								
14	ILED2_2	R/W	ILED2_2								
15	ILED3_2	R/W	ILED3_2								
16	ILED1_3	R/W	ILED1_3								
17	ILED2_3	R/W	ILED2_3								
18	ILED3_3	R/W	ILED3_3								
19	ILED1_4	R/W	ILED1_4								
1A	ILED2_4	R/W	ILED2_4								
1B	ILED3_4	R/W	ILED3_4								
1C	PWM1	R/W	PWM1								
1D	PWM2	R/W	PWM2								
1E	PWM3	R/W	PWM3								
30	PAT1_T1	R/W	TRISE				TON				
31	PAT1_T2	R/W	TFALL				TOFF				
32	PAT1_T3	R/W	-	TSLOT				TDELAY			
33	PAT1_T4	R/W	PAT_CTR	PAT_SW	MPULSE	CE4	CE3	CE2	CE1		
34	PAT1_T5	R/W	REPTIM								
35	PAT2_T1	R/W	TRISE				TON				
36	PAT2_T2	R/W	TFALL				TOFF				
37	PAT2_T3	R/W	-	TSLOT				TDELAY			
38	PAT2_T4	R/W	PAT_CTR	PAT_SW	MPULSE	CE4	CE3	CE2	CE1		
39	PAT2_T5	R/W	REPTIM								
3A	PAT3_T1	R/W	TRISE				TON				
3B	PAT3_T2	R/W	TFALL				TOFF				
3C	PAT3_T3	R/W	-	TSLOT				TDELAY			
3D	PAT3_T4	R/W	PAT_CTR	PAT_SW	MPULSE	CE4	CE3	CE2	CE1		
3E	PAT3_T5	R/W	REPTIM								

## DETAILED REGISTER DESCRIPTION

## RSTIDR, Chip ID and Software Reset Register

Address: 0x00, R/W, default: 0x31

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Symbol	Description
7:0	IDR	Chip ID, 0x31 Reset: write 0x55 to RSTIDR, reset internal logic and register

**GCR, Global Control Register**

Address: 0x01, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	PWM_F	RESERVE	CHIPEN

Bit	Symbol	Description
2	PWM_F	PWM Modulation Frequency Select 0: 122Hz PWM modulation 1: 245Hz PWM modulation
1	RESERVE	Should be set to "1"
0	CHIPEN	Device operating Enable 0: Disable, the device is in standby state 1: Enable, the device enters active state

**STATUS Register**

Address: 0x02, Read only, default: 0x10

7	6	5	4	3	2	1	0
0	0	0	PUIS	-	LS3	LS2	LS1

Bit	Symbol	Description
4	PUIS	Power Up Interrupt Status 0: No power-up reset has taken place 1: Power-up reset has taken place
2	LS3	operating status indication for pattern controller 3 0: stop state 1: running state
1	LS2	operating status indication for pattern controller 2 0: stop state 1: running state
0	LS1	operating status indication for pattern controller 1 0: stop state 1: running state

**IMAX, LED Maximum Current Register**

Address: 0x03, R/W, default: 0x01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	IMAX	

Bit	Symbol	Description
1:0	IMAX	Maximum LED output Current Select 00: 3.1875mA 01: 6.375mA 10: 12.75mA 11: 25.5mA

**LCFG1-3 LED Configure Register**

LCFG1: Address: 0x04, R/W, default: 0x01  
 LCFG2: Address: 0x05, R/W, default: 0x00  
 LCFG3: Address: 0x06, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	FADE_OUT	FADE_IN	LEDMD

Bit	Symbol	Description
2	FADE_OUT	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable, 1: PWM fade-out is enable, the dimming time decide by $T_{FALL}$
1	FADE_IN	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable, 1: PWM fade-in is enable, the dimming time decide by $T_{RISE}$
0	LEDMD	LED Operating Mode Select. 0: Manual mode, LEDx is control directly by register ILEDx_1 and PWMx 1: Pattern mode

### LEDEN, LED Channel Enable Register

Address: 0x07, R/W, default: 0x01

7	6	5	4	3	2	1	0
-	-	-	-	-	LED3EN	LED2EN	LED1EN

Bit	Symbol	Description
2	LED3EN	LED3 Enable 0: LED3 module stop work and LED3 out disable 1: LED3 output is enabled
1	LED2EN	LED2 Enable 0: LED2 module stop work and LED2 out disable 1: LED2 output is enabled
0	LED1EN	LED1 Enable 0: LED1 module stop work and LED1 out disable 1: LED1 output is enabled

### LEDCTR, LED Control Register

Address: 0x08, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	SYNC	-	PWMLOG	

Bit	Symbol	Description
3	SYNC	LED Breathing Synchronous Mode Select 0: 3 LED work in asynchronous mode with independent control 1: 3 LED work in synchronous mode for RGB application.
1:0	PWMLOG	PWM Logarithmic curve select 0x: Log60 10: Log10 11: Linearity

### PATRUN, Pattern Run/Stop Register

Address: 0x09, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	STOP3	STOP2	STOP1	-	RUN3	RUN2	RUN1

Bit	Symbol	Description
6	STOP3	Write 1, LED3 pattern stop if independent mode; The bit clears to 0 automatically after write 1.
5	STOP2	Write 1, LED2 pattern stop if independent mode; The bit clears to 0 automatically after write 1.
4	STOP1	Write 1, LED1 pattern stop if independent mode; Write 1, pattern stop if pattern mode; The bit clears to 0 automatically after write 1.
2	RUN3	Write 1, LED3 pattern run if independent mode; The bit clears to 0 automatically after write 1.
1	RUN2	Write 1, LED2 pattern run if independent mode; The bit clears to 0 automatically after write 1.
0	RUN1	Write 1, LED1 pattern run if independent mode; Write 1, pattern run if pattern mode; The bit clears to 0 automatically after write 1.

**ILED1\_y, LED1 Current Register**

ILED1\_1: Address: 0x10, R/W, default: 0xFF

ILED1\_2: Address: 0x13, R/W, default: 0x00

ILED1\_3: Address: 0x16, R/W, default: 0x00

ILED1\_4: Address: 0x19, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED1_y							

Bit	Symbol	Description
7:0	ILED1_y	LED1 Current Configure Register for 4 pre-defined colors, The LED1 output current value is $IMAX * ILED1_y / 255$ .

**ILED2\_y, LED2 Current Register**

ILED2\_y: Address: 0x11/0x14/0x17/0x1A, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED2_y							

Bit	Symbol	Description
7:0	ILED2_y	LED2Current Configure Register for 4 pre-defined colors, The LED2 output current value is $IMAX * ILED2_y / 255$ .

**ILED3\_y, LED3 Current Register**

ILED3\_y: Address: 0x12/0x15/0x18/0x1B, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED3_y							

Bit	Symbol	Description
7:0	ILED3_y	LED3 Current Configure Register, for 4 pre-defined colors The LED3 output current value is $IMAX * ILED3_y / 255$ .

**PWM1/PWM2/PWM3 , PWM duty level Register**

PWM1: Address: 0x1C, R/W, default:0xFF

PWM2: Address: 0x1D, R/W, default:0x00

PWM3: Address: 0x1E, R/W, default:0x00

7	6	5	4	3	2	1	0
PWMx							

Bit	Symbol	Description
7:0	PWMx	PWM level for LEDx (x=1,2,3)

**PATx\_T1, Time Parameter of Pattern x Register**

PAT1\_T1: Address: 0x30, R/W, default: 0x80

PAT2\_T1: Address: 0x35, R/W, default: 0x00

PAT3\_T1: Address: 0x3A, R/W, default: 0x00

7	6	5	4	3	2	1	0
TRISE				TON			

Bit	Symbol	Description			
7:4	TRISE	Rise Time of pattern:			
		TRISE	Time	TRISE	Time
		0000	0s	1000	2.1s
		0001	0.13s	1001	2.6s
		0010	0.26s	1010	3.1s
		0011	0.38s	1011	4.2s
		0100	0.51s	1100	5.2s
		0101	0.77s	1101	6.2s
		0110	1.04s	1110	7.3s
		0111	1.6s	1111	8.3s
3:0	TON	On Time of pattern:			
		TON	Time	TON	Time
		0000	0.04s	1000	2.1s
		0001	0.13s	1001	2.6s
		0010	0.26s	1010	3.1s
		0011	0.38s	1011	4.2s
		0100	0.51s	1100	5.2s
		0101	0.77s	1101	6.2s
		0110	1.04s	1110	7.3s
		0111	1.6s	1111	8.3s

**PATx\_T2, Time Parameter of Pattern x Register**

PAT1\_T2: Address: 0x31, R/W, default: 0x86

PAT2\_T2: Address: 0x36, R/W, default: 0x00

PAT3\_T2: Address: 0x3B, R/W, default: 0x00

7	6	5	4	3	2	1	0
TFALL				TOFF			

Bit	Symbol	Description					
6:4	TFALL	Fall Time of pattern:					
		TFALL	Time	TFALL	Time		
		0000	0s	1000	2.1s		
		0001	0.13s	1001	2.6s		
		0010	0.26s	1010	3.1s		
		0011	0.38s	1011	4.2s		
		0100	0.51s	1100	5.2s		
		0101	0.77s	1101	6.2s		
		0110	1.04s	1110	7.3s		
		0111	1.6s	1111	8.3s		
2:0	TOFF	Off Time of pattern:					
		TOFF	Time	TOFF	Time		
		0000	0.04s	1000	2.1s		
		0001	0.13s	1001	2.6s		
		0010	0.26s	1010	3.1s		
		0011	0.38s	1011	4.2s		
		0100	0.51s	1100	5.2s		
		0101	0.77s	1101	6.2s		
		0110	1.04s	1110	7.3s		
		0111	1.6s	1111	8.3s		

**PATx\_T3, Time Parameter of Pattern x Register**

PAT1\_T3: Address: 0x32, R/W, default: 0x00

PAT2\_T3: Address: 0x37, R/W, default: 0x00

PAT3\_T3: Address: 0x3C, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	TSLOT			TDELAY			

Bit	Symbol	Description			
6:4	TSLOT	Slot Time Between Pulses:			
		TSLOT	Time		
		000	0ms		
		001	130ms		
		010	260ms		
		011	380ms		
		100	540ms		
		101	670ms		
110	800ms				
111	1024ms				

3:0 TDELAY Startup Delay Time of Pattern:

TDELAY	Time	TDELAY	Time
0000	0s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

**PATx\_T4, Time Parameter of Pattern x Register**

PAT1\_T4: Address: 0x33, R/W, default: 0x00

PAT2\_T4: Address: 0x38, R/W, default: 0x00

PAT3\_T4: Address: 0x3D, R/W, default: 0x00

7	6	5	4	3	2	1	0
PAT_CTR	PAT_SW	MPULSE		CE4	CE3	CE2	CE1

Bit	Symbol	Description
7	PAT_CTR	Pattern running forever control 0: pattern run forever 1: pattern stop or switch to next pattern after repeating specified times.
6	PAT_SW	Pattern Switch enable, active only in true-color pattern mode. 0: Pattern switch is disabled 1: Pattern switch is enabled
5:4	MPULSE	Multiple Pulse mode selection. 00: single pulse 01: pulse repeats 2 times 10: pulse repeats 3 times 11: pulse repeats 4 times
3	CE4	Color #4 display enable 0: Color#4 is masked 1: Color#4 is allow to display
2	CE3	Color #3 display enable 0: Color#3 is masked 1: Color#3 is allow to display
1	CE2	Color #2 display enable 0: Color#2 is masked 1: Color#2 is allow to display
0	CE1	Color #1 display enable 0: Color#1 is masked 1: Color#1 is allow to display Note: if CE1~CE4 are all set to 0, Color #1 is displayed by default

**PATx\_T5, Time Parameter of Pattern x Register**

PAT1\_T5: Address: 0x34, R/W, default: 0x00

PAT2\_T5: Address: 0x39, R/W, default: 0x00

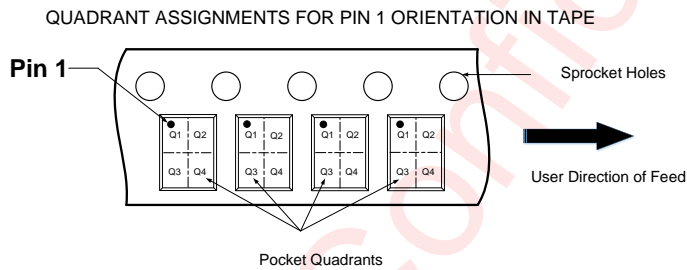
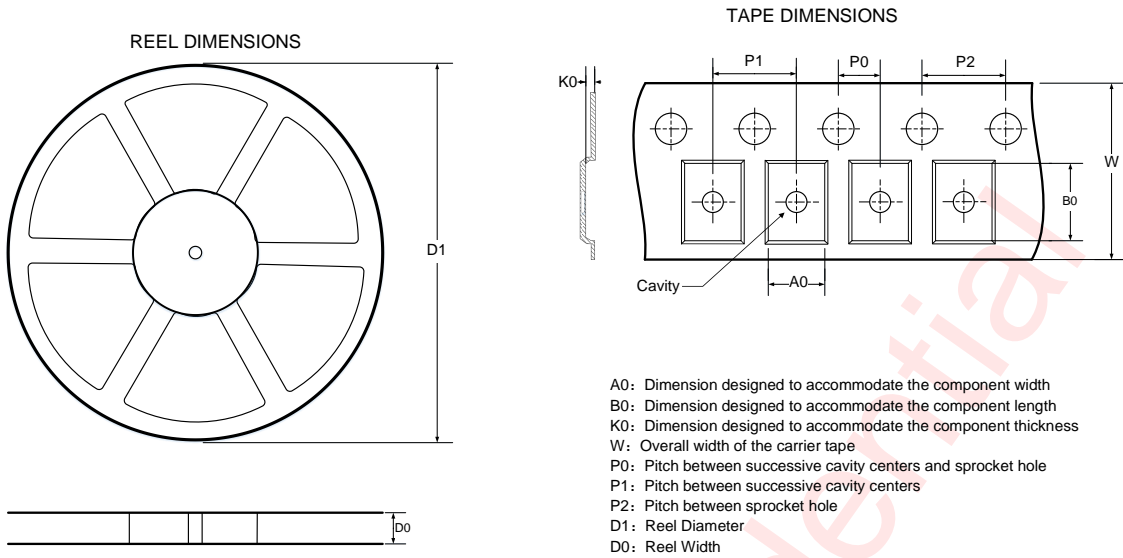
PAT3\_T5: Address: 0x3E, R/W, default: 0x00

7	6	5	4	3	2	1	0
REPTIM							

Bit	Symbol	Description
7:0	REPTIM	PATTERN Repeat Times REPTIM [7] = 0: Pattern repeats REPTIM[6:0]+1 times REPTIM [7] = 1: Pattern repeats (REPTIM[6:0]+1) * 16 times

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## TAPE AND REEL INFORMATION



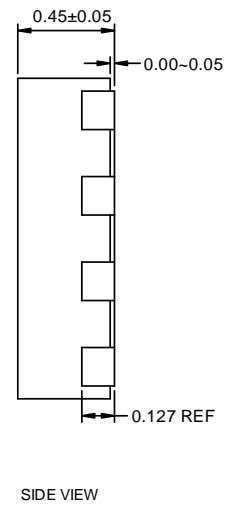
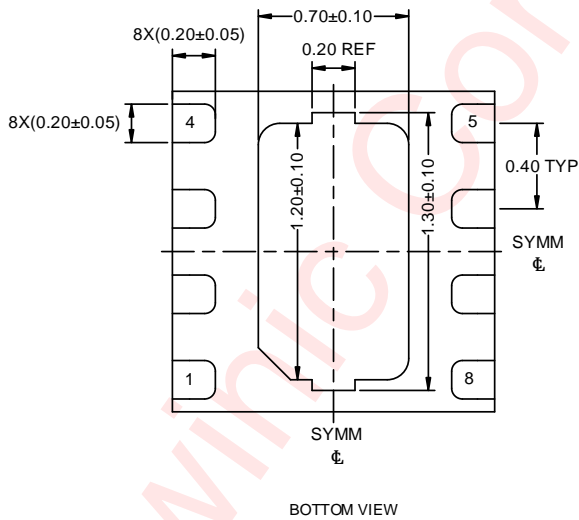
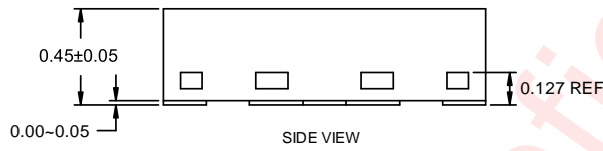
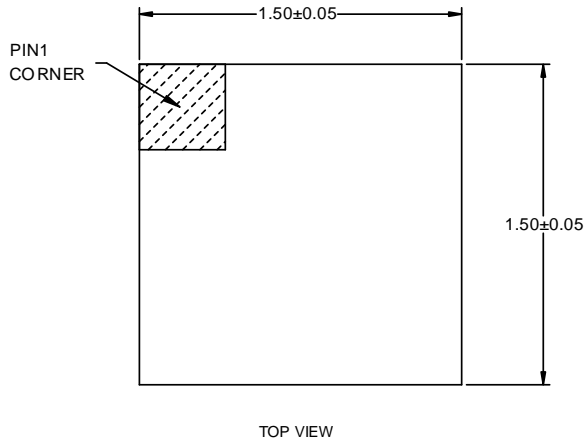
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

**DIMENSIONS AND PIN1 ORIENTATION**

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
180	9.5	1.7	1.7	0.75	2	4	4	8	Q1

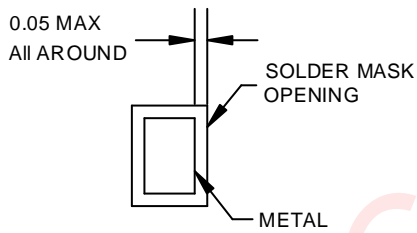
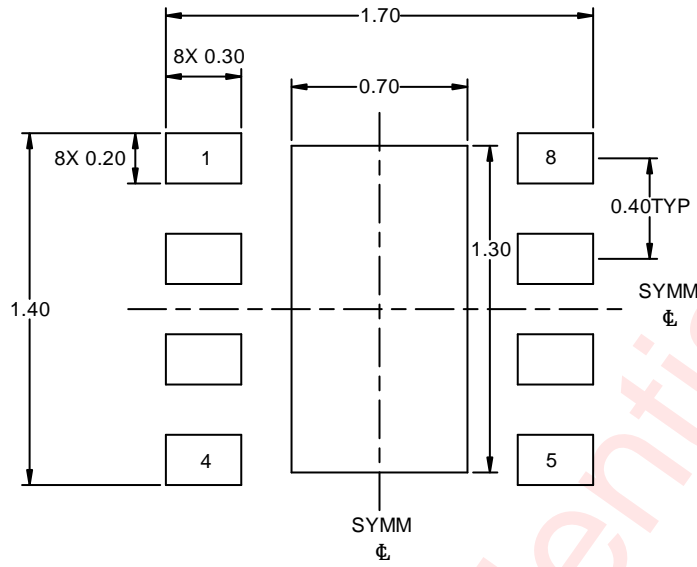
All dimensions are nominal

PACKAGE DESCRIPTION

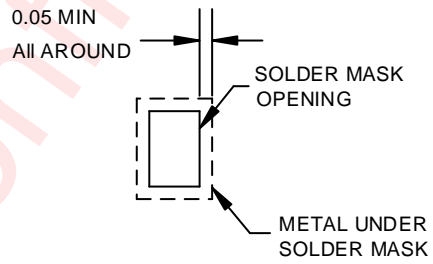


Unit: mm

LAND PATTERN EXAMPLE



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

## REFLOW

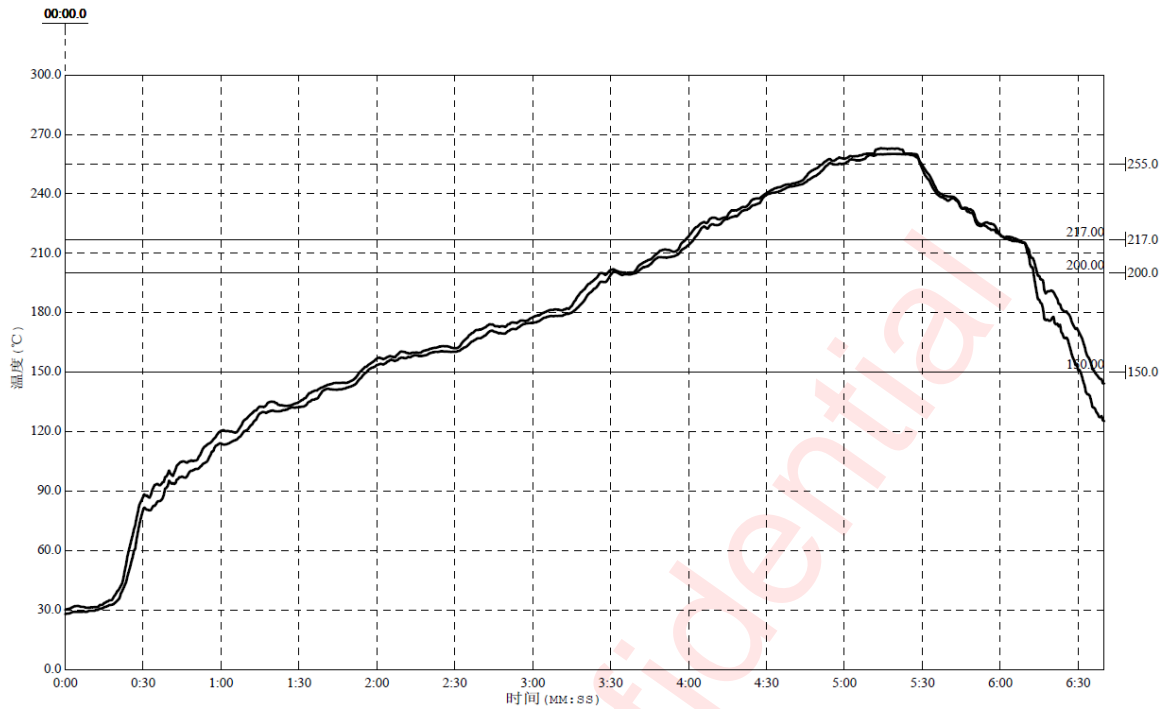


Figure 1 Package Reflow Oven Thermal Profile

Reflow Note	Spec
Average ramp-up rate (217°C to Peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec.
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min.

## REVISION HISTORY

Vision	Date	Change Record
V0.9	June 2016	Datasheet V0.9 Released
V0.91	July 2016	Datasheet V0.91 Released
V1.0	October 2016	Datasheet V1.0 Released
V1.1	November 2016	<ol style="list-style-type: none"> <li>Added Pin 1 and Land pattern information;</li> <li>Corrected mistake at pin configuration.</li> </ol>
V1.2	December 2017	<ol style="list-style-type: none"> <li>Added exposed pad description in Pin definition;</li> <li>Added RoHS and MSL statements in Ordering information.</li> </ol>
V1.3	September 2018	<ol style="list-style-type: none"> <li>Refreshed Land Pattern Example (P28);</li> <li>Refreshed Pin1 information (P26);</li> <li>Refreshed AMR ESD and Temperature information (P4);</li> <li>Refreshed Package Description (P28).</li> </ol>
V1.4	December 2020	<ol style="list-style-type: none"> <li>Refreshed Land Pattern Example (P28);</li> <li>Refreshed Pin1 information (P27);</li> </ol>
V1.5	December 2022	<ol style="list-style-type: none"> <li>0X02 Status Register Read only(P20);</li> </ol>
V1.6	July 2023	<ol style="list-style-type: none"> <li>Refreshed bit4-6 PATx_T3. TSLOT (P13);</li> <li>Refreshed PATx_T4 (register: 0x33/0x38/0x3D) (P13);</li> <li>Refreshed PATx_T4. PAT_SW (register: 0x33/0x38/ 0x3D) (P14);</li> <li>Refreshed ILED1_y bit 7:0 (P21);</li> <li>0X00 RSTIDR Register LIST R/W (P18).</li> <li>Deleted note1 recommended operating conditions (P4).</li> <li>Modified ESDA/JEDEC JS-001-2017(HBM) (P4).</li> <li>Modified JEDEC JESD78F-2022 (Latch-up) (P4).</li> </ol>

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