

## Triple Outputs Switching Converter for AMOLED Display

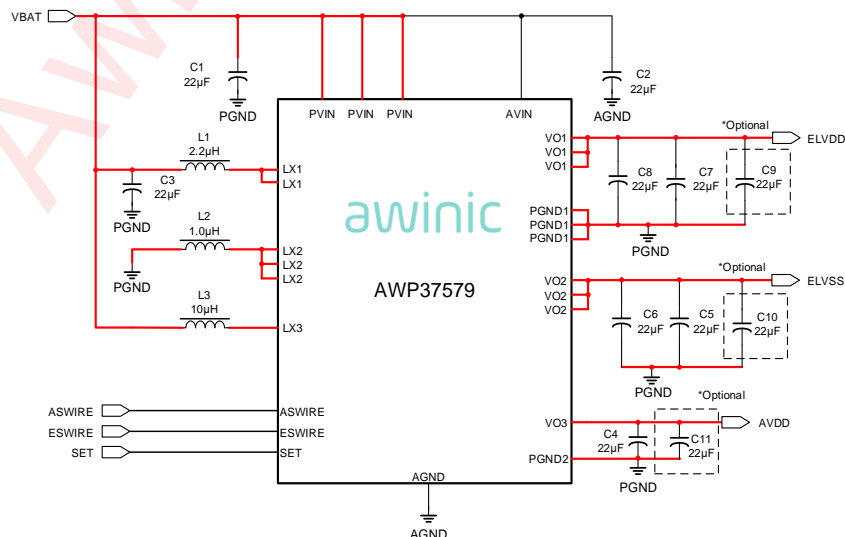
### FEATURES

- Input voltage: 2.5V ~ 4.8V
- Excellent line and load transient response
- Programmable output voltage by ESWIRE from 4.6V to 5V in 100mV steps (Default: 4.6V)
- Programmable output voltage by ESWIRE from -6.6V to -0.5V in 100mV steps (Default: -4V)
- Programmable output voltage by ASWIRE from 6.5 V to 8.0V in 50mV or in 100mV steps (Default: 7.6V)
- Max Output current for ELVDD and ELVSS
- **1000mA @  $V_{IN}=2.5V$ , ELVDD=4.6V, ELVSS= -4V**
- **1000mA @  $V_{IN}=2.7V$ , ELVDD=4.6V, ELVSS= -5.5V**
- 150mA Max Output current for AVDD
- Short Circuit Protection (SCP)
- WLCSP 2.017x2.017 - 25B

### APPLICATIONS

Active Matrix OLED

### TYPICAL APPLICATION CIRCUIT

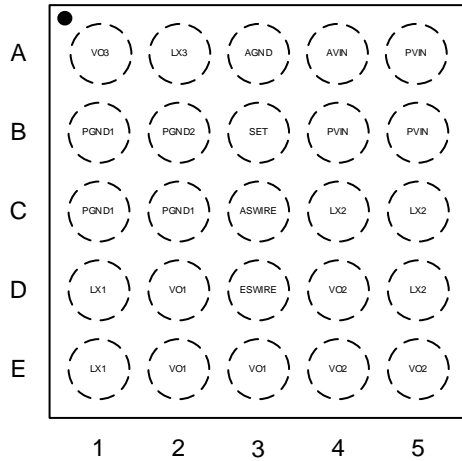
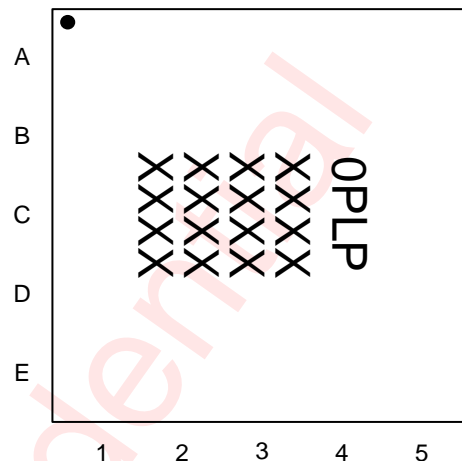


### GENERAL DESCRIPTION

The AWP37579CSR is specially designed for AMOLED (Active Matrix organic LED) Display panels. It integrates two high performance boost converters, VO1 (positive voltage ELVDD) and VO3 (AVDD), one inverting buck-boost converter for VO2 (negative voltage ELVSS). These converters have excellent line and load transient response.

The VO3 can be programmed by ASWIRE, the VO1 and VO2 can be programmed by ESWIRE. All these interfaces can turn on/off corresponding converters.

## PIN CONFIGURATION AND TOP MARK

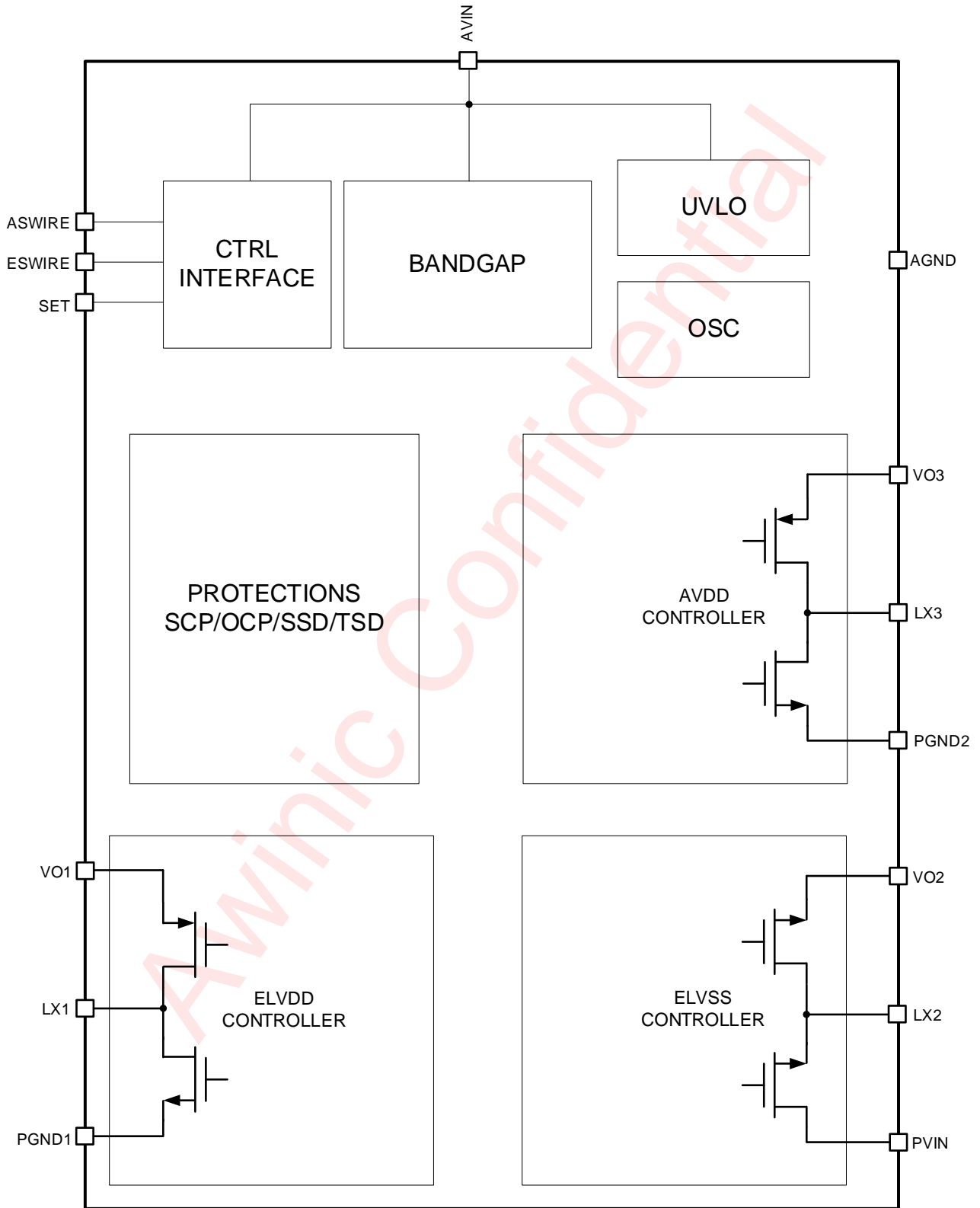
AWP37579CSR  
(Top View)AWP37579CSR Marking  
(Top View)

0PLP - AWP37579CSR  
XXXX/XXXX/XXXX/XXXX - Production Tracing Code

## PIN DEFINITION

Ball No.	Symbol	I/O	Description
D1, E1	LX1	Output	Switching node of ELVDD Boost converter
D2, E2, E3	VO1	Output	Output voltage of ELVDD Boost converter
B1, C1, C2	PGND1	GND	Power ground for ELVDD Boost converter
C4, C5, D5	LX2	Output	Switching node of ELVSS inverting Buck-Boost converter
D4, E4, E5	VO2	Output	Output voltage of ELVSS inverting Buck-Boost converter
A5, B4, B5	PVIN	Input	Input supply voltage for Power
A2	LX3	Output	Switching node of AVDD Boost converter
A1	VO3	Output	Output voltage of AVDD Boost converter
B2	PGND2	GND	Power ground for AVDD Boost converter
A4	AVIN	Input	Input supply voltage for analog
A3	AGND	GND	Analog ground
D3	ESWIRE	Input	S-wire control input (Active-High) for ELVDD and ELVSS
C3	ASWIRE	Input	S-wire control input (Active-High) for AVDD
B3	SET	Input	GPIO input to select AVDD output voltage range and steps

FUNCTIONAL BLOCK DIAGRAM



**ORDERING INFORMATION**

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP37579CSR	-40°C ~ 85°C	WLCSP 2.017×2.017 - 25B	0PLP	MSL1	RoHS+HF	4500 units/ Tape and Reel

**ABSOLUTE MAXIMUM RATINGS**(NOTE 1)

PARAMETERS		RANGE
Supply voltage range AVIN, PVIN		-0.3V to 6V
Input voltage range	ASWIRE, ESWIRE, SET	-0.3V to 6V
Output voltage range	VO1	-0.3V to 6V
	LX1	-0.3V to 7V
	VO3	-0.3V to 10V
	LX3	-0.3V to VO3+0.3V
	VO2	-8V to 0.3V
	LX2	-8V to PVIN+0.3V
Operating free-air temperature range T <sub>A</sub>		-40°C to 85°C
Operating junction temperature range T <sub>J</sub>		-40°C to 125°C
Maximum operating junction temperature T <sub>JMAX</sub>		165°C
Storage temperature T <sub>STG</sub>		-65°C to 160°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including HBM CDM)(NOTE 2)		
HBM		±2kV
CDM		±1.5kV
Latch-Up		
Test standard: JESD78F		+IT: +200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023(HBM). ESDA/JEDEC JS-002-2022(CDM).

## Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IN}$	Input voltage	2.5	3.7	4.8	V
$C_{IN}$	Input capacitance	40	66		$\mu F$
$C_{OUT(NOTE\ 3)}$	Output capacitance	$C_{OUT}$ of VO1	44		$\mu F$
		$C_{OUT}$ of VO2	44		$\mu F$
		$C_{OUT}$ of VO3	22		$\mu F$
$L_1(NOTE\ 4)$	Inductance for VO1		2.2		$\mu H$
			4.7		$\mu H$
$L_2(NOTE\ 4)$	Inductance for VO2		1.0		$\mu H$
			2.2		$\mu H$
$L_3(NOTE\ 4)$	Inductance for VO3		10		$\mu H$
			4.7		$\mu H$
$T_A$	Operating free-air temperature range	-40	25	85	$^{\circ}C$

**NOTE3:** The minimum value of the required capacitor for 900mA load at  $V_{VO1} = 4.6V$  or  $V_{VO2} = -4.0V$  is  $13.2\mu F$  and for 150mA load at  $V_{VO3} = 7.6V$  is  $3.9\mu F$ . In order to improve the stability at lower input voltage and heavy loads, it is recommended that another  $22\mu F$  capacitor be added to the VO1 and VO2 outputs.

**NOTE4:** In addition to typical application, AWP37579CSR can supports  $L1 = 4.7\mu H$ ,  $L2 = 2.2\mu H$  and  $L3 = 4.7\mu H$ .

**ELECTRICAL CHARACTERISTICS**

AVIN = PVIN = 3.7V, VVO1 = 4.6V, VVO2 = -4V, VVO3 = 7.6V, typical values are at TA = TJ = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT AND THERMAL PROTECTION</b>						
AVIN, PVIN	Input voltage range		2.5	3.7	4.8	V
ISD	Shutdown current	ASWIRE = ESWIRE = GND, total current flowing into AVIN and PVIN			1.5	μA
Iq	Quiescent current	ASWIRE = ESWIRE = HIGH, total current flowing into AVIN and PVIN			6	mA
VUVLO	Under-voltage lockout threshold	AVIN Falling	1.75	2.05	2.15	V
		AVIN Rising	1.85	2.15	2.25	V
TSD	Thermal shutdown temperature	Temperature Rising		165		°C
<b>ELVDD BOOST CONVERTER(VO1)</b>						
VVO1	Output voltage		4.6	4.6	5	V
	Output voltage accuracy	No load	-0.5		0.5	%
No load, TA = -40°C to +85°C		-0.8		0.8	%	
IO1MAX(NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V, VVO2 = -4V	1000			mA
		AVIN = PVIN = 2.7V ~ 4.8V, VVO2 = -5.5V	1000			mA
RDSONS	Switch on-resistance	IDS = 200 mA		80		mΩ
RDSONR	Rectifier on-resistance			60		mΩ
fSW1	Switching frequency			1.45		MHz
			-10		10	%
ILIMIT1	Switch current limit	Inductor peak current	2.8	3.5		A
VSCP1	Short-circuit threshold in operation	Voltage decrease from nominal VVO1		0.9x		V
tSCP1	Short-circuit detection time in operation			1		ms
RDCHG	Discharge resistance	FD = ON, IO1 = 1mA	30	50	70	Ω
Line Regulation	VVO1_LINEREG	IO1 = 100mA, VIN = 2.5V to 4.8V		10		mV
Load Regulation	VVO1_LOADREG	IO1 = 1mA ~ 1000mA		25		mV
<b>ELVSS INVERTING BUCK-BOOST CONVERTER (VO2)</b>						
VVO2	Output voltage range		-6.6	-4.0	-0.5	V
	Output voltage accuracy	No load	-25		25	mV
No load, TA = -40°C to +85°C		-40		40	mV	
IO2MAX(NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V, VVO2 = -4V			-1000	mA
		AVIN = PVIN = 2.7V ~ 4.8V, VVO2 = -5.5V			-1000	mA
RDSONS	Switch on-resistance	IDS = 200 mA		45		mΩ
RDSONR	Rectifier on-resistance			45		mΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>SW2</sub>	Switching frequency			1.45		MHz
			-10		10	%
I <sub>LIMIT2</sub>	Switch current limit	AVIN = PVIN = 2.5 V	4.8	5.8		A
R <sub>DCHG</sub>	Discharge resistance	FD = ON, I <sub>O2</sub> = 1 mA	30	50	70	Ω
V <sub>SCP2</sub>	Short circuit threshold in operation	Voltage increase from nominal V <sub>VO2</sub>		0.8x V <sub>VO2</sub>		V
t <sub>SCP2</sub>	Short circuit detection time in operation			1		ms
V <sub>SSD</sub>	Start-up short detection threshold			200		mV
t <sub>SSD</sub>	Start-up short detection time			5		ms
Line Regulation	V <sub>VO2_LINEREG</sub>	I <sub>O2</sub> = 100mA, V <sub>IN</sub> = 2.5V to 4.8V		10		mV
Load Regulation	V <sub>VO2_LINEREG</sub>	I <sub>O2</sub> = 1mA ~ 1000mA		25		mV
<b>AVDD BOOST CONVERTER (VO3)</b>						
V <sub>VO3</sub>	Output voltage	SET = HIGH (step: 50mV)	6.5	7.6	8.0	V
		SET = LOW (step: 100mV)	6.5	7.6	8.0	V
	Output voltage accuracy	No load	-0.8		0.8	%
		No load, T <sub>A</sub> = -40°C to +85°C	-1.0		1.0	%
I <sub>O3MAX</sub> (NOTE 5)	Maximum Output Current	AVIN = PVIN = 2.5V ~ 4.8V	150			mA
R <sub>DSONS</sub>	Switch on-resistance	I <sub>DS</sub> = 30 mA		300		mΩ
R <sub>DSONR</sub>	Rectifier on-resistance			500		mΩ
f <sub>SW3</sub>	Switching frequency			1.45		MHz
			-10		10	%
I <sub>LIMIT3</sub>	Switch current limit	Inductor peak current	0.8	1.0		A
R <sub>DCHG</sub>	Discharge resistance	FD = ON, I <sub>O3</sub> = 1 mA	40	70	100	Ω
V <sub>SCP3</sub>	Short-circuit threshold in operation	Voltage decrease from nominal V <sub>VO3</sub>		0.8x V <sub>VO3</sub>		V
t <sub>SCP3</sub>	Short-circuit detection time in operation			1		ms
Line Regulation	V <sub>VO3_LINEREG</sub>	I <sub>O3</sub> = 50mA, V <sub>IN</sub> = 2.5V to 4.8V		5		mV
Load Regulation	V <sub>VO3_LINEREG</sub>	I <sub>O3</sub> = 1mA ~ 150mA		10		mV
<b>LOGIC SET</b>						
V <sub>IH</sub>	High level input voltage	AVIN = PVIN = 2.5V ~ 4.8V	0.84			V
V <sub>IL</sub>	Low level input voltage	AVIN = PVIN = 2.5V ~ 4.8V			0.36	V
<b>CTRL INTERFACE(ASWIRE,ESWIRE)</b>						
V <sub>IH</sub>	High level input voltage	AVIN = PVIN = 2.5V ~ 4.8V	0.84			V
V <sub>IL</sub>	Low level input voltage	AVIN = PVIN = 2.5V ~ 4.8V			0.36	V
R <sub>SWIRE</sub>	Pull down resistance of ASWIRE and ESWIRE interfaces	V <sub>SWIRE</sub> = 1.8V		300		kΩ
t <sub>LOW</sub> (NOTE 6)	Low-level pulse duration		2	10	25	μs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>HIGH</sub> (NOTE 6)	High-level pulse duration		2	10	25	μs
t <sub>OFF</sub> (NOTE 6)	Shutdown pulse duration(ASWIRE/ESWIRE = low)		200			μs
t <sub>INIT</sub> (NOTE 6)	Initialization time			400	500	μs
t <sub>STORE</sub> (NOTE 6)	Data storage/accept time period		160			μs
<b>POWER SEQUENCE</b>						
t <sub>DELAY</sub> (NOTE 6)	VO2 start up time delay VO1			5		ms
t <sub>SS1</sub> (NOTE 6)	VO1 soft-start time			3		ms
t <sub>SS2</sub> (NOTE 6)	VO2 soft-start time			3		ms
t <sub>SS3</sub> (NOTE 6)	VO3 soft-start time			3		ms

NOTE5: The specific parameters of the peripheral inductors for maximum output current are as follows:

L1: DFE252012F-2R2M=P2 3.3A, 82mΩ, 252012 L2: SKFB252010-1R0M 4.4A, 38mΩ, 252010

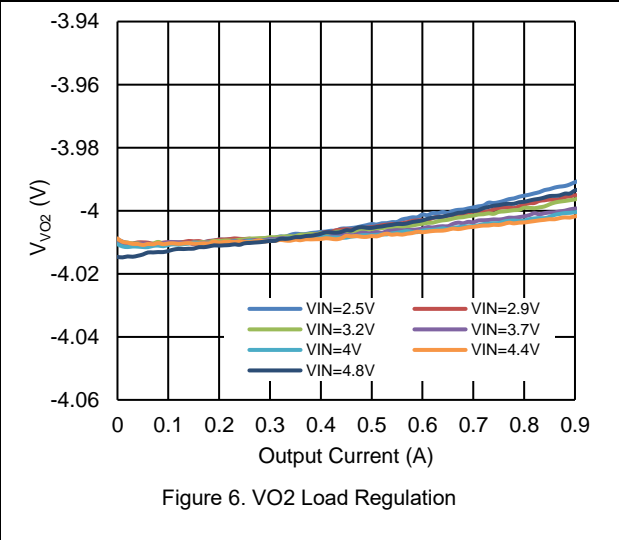
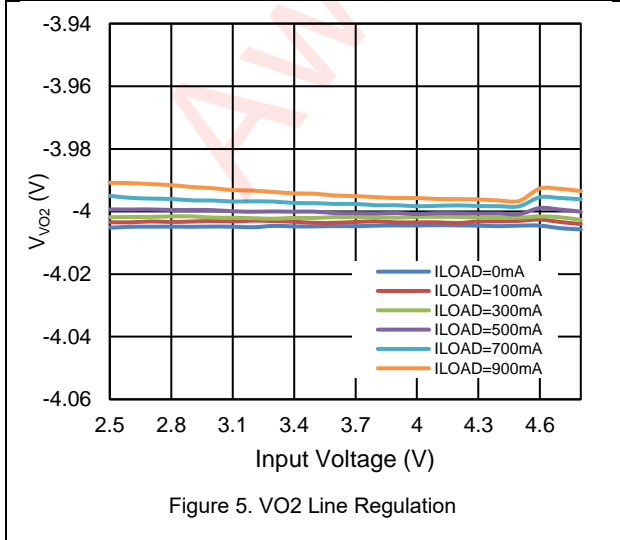
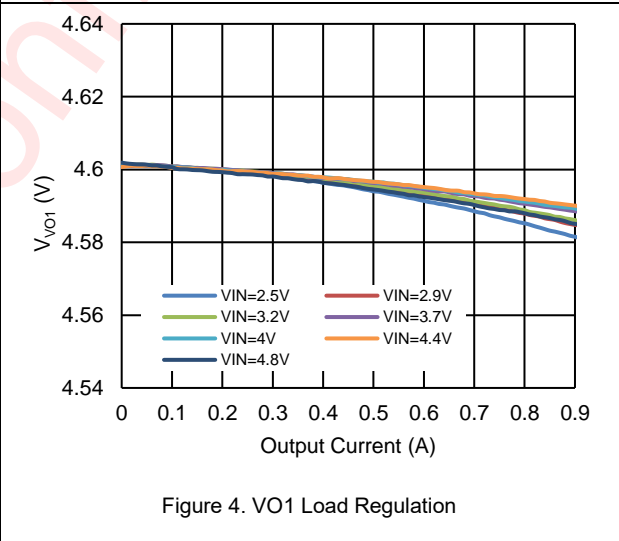
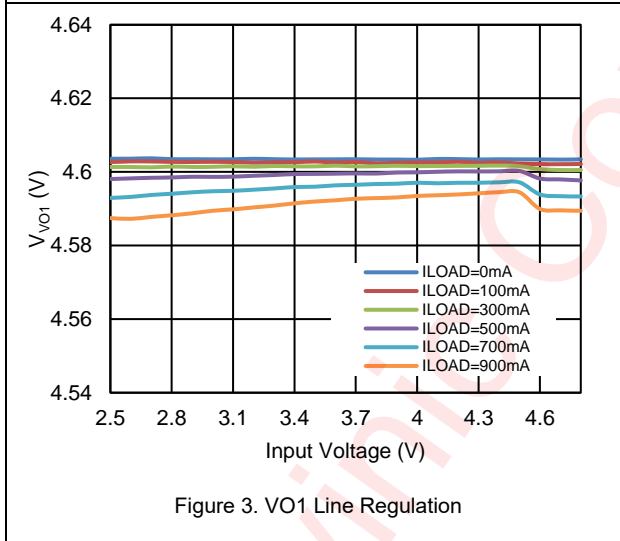
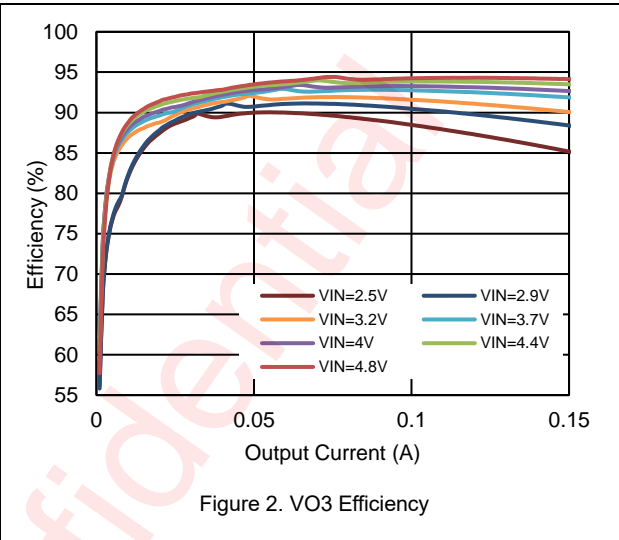
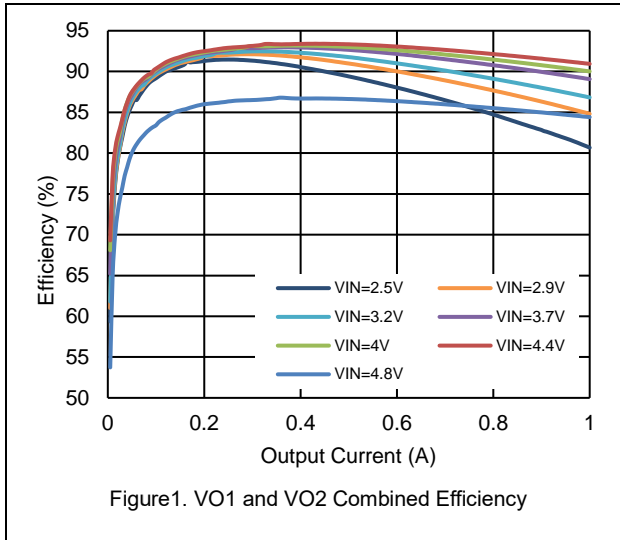
L3: DFE252012F-100M=P2 1.4A, 480mΩ, 252012

Test Condition: Ambient temperature is 60°C, the load current is only between the VO1 and VO2, VO3 is no load, AWP37579CSR works stably in laboratory test environment.

NOTE6: Guaranteed by design characterization and correlation with process controls. Not fully test in production.

## TYPICAL CHARACTERISTICS

AVIN = PVIN = VIN = 3.7V, VVO1= 4.6V, VVO2= -4V, VVO3= 7.6V, L1= 2.2μH, L2= 1.0μH, L3= 4.7μH. Typical values are at TA = TJ = 25°C (unless otherwise noted)



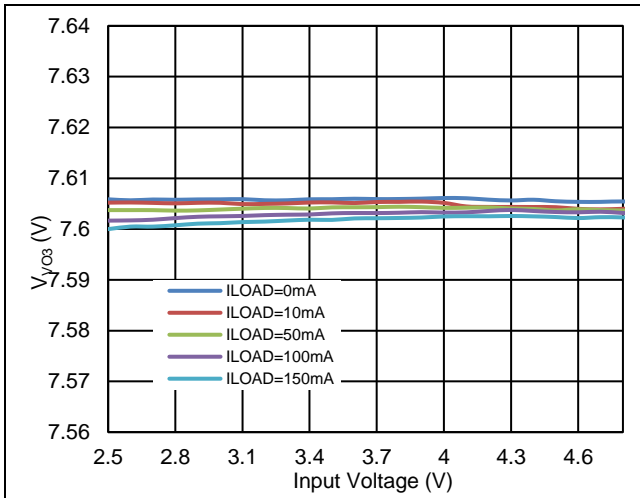


Figure 7. VO3 Line Regulation

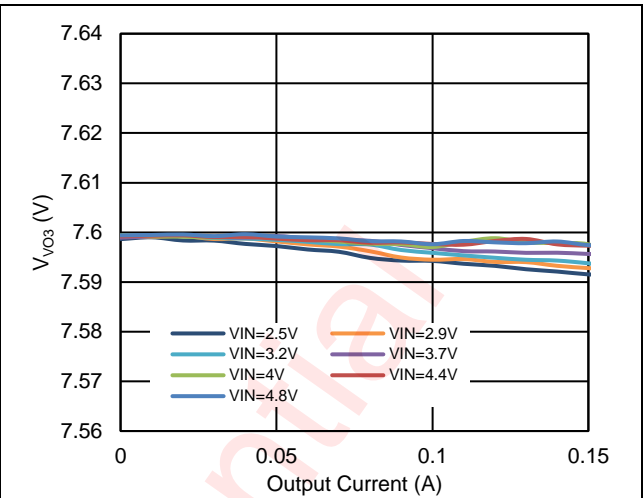


Figure 8. VO3 Load Regulation

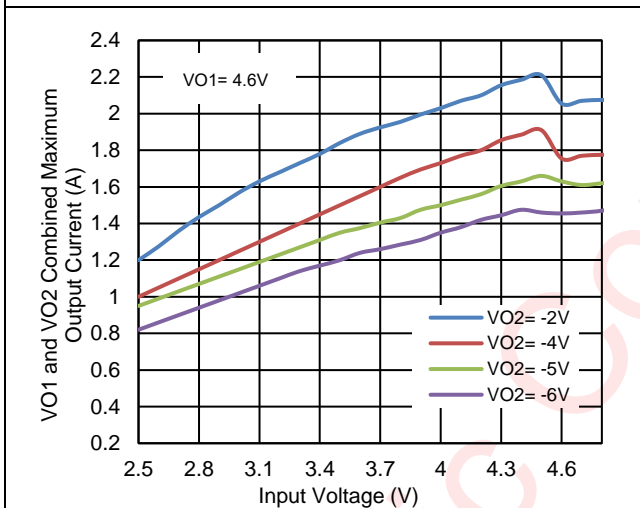


Figure 9. VO1 and VO2 Combined Maximum Output Current (NOTE 5)

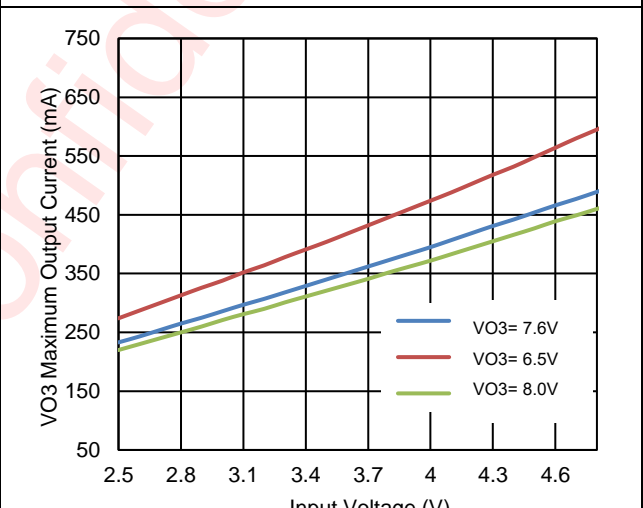


Figure 10. VO3 Maximum Output Current (NOTE 5)

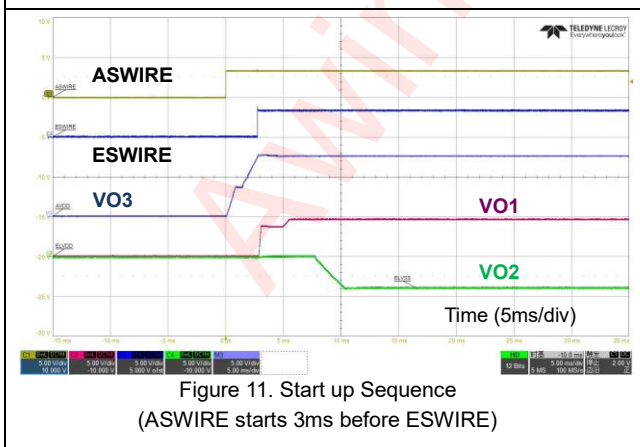


Figure 11. Start up Sequence (ASWIRE starts 3ms before ESWIRE)

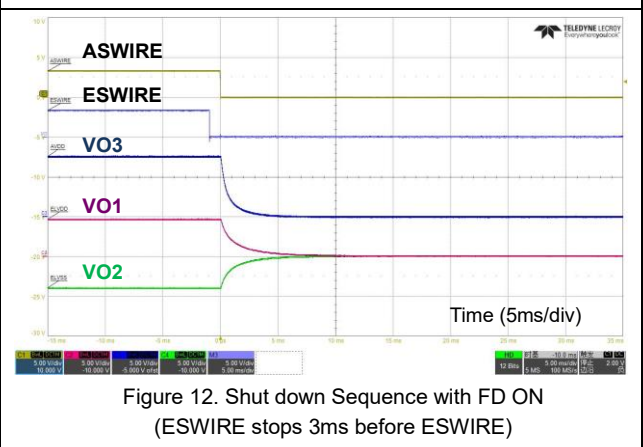


Figure 12. Shut down Sequence with FD ON (ESWIRE stops 3ms before ASWIRE)

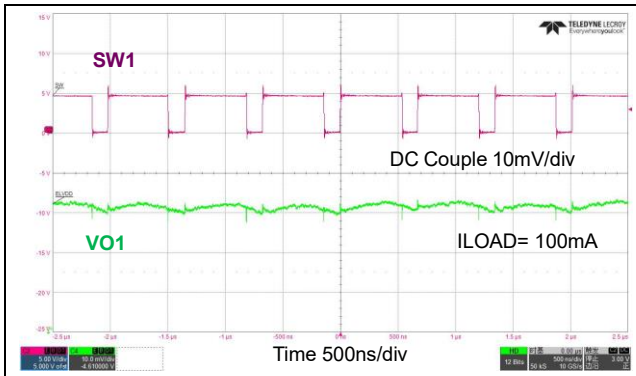


Figure 13. VO1 Switching and Output Waveforms at light load



Figure 14. VO1 Switching and Output Waveforms at heavy load

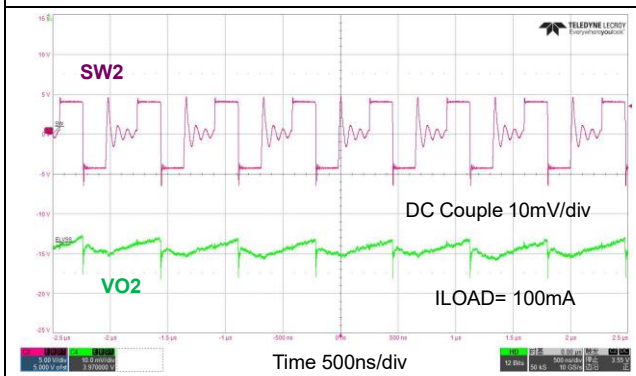


Figure 15. VO2 Switching and Output Waveforms at light load



Figure 16. VO2 Switching and Output Waveforms at heavy load

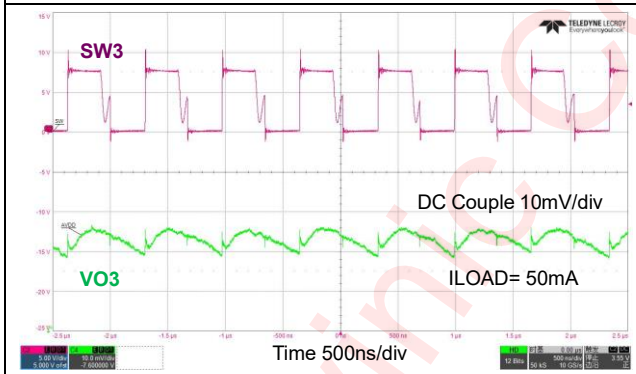


Figure 17. VO3 Switching and Output Waveforms at light load

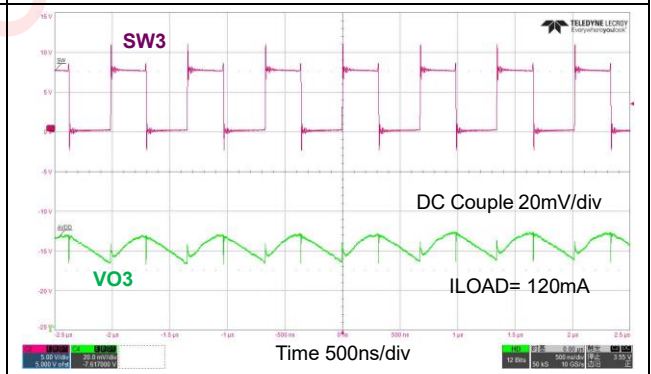


Figure 18. VO3 Switching and Output Waveforms at heavy load

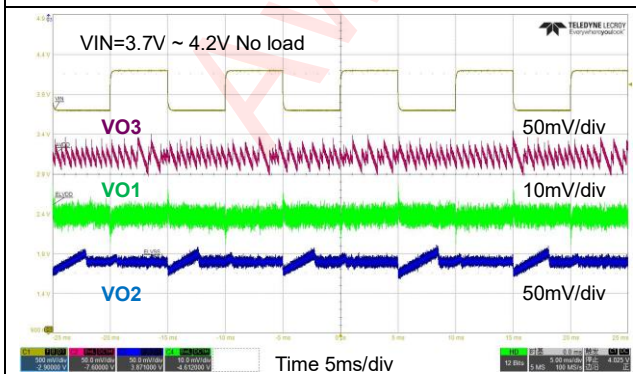


Figure 19. Line transient at No load

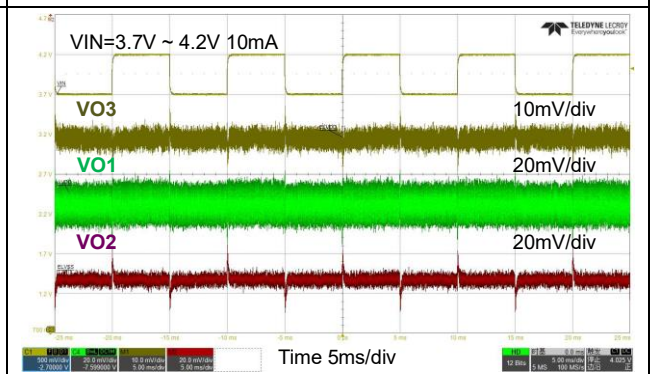


Figure 20. Line transient at light load (10mA)

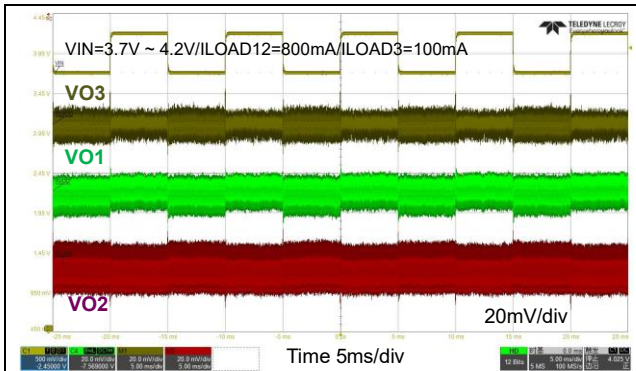


Figure 21. Line transient at heavy load



Figure 22. VO1 load transient (10~500mA/SR=0.1A/μs)

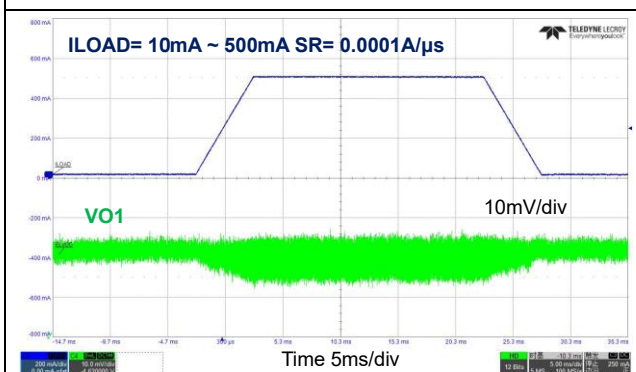


Figure 23. VO1 load transient (10~500mA/SR=0.0001A/μs)

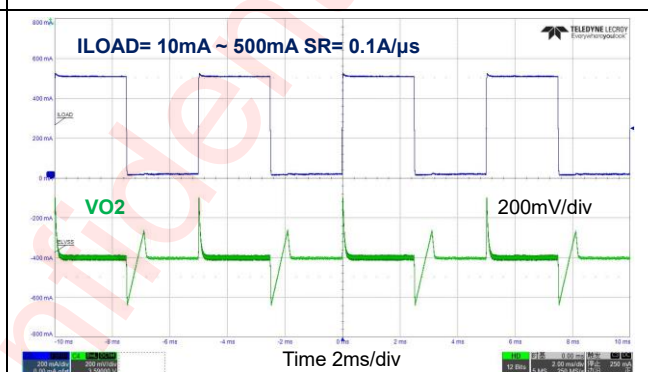


Figure 24. VO2 load transient (10~500mA/SR=0.1A/μs)

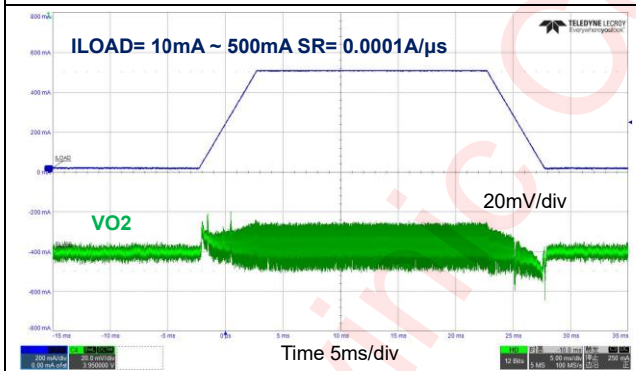


Figure 25. VO2 load transient (10~500mA/SR=0.0001A/μs)

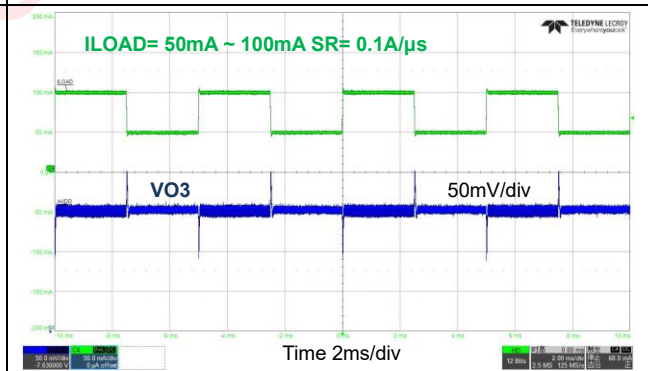


Figure 26. VO3 load transient (50~100mA/SR=0.1A/μs)

## DETAILED FUNCTIONAL DESCRIPTION

### Sequence

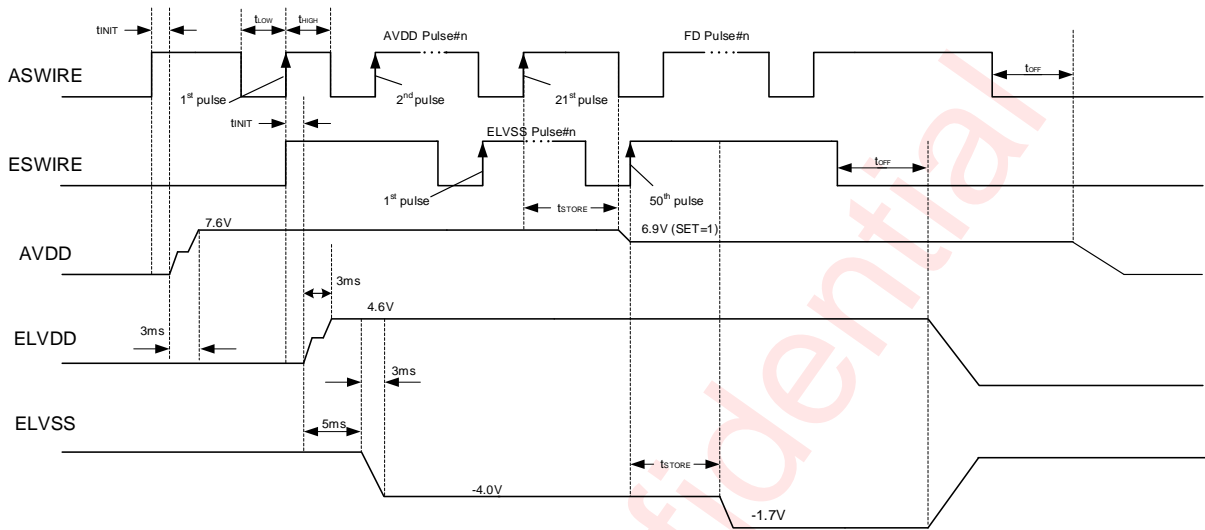


Figure 27. Timing diagram

The AVDD boost converter operates with a cycle-by-cycle peak current limit topology and fixed 1.45MHz frequency. The AVDD output voltage can be programmed through ASWIRE interface, and the output voltage table can be changed by the condition of SET interface. When SET = LOW, AVDD is available from 6.5V to 8.0V with 100mV steps, while SET = HIGH, AVDD is available from 6.5V to 8.0V with 50mV steps. The programming table of AVDD output voltage is shown in Table 1.

The AVDD boost converter begins soft-start to its default voltage 7.6V with a  $t_{INIT}$  time delay after the ASWIRE logic level goes high. The soft-start lasts for 3ms typically.

The AVDD output voltage is programmable by applying different pulses to ASWIRE interface, which counts the rise edges, plus a high logic level to ASWIRE lasts longer than a  $t_{STORE}$  time is detected after control pulses stop, AVDD starts altering to the target voltage. The AVDD boost converter turns off with a  $t_{OFF}$  time delay after the logic level of ASWIRE interface goes from high to low.

Table 1 Programming of AVDD output voltage

SET=0		SET=1	
ASWIRE Pulse	AVDD	ASWIRE Pulse	AVDD
0	7.6V	0	7.60V
1	7.8V	1	7.90V
2	7.7V	2	7.85V
3	7.6V	3	7.80V
4	7.5V	4	7.75V
5	7.4V	5	7.70V
6	7.3V	6	7.65V

SET=0		SET=1	
ASWIRE Pulse	AVDD	ASWIRE Pulse	AVDD
7	7.2V	7	<b>7.60V</b>
8	7.1V	8	7.55V
21	7.0V	9	7.50V
22	6.9V	10	7.45V
23	6.8V	11	7.40V
24	6.7V	12	7.35V
25	6.6V	13	7.30V
26	6.5V	14	7.25V
37	8.0V	15	7.20V
38	7.9V	16	7.15V
		17	7.10V
		18	7.05V
		19	7.00V
		20	6.95V
		21	6.90V
		40	6.85V
		41	6.80V
		42	6.75V
		43	6.70V
		44	6.65V
		45	6.60V
		46	6.55V
		47	6.50V
		68	8.00V
		69	7.95V

The inverting buck-boost and boost converters both operate with a cycle-by-cycle peak current limit topology and fixed 1.45MHz frequency. The ELVSS output voltage can be programmed from -6.6V to -0.5V with 100mV steps. The programming table of ELVSS output voltage is shown in Table 2. The ELVDD output voltage can be programmed from 4.6V to 5.0V with 100mV steps by ESWIRE interface as well. The programming table of ELVDD output voltage is shown in Table 3.

The ESWIRE interface controls the on and off state of ELVDD and ELVSS. The ELVDD boost converter begins soft-start to its default voltage 4.6V with a  $t_{INIT}$  time delay after the ESWIRE logic level goes high. The ELVSS buck-boost converter with -4V default value starts to operate 5ms later than the ELVDD boost converter. Both

converters are implemented with a 3ms soft-start to limit the inrush current. When ESWIRE interface goes low for  $t_{OFF}$  time, the ELVDD and ELVSS converters stop operation simultaneously.

The ELVDD and ELVSS output voltage both are programmable by applying different pulses to ESWIRE interface, which also counts the rise edges, plus a high logic level of ESWIRE lasts longer than a  $t_{STORE}$  time is detected after controll pulses stop, the ELVDD and ELVSS outputs start altering to the target voltage.

**Table 2 Programming of ELVSS output voltage**

ESWIRE Pulse	ELVSS	ESWIRE Pulse	ELVSS
0	-4.0V	31	-3.6V
1	-6.6V	32	-3.5V
2	-6.5V	33	-3.4V
3	-6.4V	34	-3.3V
4	-6.3V	35	-3.2V
5	-6.2V	36	-3.1V
6	-6.1V	37	-3.0V
7	-6.0V	38	-2.9V
8	-5.9V	39	-2.8V
9	-5.8V	40	-2.7V
10	-5.7V	41	-2.6V
11	-5.6V	42	-2.5V
12	-5.5V	43	-2.4V
13	-5.4V	44	-2.3V
14	-5.3V	45	-2.2V
15	-5.2V	46	-2.1V
16	-5.1V	47	-2.0V
17	-5.0V	48	-1.9V
18	-4.9V	49	-1.8V
19	-4.8V	50	-1.7V
20	-4.7V	51	-1.6V
21	-4.6V	52	-1.5V
22	-4.5V	53	-1.4V
23	-4.4V	54	-1.3V
24	-4.3V	55	-1.2V
25	-4.2V	56	-1.1V
26	-4.1V	57	-1.0V

ESWIRE Pulse	ELVSS	ESWIRE Pulse	ELVSS
27	-4.0V	58	-0.9V
28	-3.9V	59	-0.8V
29	-3.8V	60	-0.7V
30	-3.7V	61	-0.6V
		62	-0.5V

Table 3 Programming of ELVDD output voltage

ESWIRE Pulse	ELVDD
0/no pulse	4.6V
71	4.6V
76	5.0V
77	4.9V
78	4.8V
79	4.7V

## ELVSS Transition

AWP37579CSR also has the slew rate control during the transition of the ELVSS output voltage, which aims to accomplish smooth voltage changes. The ramp time is 100 $\mu$ s typically, step is 100mV (Actually ramp step is 12.5 mV/12.5  $\mu$ s). The wider the transition range of the ELVSS output voltage, the longer the transition time.

Therefore, AWP37579CSR supports the ELVSS output voltage transition in fine steps. The configuration for finer steps via the pulse numbers of ESWIRE interface, which is shown in Table 4. Firstly configuring the ELVSS transition fine steps basing on Table 4, Secondly configuring the initial voltage according to Table 2.

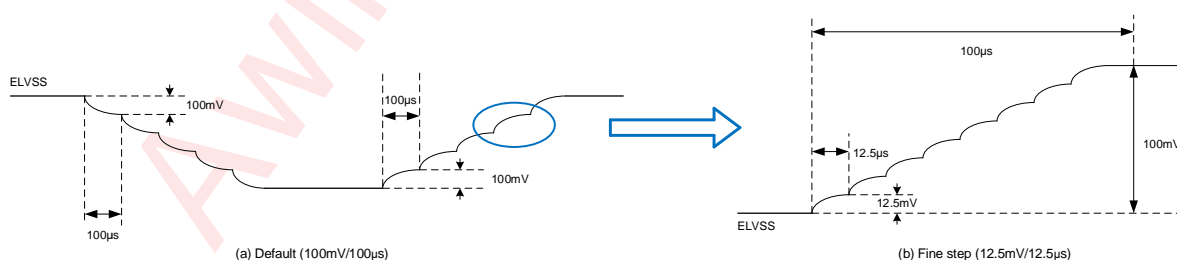


Figure 28. The output voltage of ELVSS transition time

Table 4 Programming of the ELVSS Transition steps

ESWIRE Pulse	Fine Steps
63	0 (Default)

ESWIRE Pulse	Fine Steps
64	12.5mV plus
65	25mV plus
66	37.5mV plus
67	50mV plus
68	62.5mV plus
69	75mV plus
70	87.5mV plus

### Maximum Output Current Capacity

AWP37579CSR operates with an input voltage range of 2.5V to 4.8V. However, due to different input and output voltage, the maximum output current capacity is quite different, and also affected by peripheral inductors and capacitors, additional input capacitors are recommended for lower input supply voltage.

The maximum output current in  $T_A = 60^\circ\text{C}$  for different  $V_{IN}$  and  $V_{O2}$  voltages is shown in Table 5.

Table 5 The maximum output current

$V_{IN}$ (V)	The maximum output current (A)				
	$V_{V02} = -2V$	$V_{V02} = -4V$	$V_{V02} = -5V$	$V_{V02} = -5.5V$	$V_{V02} = -6V$
2.5	1.2	1	0.95	0.9	0.82
2.6	1.275	1.05	0.99	0.95	0.86
2.7	1.36	1.1	1.03	1	0.9
2.8	1.435	1.15	1.07	1.04	0.94
2.9	1.5	1.2	1.11	1.08	0.98
3	1.57	1.25	1.15	1.12	1.02
3.1	1.63	1.3	1.19	1.16	1.06
3.2	1.68	1.35	1.23	1.2	1.1
3.3	1.73	1.4	1.27	1.24	1.14
3.4	1.78	1.45	1.31	1.28	1.17

### EMI Description

AWP37579CSR can configured the SW edge rate by applying different pulses to ESWIRE interface, the default is fastest, the pulse numbers are shown in Table 6. Slower SW edge rate can optimize RF interference, at the

same time the efficiency will be decreased. If the SW edge rate configuration is required, it is recommended to send ESWIRE pulse after the soft-start completion of the output voltage of ELVDD and ELVSS.

**Table 6 Programming of SW edge rate**

ESWIRE Pulse	SW edge rate
0/no pulse	fastest
86	slow
87	fast
88	faster
89	fastest

### Under Voltage Lock-Out

Under Voltage Lock-Out (UVLO) is implemented to detect the input voltage AVIN. Once AVIN drops below UVLO falling threshold, all of the three converters (AVDD, ELVDD and ELVSS) stop switching; If AVIN increases above UVLO rising threshold, the three converters restart switching and resume to their previous settings.

### Start-up Short Detection (SSD)

The start-up short detection block detects the ELVSS output voltage to monitor whether ELVSS and ELVDD are short connected. If the ELVSS output voltage is pulled up to 0.2V in 5ms after ESWIRE interface goes high, SSD function is triggered and the ELVDD and ELVSS converters shut down immediately, FD function is on at the same time. Resetting the power supply or pulling the ESWIRE interface low for more than a  $t_{OFF}$  time can restart the device.

SSD function is enabled and disabled by the pulse numbers of ASWIRE interface. Number of controll pulse is set differently depending on the logic condition of SET interface. SSD function is off by default, the pulse numbers are shown in Table 7.

**Table 7 ASWIRE pulses for SSD function**

SET=0		SET=1	
ASWIRE Pulse	SSD	ASWIRE Pulse	SSD
0/no pulse	OFF	0/no pulse	OFF
9	OFF	22	OFF
10	ON	23	ON

### Fast discharge (FD)

The output voltage (AVDD, ELVDD and ELVSS) fast discharge function is enabled and disabled by the pulse numbers of ASWIRE interface. Number of controll pulse is set differently depending on the logic condition of SET interface. The pulse numbers are shown in Table 8, FD function is off by default.

When FD function is active, ASWIRE and ESWIRE both stop, all outputs of the device are always discharged to GND until ASWIRE and ESWIRE start again.

**Table 8 ASWIRE pulses for FD function**

SET=0		SET=1	
ASWIRE Pulse	FD	ASWIRE Pulse	FD
0/no pulse	OFF	0/no pulse	OFF
11	ON	25	ON
12	OFF	26	OFF

### Short Circuit Protection (SCP)

The short circuit protection block monitors the output voltages of the AVDD, ELVDD and ELVSS converters to protect the device of short connections to ground or overload. When a SCP or overload event occurs, all the three converters shut down and FD function is enabled simultaneously. Only resetting the power supply or both pulling the ASWIRE and ESWIRE interface to low at the same time for more than a  $t_{OFF}$  time can restart the device.

An SCP or overload event occurs in the following cases:

- (1) After the output voltages of all the three converters are properly established, ELVDD output voltage falls below 90% of the target voltage and lasts for 1ms; ELVSS and AVDD output voltage falls below 80% of the target voltage and lasts for 1ms;
- (2) In soft-start process,  $V_{ELVDD}$ ,  $V_{ELVSS}$  and  $V_{AVDD}$  are not in regulation 4ms when ELVDD and ELVSS output voltages begin to establish;

### Thermal Shut-Down (TSD)

The Thermal Shut-Down (TSD) function protects the device when overheating occurs. If the IC's junction temperature exceeds 165°C, three converters stop operation. It can not exit this state automatically. Pulling the SWIRE interface to low for more than a  $t_{OFF}$  time or a power-cycle on the input supply restarts the device with the default values.

### Device Reset

- (1) Power resetting resets the device to default settings;
- (2) Pulling ASWIRE interface low for  $t_{OFF}$  then the output voltage of AVDD is reset to default value of 7.6V;
- (3) Pulling ESWIRE interface low for  $t_{OFF}$  then the output voltage of ELVDD and ELVSS are reset to default value of 4.6V and -4V.

## PCB LAYOUT CONSIDERATION

It is recommended to follow the below PCB layout guidelines:

- 1) A common ground plane between AGND and PGND to minimize ground shifts is recommended.
- 2) Put inductors as close as possible to the device, creating forbidden area under inductors for each PCB layer. Traces of switching nodes (LX1, LX2 and LX3) should be short and wide.
- 3) Place input capacitors on PVIN and output capacitors on outputs as close as possible to the device.
- 4) If vias are used for power paths, multiple vias are necessary to obtain lower equivalent resistance on power paths and facilitate heat dissipation.

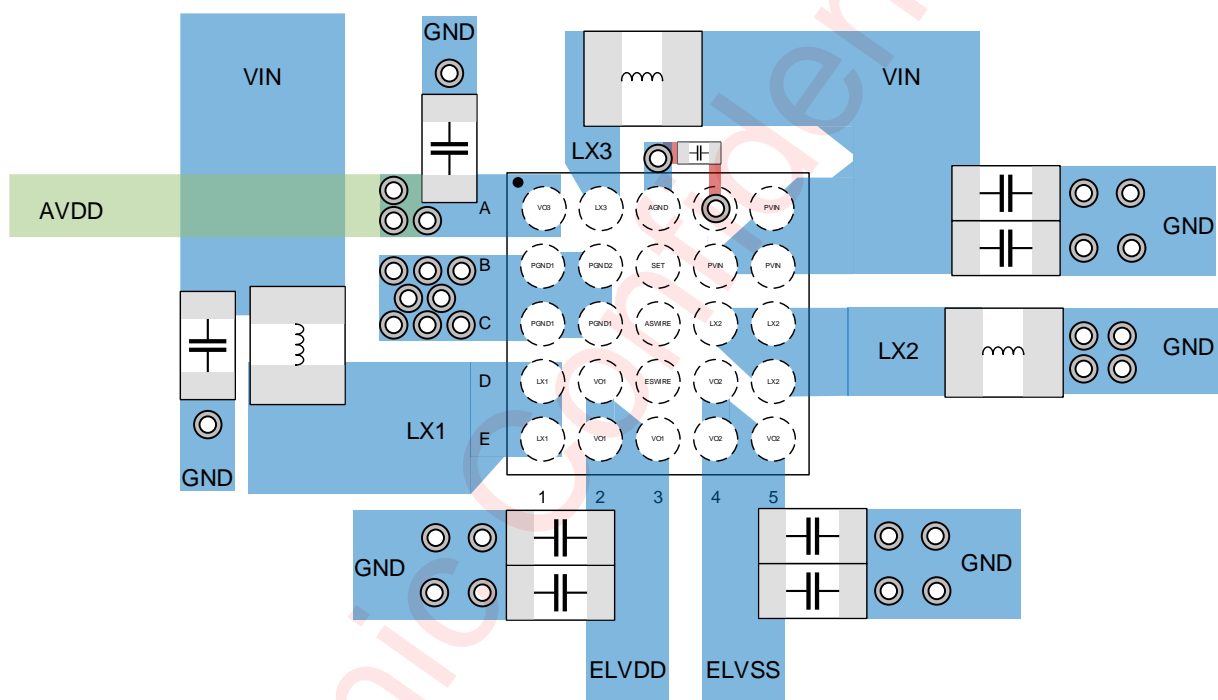
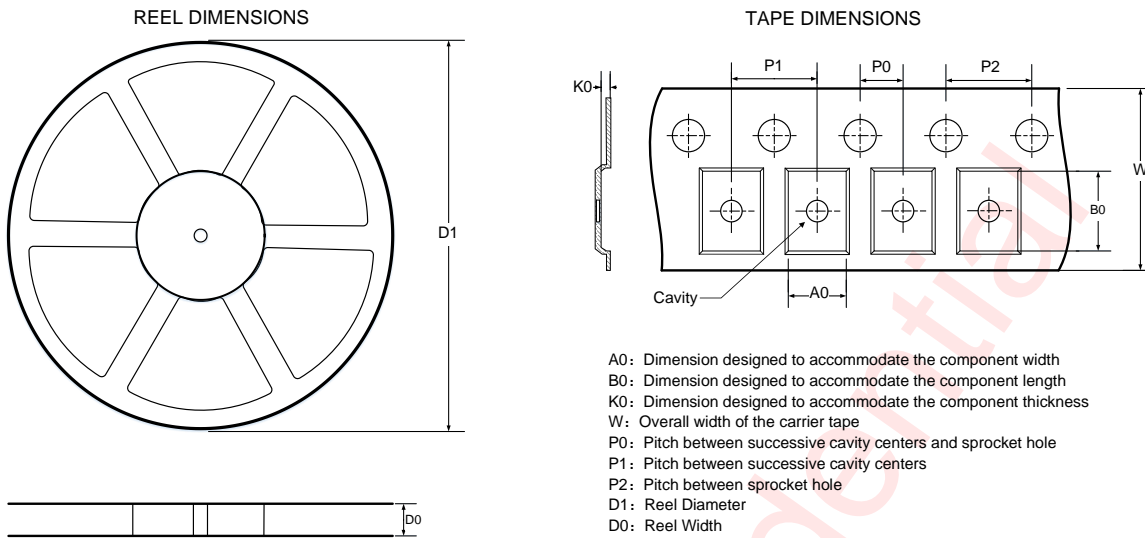
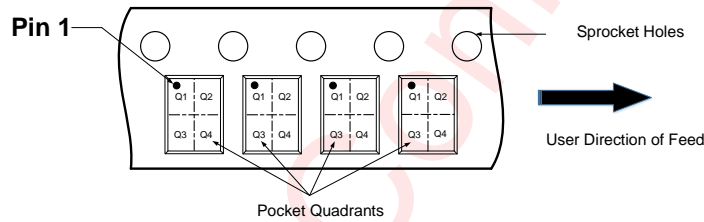


Figure 29. AWP37579 PCB Layout example

## TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



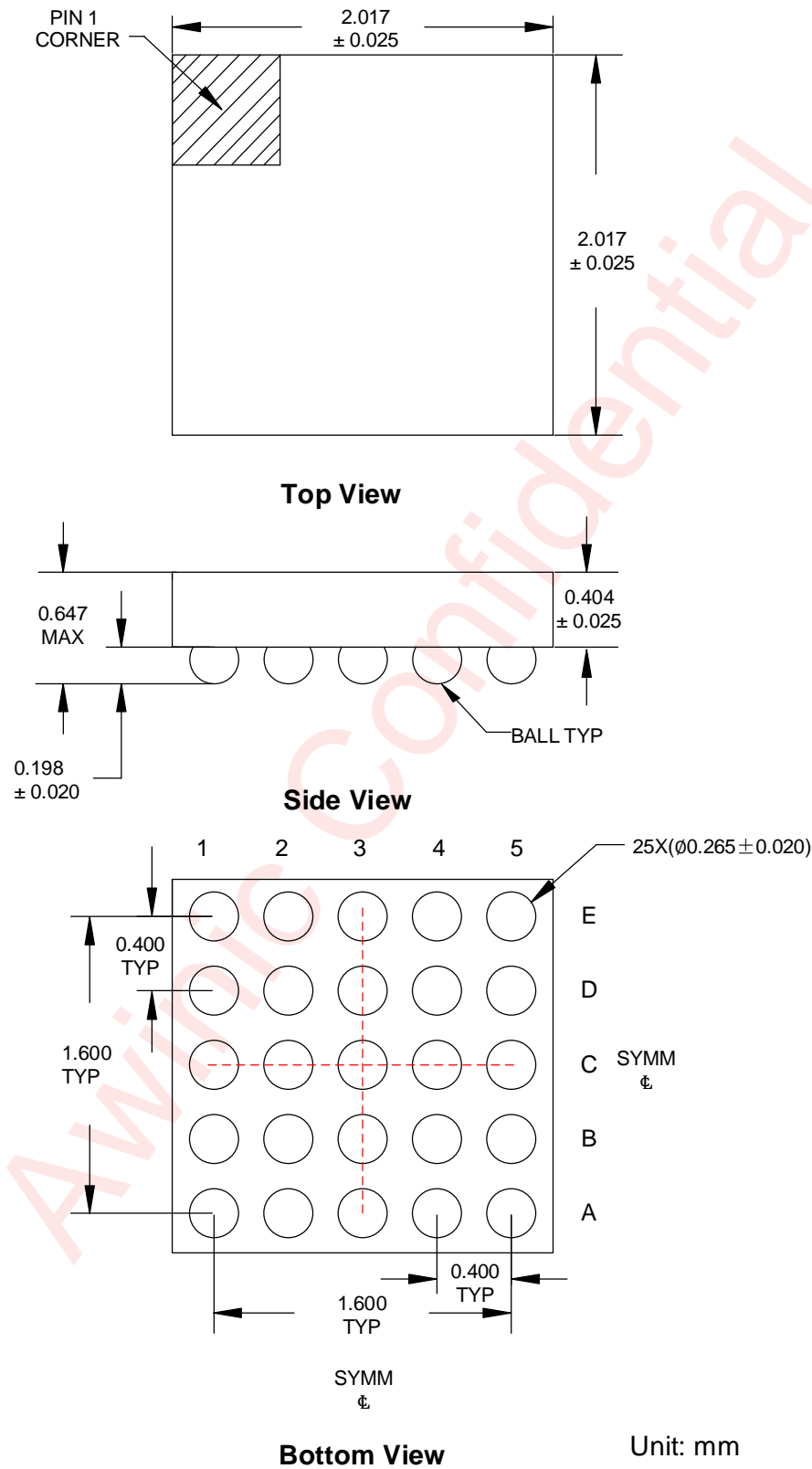
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

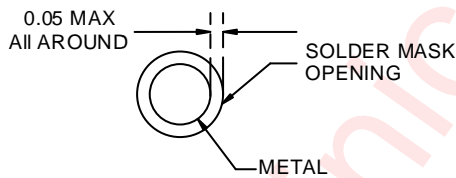
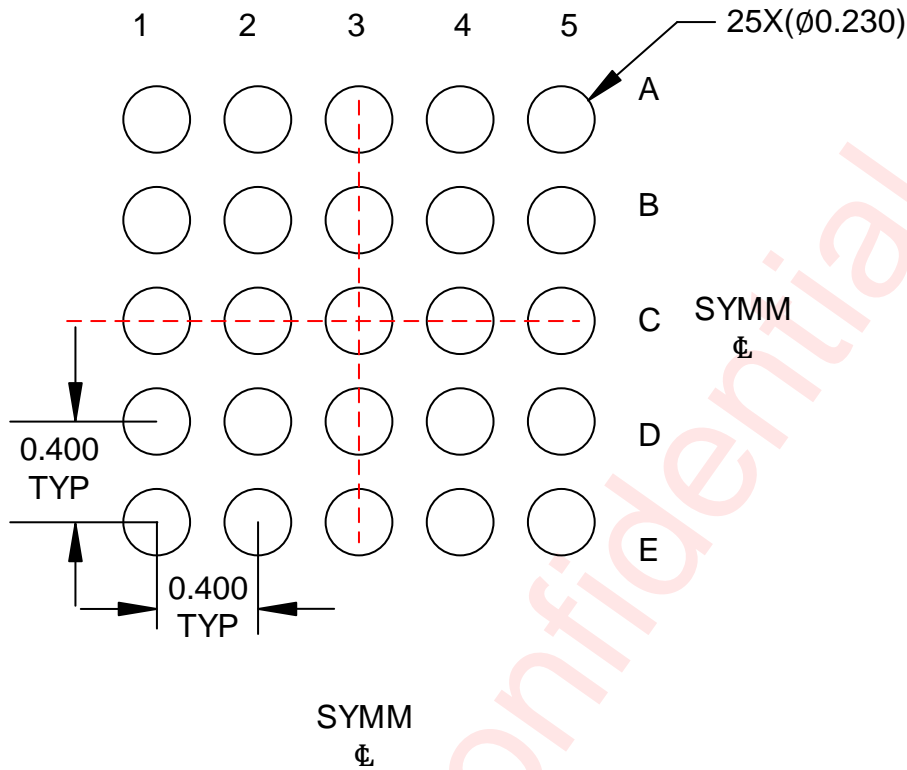
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	2.25	2.25	0.70	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

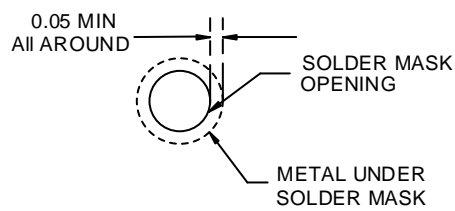
PACKAGE DESCRIPTION



LAND PATTERN DATA



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

**REVISION HISTORY**

Version	Date	Change Record
V1.0	Oct. 2025	Officially released

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