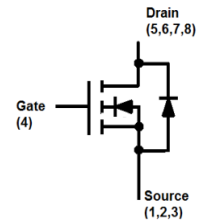
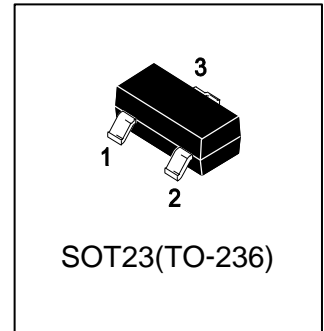


# LN2302ALT1G,S-LN2302ALT1G

20V N-Channel Enhancement-Mode MOSFET

## 1. FEATURES

- $R_{DS(ON)} \leq 85m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 115m\Omega @ V_{GS}=2.5V$
- $R_{DS(ON)} \leq 135m\Omega @ V_{GS}=1.8V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



## 2. APPLICATIONS

- Power Management in Notebook
- Portable Equipment
- Load Switch
- DSC

## 3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2302ALT1G S-LN2302ALT1G	02A	3000/Tape&Reel
LN2302ALT3G S-LN2302ALT3G	02A	10000/Tape&Reel

## 4. MAXIMUM RATINGS( $T_a = 25^\circ C$ )

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDSS	20	V
Gate-to-Source Voltage	VGS	$\pm 8$	V
Continuous Drain Current	ID	Ta=25°C	2.8
		Ta=70°C	2.2
Pulsed Drain Current (Note 2)	IDM	10	A
Power Dissipation	PD	Ta=25°C	1.25
		Ta=70°C	0.8
Junction and Storage Temperature Range	Tj,Tstg	-55~+150	°C

## 5. THERMAL CHARACTERISTICS

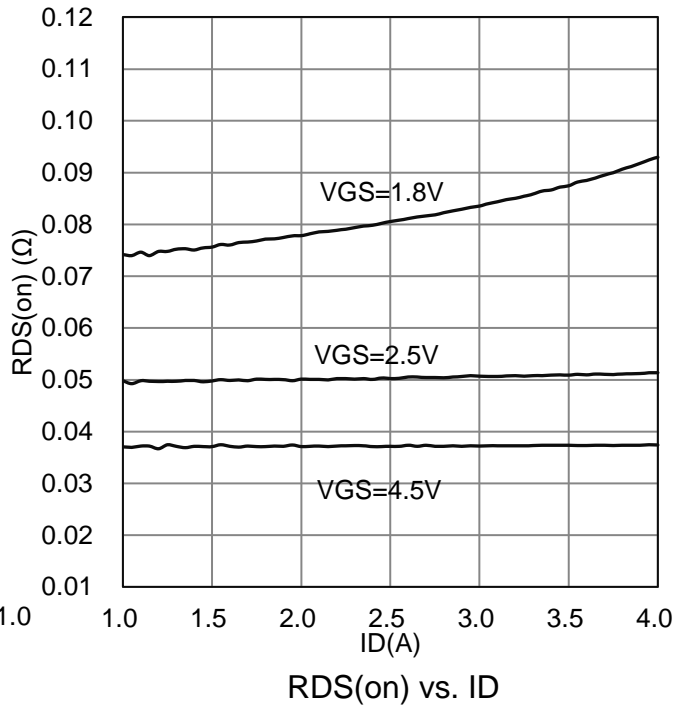
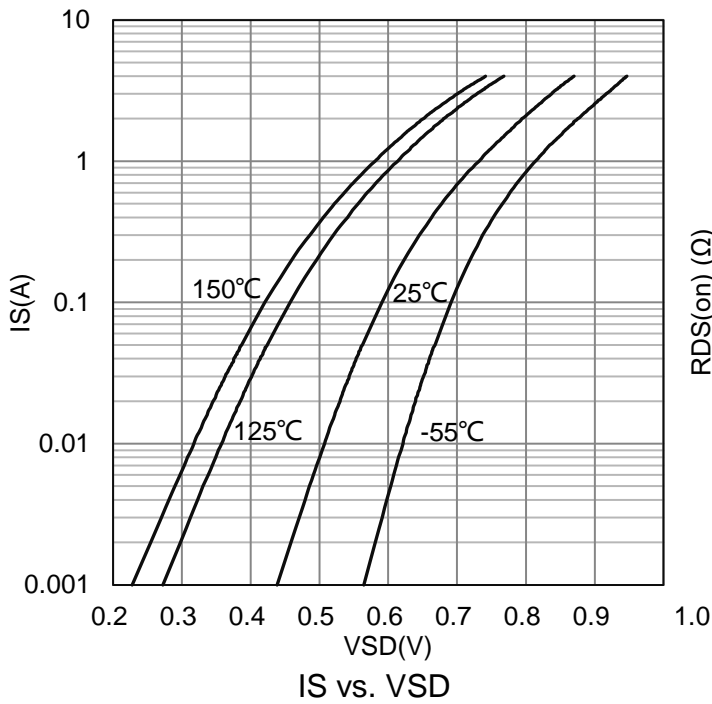
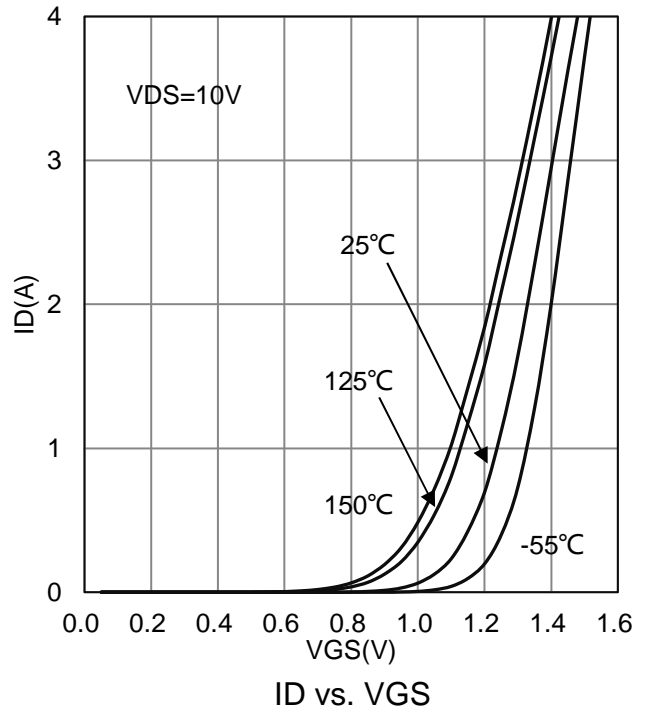
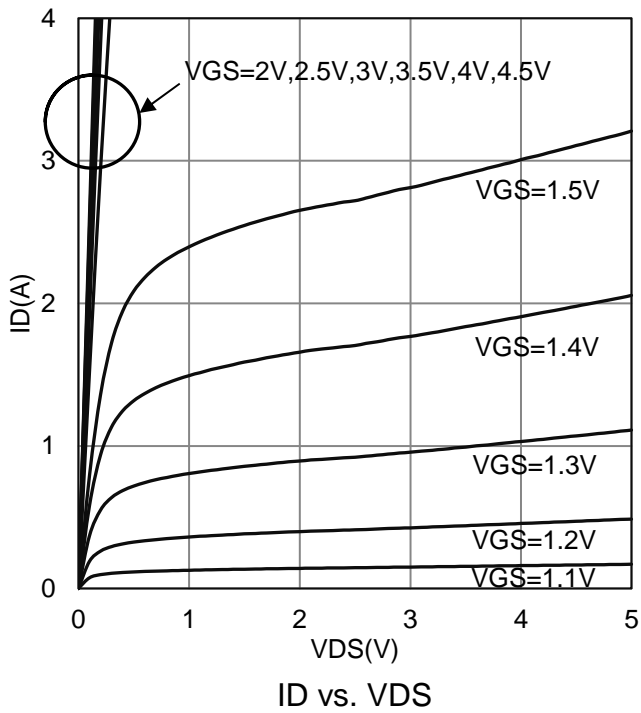
Parameter		Symbol	Limits	Unit
Thermal Resistance, Junction-to-Ambient (Note 1)	$t \leq 10$ s	R $\theta$ JA	77	$^{\circ}\text{C}/\text{W}$
	Steady State		105	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case		R $\theta$ JC	70	$^{\circ}\text{C}/\text{W}$

1. Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.
2. Pulse width limited by maximum junction temperature

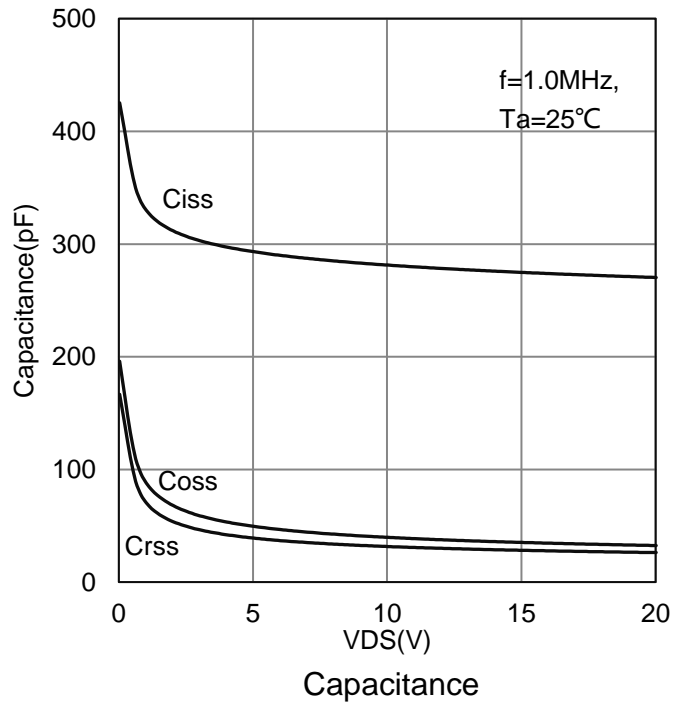
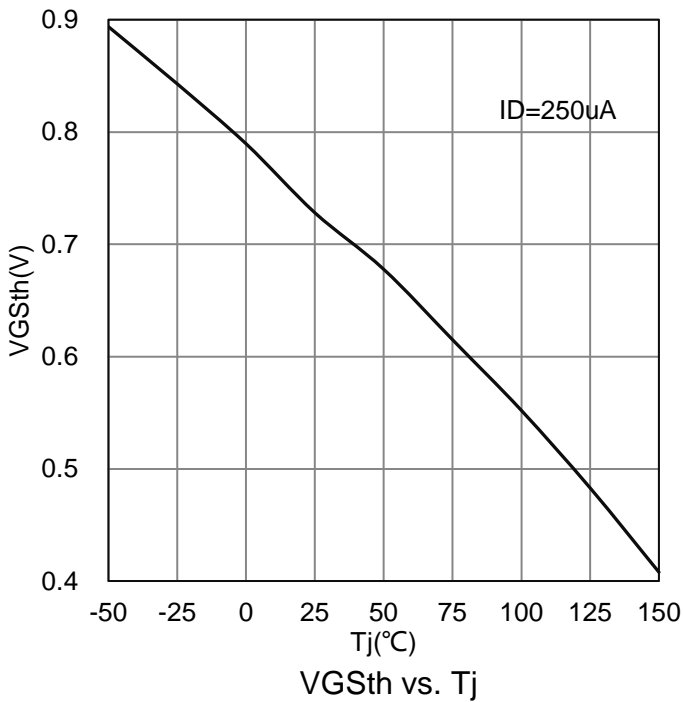
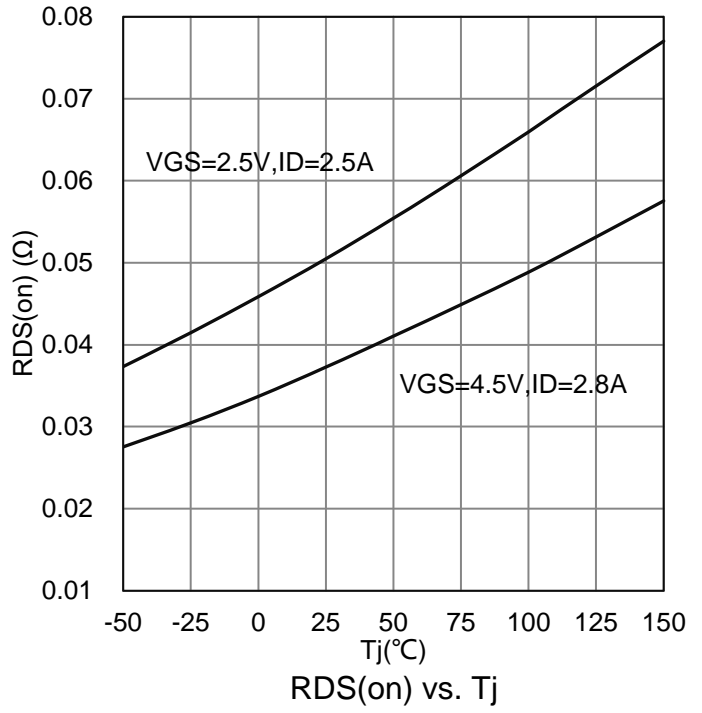
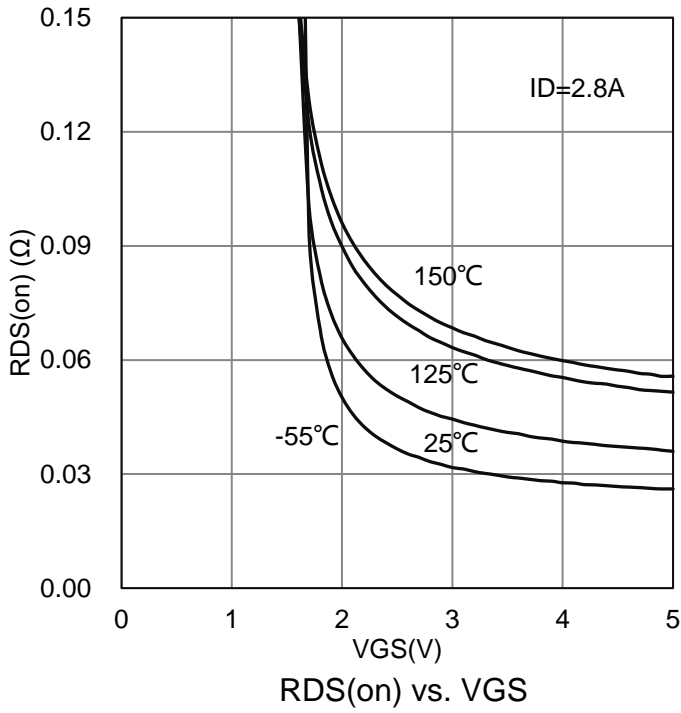
## 6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
<b>STATIC PARAMETERS</b>						
Drain-Source Breakdown Voltage (VGS = 0, ID = 250 $\mu$ A)	VBRDSS	20	-	-	V	
Zero Gate Voltage Drain Current (VGS = 0, VDS = 20 V) (VGS = 0, VDS = 20 V, TJ = 55 $^{\circ}$ C)	IDSS	-	-	1 10	$\mu$ A	
Gate Leakage Current (VDS = 0V, VGS = $\pm$ 8V)	IGSS	-	-	$\pm$ 100	nA	
Gate Threshold Voltage (VDS = VGS, ID = 250 $\mu$ A)	VGS(th)	0.6	0.9	1.2	V	
Static Drain-Source On-State Resistance (VGS = 4.5V, ID = 2.8A) (VGS = 2.5V, ID = 2.5A) (VGS = 1.8V, ID = 2.2A)	RDS(on)	-	55 65 80	85 115 130	m $\Omega$	
<b>Dynamic</b>						
Input Capacitance (VGS = 0 V, f = 1.0MHz, VDS = 10 V)	Ciss	-	281	-	pF	
Output Capacitance (VGS = 0 V, f = 1.0MHz, VDS = 10 V)	Coss	-	40	-		
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz, VDS = 10 V)	Crss	-	32	-		
Total Gate Charge	(VDS = 10V, VGS = 4.5V, ID = 2.8A)	Qg	-	2.9	-	nC
Gate-Source Charge		Qgs	-	0.6	-	
Gate-Drain Charge		Qgd	-	0.8	-	
Turn-On Delay Time	(VDD = 10V, RL = 10 $\Omega$ , VGEN = 4.5V, RG = 6 $\Omega$ )	td(on)	-	9	-	ns
Rise Time		tr	-	23	-	
Turn-Off Delay Time		td(off)	-	38	-	
Fall Time		tf	-	3	-	
Forward Voltage (VGS = 0 V, IS = 1A)	VSD	-	0.75	1.2	V	

**7. ELECTRICAL CHARACTERISTICS CURVES**



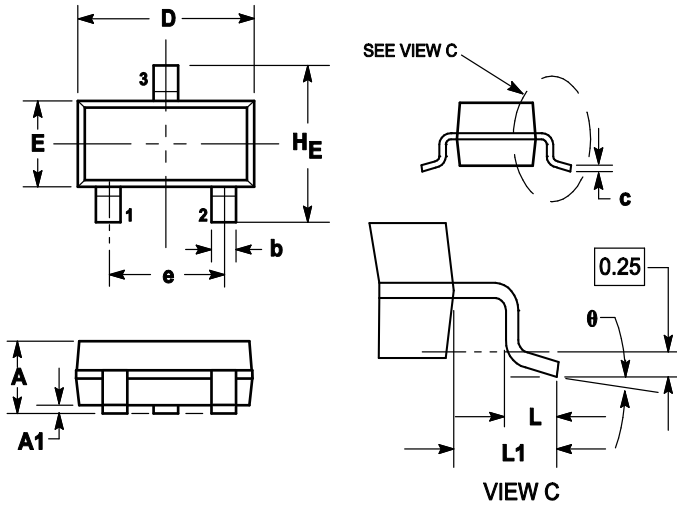
**7. ELECTRICAL CHARACTERISTICS CURVES(Con.)**



### 8. OUTLINE AND DIMENSIONS

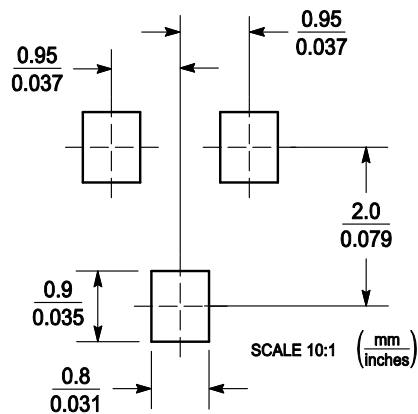
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

### 9. SOLDERING FOOTPRINT



## **DISCLAIMER**

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