

I²S Input, High Efficiency, 6V Charge Pump, Digital Smart K Audio Amplifier

FEATURES

- **Adaptive Charge Pump with total efficiency up to 86%**
- **Supports Speaker, Receiver 2-in-1 application**
- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 15 μ V**
- **THD+N: 0.02%**
- Extensive Pop-Click Suppression
- Volume control(from -96dB to 0dB)
- I²S interface:
 - I²S, Left-Justified and Right-Justified
 - Input Sample Rates from 8kHz to 96kHz
 - Data Width: 16, 20, 24, 32 Bits
- I²C-bus control interface(400kHz)
- Power Supplies:
 - VDD: 3.0V~5.5V
 - DVDD: 1.65V~1.95V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- FCQFN 2X3-20L Package

APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

DESCRIPTION

The AW8838 is an I²S input, high efficiency digital Smart K audio amplifier with an integrated 6V adaptive charge pump, sound quality enhancement algorithms and speaker protection. Due to its 15 μ V noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 1.8W (RMS, THD+N = 1%) output power into an 8 Ω speaker at a battery voltage of 4.2V.

The AW8838 integrates a high-efficiency adaptive charge pump as the Class-D amplifier supply rail. The output voltage of charge pump is only raised when necessary. This improves the output dynamic range of audio signal while limiting quiescent power consumption.

The AW8838 features AWINIC proprietary AGC algorithm that prevents clipping noise and improves sound quality.

The AW8838 supports speaker and receiver 2-in-1 applications. In the receiver application, it connects VDD directly to the Class-D amplifier power supply.

The AW8838 features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I²C-bus interface, and the device address is configurable.

The AW8838 offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

AW8838 is available in FCQFN 2X3-20L package.

PIN CONFIGURATION AND TOP MARK

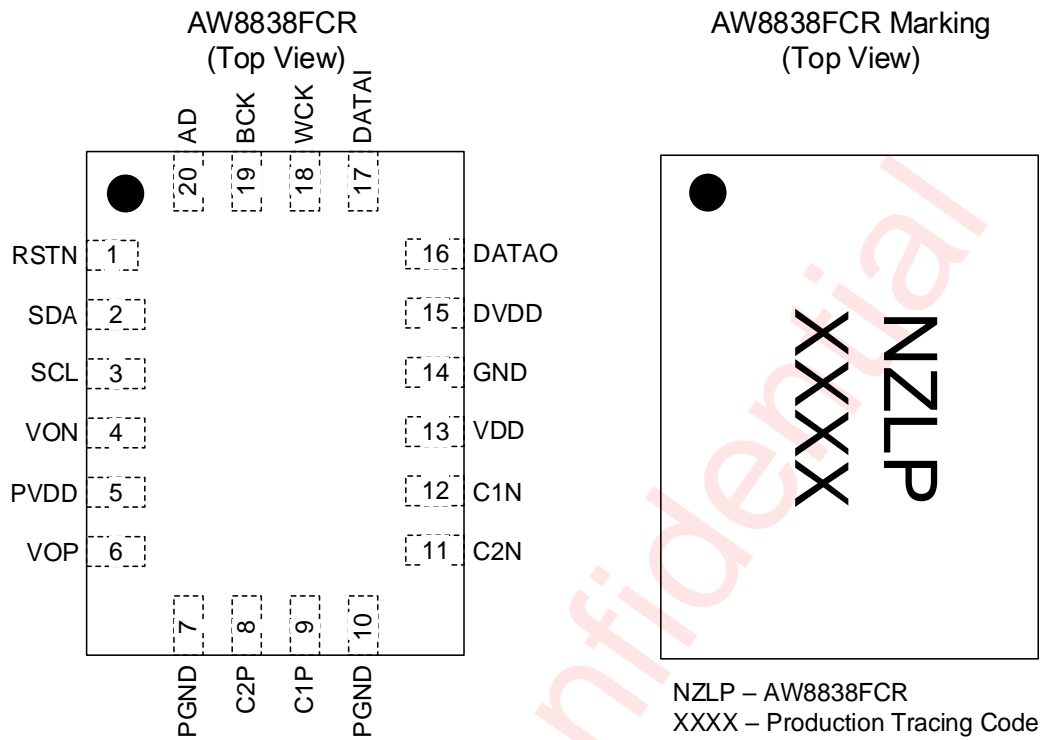


Figure 1 AW8838FCR Pin Diagram Top View and Device Marking

PIN DEFINITION

| No. | NAME | DESCRIPTION |
|-----|-------|---|
| 1 | RSTN | Active low hardware reset |
| 2 | SDA | I ² C data I/O |
| 3 | SCL | I ² C clock input |
| 4 | VON | Inverting Class-D output |
| 5 | PVDD | Charge Pump output |
| 6 | VOP | Non-inverting Class-D output |
| 7 | PGND | Power GND |
| 8 | C2P | Non-Inverting terminal of flying capacitance C2 |
| 9 | C1P | Non-Inverting terminal of flying capacitance C1 |
| 10 | PGND | Power GND |
| 11 | C2N | Inverting terminal of flying capacitance C2 |
| 12 | C1N | Inverting terminal of flying capacitance C1 |
| 13 | VDD | Battery power supply |
| 14 | GND | GND |
| 15 | DVDD | Digital power supply |
| 16 | DATAO | I ² S data out |
| 17 | DATAI | I ² S data input |
| 18 | WCK | I ² S word select input |
| 19 | BCK | I ² S bit clock input |
| 20 | AD | I ² C address select input |

FUNCTIONAL BLOCK DIAGRAM

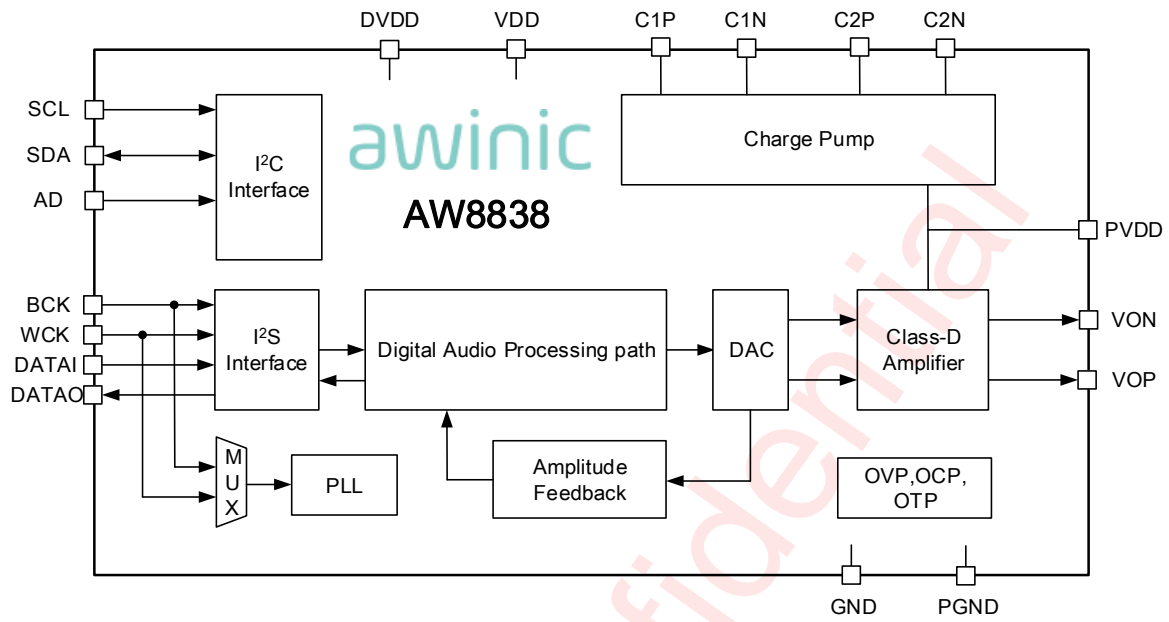


Figure 2 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION CIRCUITS

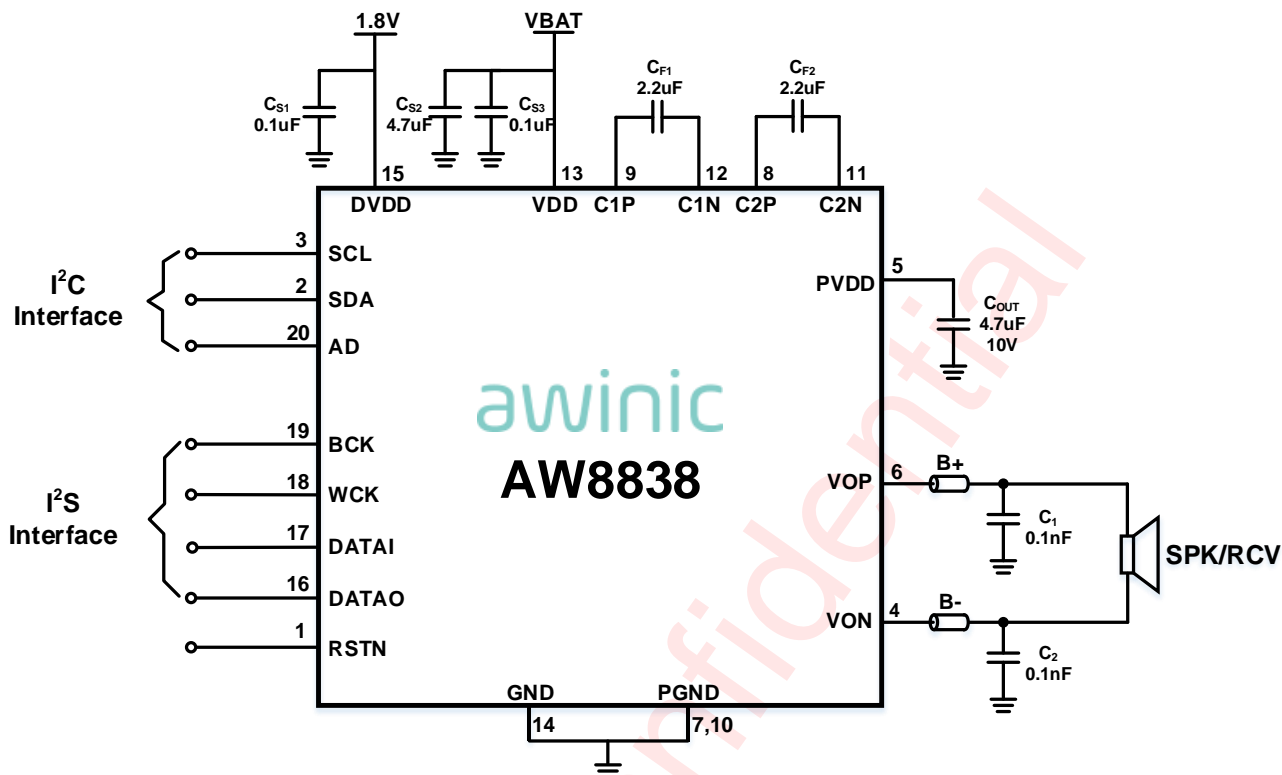


Figure 3 AW8838 Application Circuit

All trademarks are the property of their respective owners.

ORDERING INFORMATION

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|-------------|--------------|------------------|---------|----------------------------|---------------------------|------------------------------|
| AW8838FCR | -40°C ~ 85°C | FCQFN 2X3-20L | NZLP | MSL1 | RoHS+HF | 6000 units/ Tape and Reel |

ABSOLUTE MAXIMUM RATINGS^(NOTE1)

| PARAMETERS | | RANGE |
|--|--------------------|---------------------------|
| Battery Supply Voltage VDD | | -0.3V to 6V |
| Digital Supply Voltage DVDD | | -0.3V to 2V |
| Charge Pump Output Voltage PVDD | | -0.3V to 7V |
| Output Voltage Range | VOP, VON, C1P, C2P | -0.3V to PVDD + 0.3V |
| | C1N, C2N | -0.3V to VDD + 0.3V |
| Digital Input Voltage | RSTN, AD, SCL, SDA | -0.3V to VDD + 0.3V |
| | BCK, WCK, DATAI | -0.3V to DVDD + 0.3V |
| Minimum load resistance R _L | | 5Ω |
| Package Thermal Resistance θ _{JA} | | 60°C/W |
| Ambient Temperature Range | | -40°C to 85°C |
| Maximum Junction Temperature T _{JMAX} | | 165°C |
| Storage Temperature Range T _{STG} | | -65°C to 150°C |
| Lead Temperature(Soldering 10 Seconds) | | 260°C |
| ESD Rating | | |
| HBM(Human Body Model) ^(Note 2) | | ±4000V |
| CDM(Charge Device Model) ^(Note 3) | | ±2000V |
| Latch-up | | |
| Test Condition: JESD78E | | +IT: 450mA -IT: -450mA |

NOTE1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
Test method: MIL-STD-883J Method 3015.9

NOTE3: Test method: ESDA/JEDEC JS-002-2014

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition: $T_A=25^{\circ}\text{C}$, $V_{DD}=3.6\text{V}$, $DVDD=1.8\text{V}$, $R_L=8\Omega+33\mu\text{H}$, $f_{in}=1\text{kHz}$, $f_s=48\text{kHz}$ for typical values (unless otherwise noted)

| Symbol | Description | Test Conditions | Min | Typ. | Max | Units |
|--------------------|--|--|------|---------------------|------|---------------|
| V_{DD} | Battery supply voltage | On pin VDD | 3 | | 5.5 | V |
| V_{DVDD} | Digital supply voltage | On pin DVDD | 1.65 | 1.8 | 1.95 | V |
| I_{VDD} | Battery supply current | Operating mode, Charge Pump off | | 3 | | mA |
| | | Operating mode, Charge Pump on | | 8 | | mA |
| | | Power down mode | | 0.3 | 2 | μA |
| I_{DVDD} | Digital supply current | Operating mode | | 1.2 | | mA |
| | | Power down mode | | 3 | | μA |
| T_{ON} | Startup time | | | 2.5 | | ms |
| Charge Pump | | | | | | |
| $PVDD$ | Charge Pump output voltage | $V_{DD}=3\text{V to }4.0\text{V}$ | | $1.5 \times V_{DD}$ | | V |
| | | $V_{DD}>4.0\text{V}$ | | 6 | | V |
| V_{HYS} | OVP hysteresis voltage | $V_{DD}>4.0\text{V}$ | | 50 | | mV |
| F_{CP} | Operating Frequency | $f_s=48\text{kHz}$ | | 1.06 | | MHz |
| T_{ST} | Soft-start time | $C_{OUT}=4.7\mu\text{F}$ | | 1 | | ms |
| η_{CP} | Charge Pump efficiency | $V_{DD}=3.6\text{V}$, $I_{LOAD}=200\text{mA}$ | | 94 | | % |
| I_{LIMIT} | PVDD short limit current | | | 250 | | mA |
| Class-D | | | | | | |
| P_o | Speaker output power | THD+N=1%, $R_L=6\Omega+33\mu\text{H}$, $V_{DD}=4.2\text{V}$ | | 2.15 | | W |
| | | THD+N=10%, $R_L=6\Omega+33\mu\text{H}$, $V_{DD}=4.2\text{V}$ | | 2.75 | | W |
| | | THD+N=1%, $R_L=8\Omega+33\mu\text{H}$, $V_{DD}=4.2\text{V}$ | | 1.8 | | W |
| | | THD+N=10%, $R_L=8\Omega+33\mu\text{H}$, $V_{DD}=4.2\text{V}$ | | 2.2 | | W |
| η | Total efficiency (Charge Pump + Class-D) | $V_{DD}=4.2\text{V}$, $P_o=1.0\text{W}$, $R_L=8\Omega+33\mu\text{H}$ | | 86 | | % |
| | | $V_{DD}=4.2\text{V}$, $P_o=1.0\text{W}$, $R_L=6\Omega+33\mu\text{H}$ | | 85 | | % |
| V_{OS} | Output offset voltage | | -30 | 0 | 30 | mV |

| Symbol | Description | Test Conditions | | Min | Typ. | Max | Units |
|----------------------------------|--|--|-------|-----------------------|-----------------------|------------|-------------|
| R_{dson} | Total drain-source on-state resistance | High side MOS + Low side MOS | | | 350 | | mΩ |
| THD+N | Total harmonic distortion plus noise | $V_{DD}=4.2V$, $P_o=0.5W$, $R_L=8\Omega+33\mu H$ | | | 0.02 | | % |
| E_N | Receiver mode output noise | A-weighting | | | 15 | | μV |
| | Speaker mode output noise | A-weighting | | | 22 | | μV |
| SNR | Signal-to-noise ratio | $V_{DD}=4.2V$, $P_o=1.8W$, $R_L=8\Omega+33\mu H$, A-weighting | | | 105 | | dB |
| PSRR | Power supply rejection ratio | $V_{DD}=4.2V$, $V_{p-p_sin}=200mV$ | 217Hz | | -85 | | dB |
| | | | 1kHz | | -80 | | dB |
| Digital Logical Interface | | | | | | | |
| V_{IH} | High-level digital input voltage | BCK, WCK, DATA Pin | | $0.7 \times V_{DVDD}$ | | V_{DVDD} | V |
| V_{IL} | Low-level digital input voltage | | | | $0.3 \times V_{DVDD}$ | | V |
| V_{IH} | High-level digital input voltage | RSTN, SCL, SDA, AD Pin | | $0.7 \times V_{DVDD}$ | | 3.6 | V |
| V_{IL} | Low-level digital input voltage | | | | $0.3 \times V_{DVDD}$ | | V |
| V_{OH} | High-level digital input voltage | $I_{OUT}=-2mA$ | | $V_{DVDD} - 0.45$ | | | V |
| V_{OL} | Low-level digital input voltage | $I_{OUT}=2mA$ | | | | 0.45 | V |
| Protection | | | | | | | |
| T_{SD} | Over temperature protection threshold | | | | 160 | | $^{\circ}C$ |
| T_{SDR} | Over temperature protection recovery threshold | | | | 130 | | $^{\circ}C$ |
| UVP | Under-voltage protection voltage | | | | 2.5 | | V |
| | Under-voltage protection hysteresis voltage | | | | 100 | | mV |

I²C INTERFACE TIMING

| Parameter | | | Min | Typ. | Max | Units |
|-----------|---------------------|---|-----|------|-----|-------|
| No. | Sym | Name | | | | |
| 1 | f _{SCL} | SCL Clock frequency | | | 400 | kHz |
| 2 | t _{LOW} | SCL Low level Duration | 1.3 | | | μs |
| 3 | t _{HIGH} | SCL High level Duration | 0.6 | | | μs |
| 4 | t _{RISE} | SCL, SDA rise time | | | 0.3 | μs |
| 5 | t _{FALL} | SCL, SDA fall time | | | 0.3 | μs |
| 6 | t _{SU:STA} | Setup time SCL to START state | 0.6 | | | μs |
| 7 | t _{HD:STA} | (Repeat-start) Start condition hold time | 0.6 | | | μs |
| 8 | t _{SU:STO} | Stop condition setup time | 0.6 | | | μs |
| 9 | t _{BUF} | the Bus idle time START state to STOP state | 1.3 | | | μs |
| 10 | t _{SU:DAT} | SDA setup time | 0.1 | | | μs |
| 11 | t _{HD:DAT} | SDA hold time | 10 | | | ns |

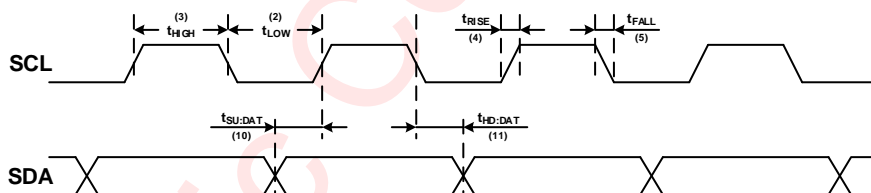


Figure 4 SCL and SDA timing relationships in the data transmission process

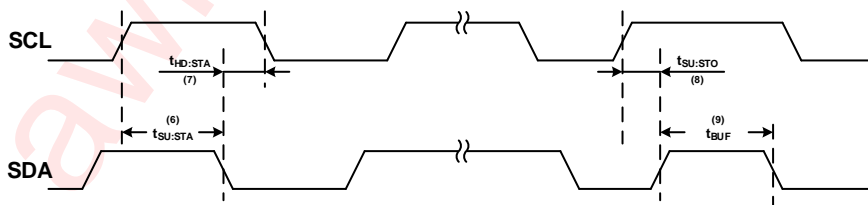
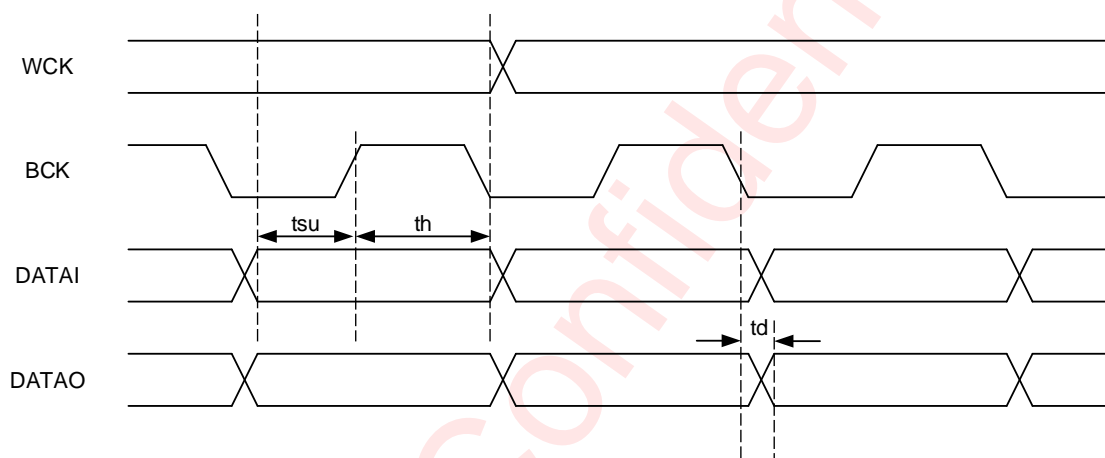


Figure 5 The timing relationship between START and STOP state

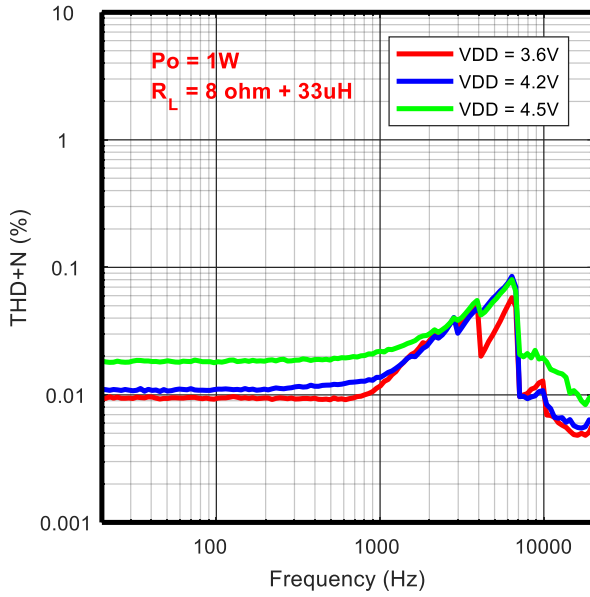
I²S INTERFACE TIMING

| Parameter Name | | Min | Typ. | Max | Units |
|----------------|---------------------------------|----------|------|----------|-------|
| f_s | Sampling frequency, on pin WCK | 8 | | 96 | kHz |
| f_{BCK} | Bit clock frequency, on pin BCK | 32 f_s | | 64 f_s | Hz |
| t_{su} | WCK, DATAI Setup time to BCK | 10 | | | ns |
| t_h | WCK, DATAI hold time to BCK | 10 | | | ns |
| t_d | DATAO output delay time to BCK | | | 50 | ns |

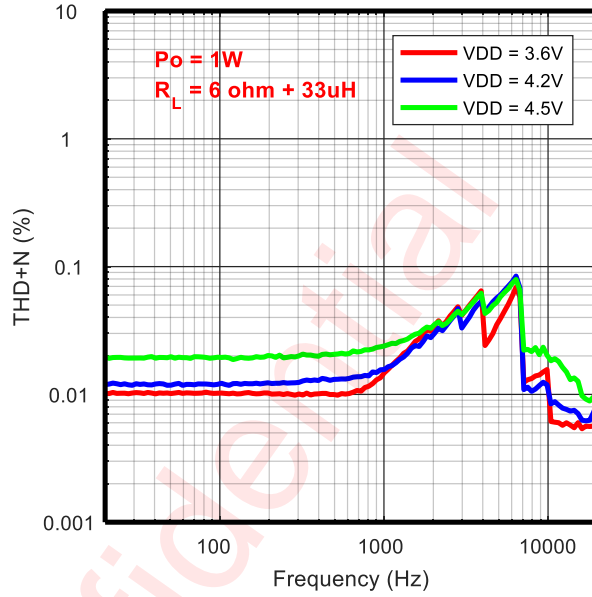
Figure 6 I²S Interface Timing

TYPICAL CHARACTERISTICS

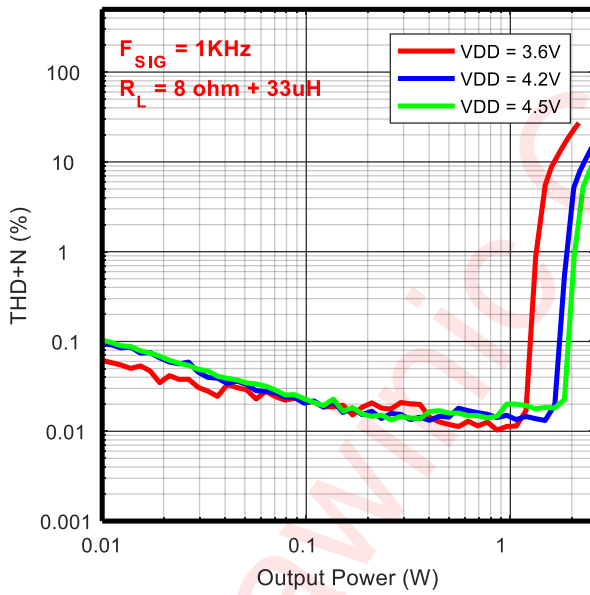
THD+N VS. FREQUENCY



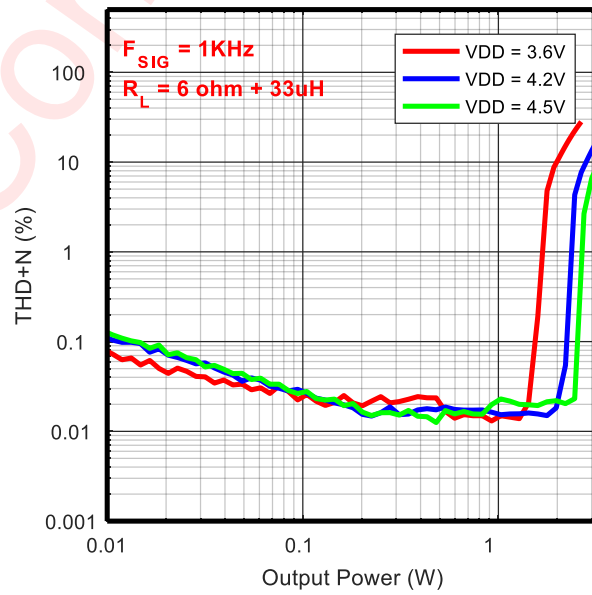
THD+N VS. FREQUENCY



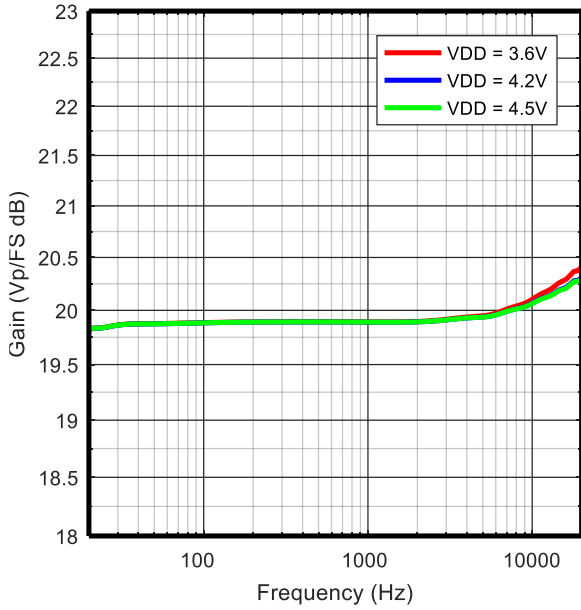
THD+N VS. OUTPUT POWER



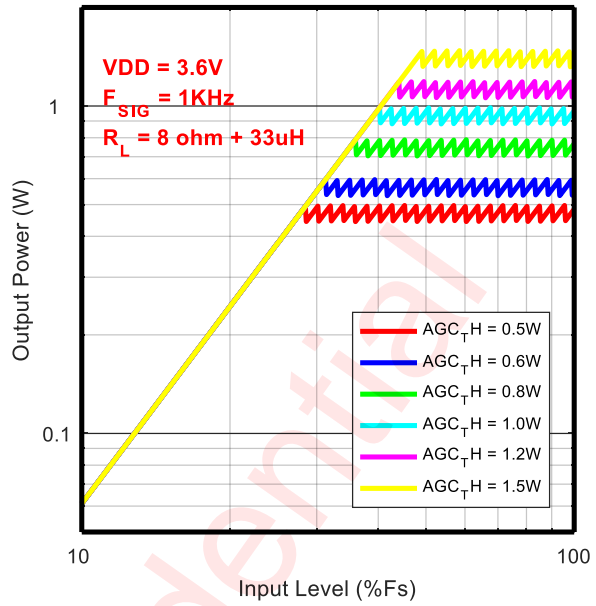
THD+N VS. OUTPUT POWER



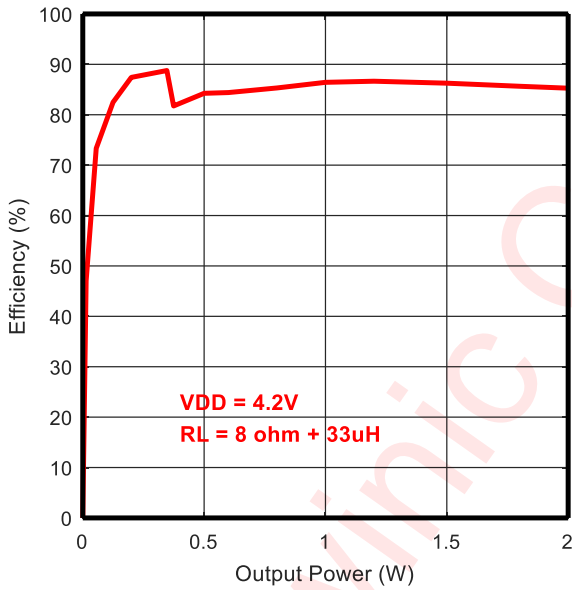
GAIN VS. FREQUENCY



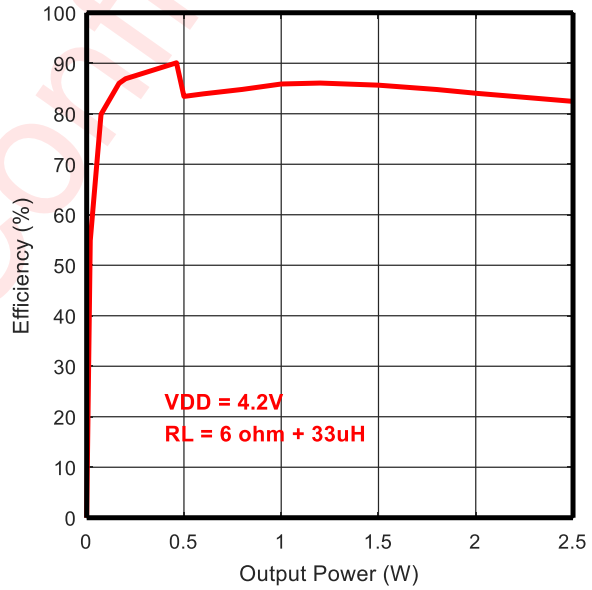
OUTPUT POWER VS. Din



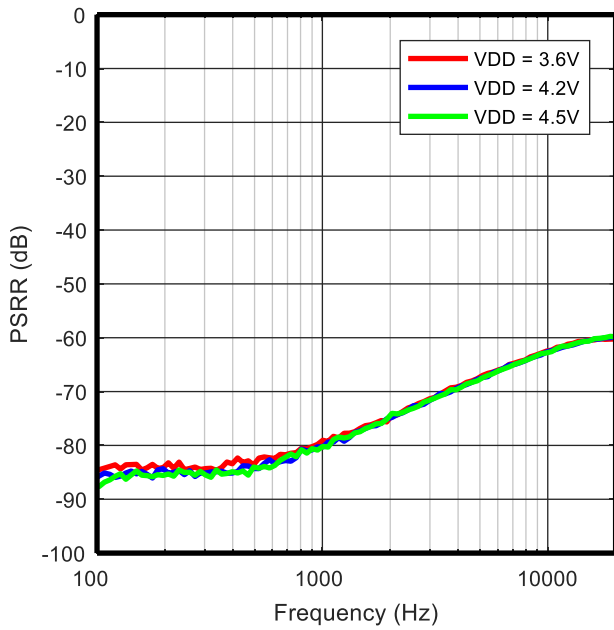
EFFICIENCY VS. OUTPUT POWER



EFFICIENCY VS. OUTPUT POWER



PSRR VS. FREQUENCY



awinic Confidential

DETAILED FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDD and DVDD supply voltage. When the VDD supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

| Mode | Condition | Description |
|-------------|--------------------------------------|--|
| Power-Down | $V_{DD} < 2.1V$ $V_{DVDD} < 1.1V$ | Power supply is not ready, chipset is power down. |
| Stand-By | $V_{DD} > 3V$ $V_{DVDD} > 1.65V$ | Power supply is ready, most parts of the device are power down for low power consumption except I ² C interface |
| Configuring | PWDN = 0 | Device is biased while Charge Pump and Class-K output is floating. Configuring DAP(Digital Audio Processor) |
| Operating | AMPPD = 0 | Amplifier is fully operating |

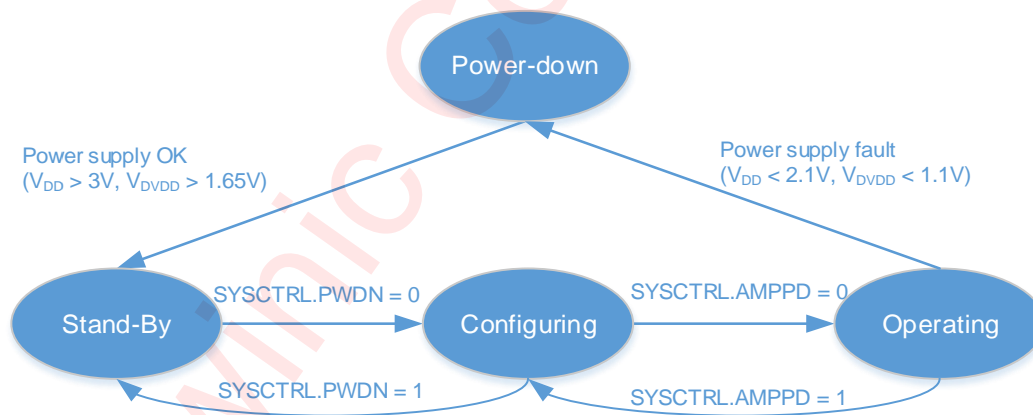


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- $V_{DVDD} < 1.1\text{ V}$
- $V_{DD} < 2.1\text{ V}$
- RSTN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

$$V_{DVDD} > 1.65\text{ V and } V_{DD} > 3\text{ V}$$

And RSTN goes HIGH.

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

CONFIG MODE

The device switches to OFF mode when:

- $\text{SYSCTRL.PWDN} = 0$
- $\text{SYSCTRL.AMPPD} = 1$

In this mode the internal bias, OSC, PLL will start to work

OPERATING MODE

The device is fully operational in this mode. Charge pump, amplifier loop and power stage circuits will start to work. Customer can set $\text{SYSCTRL.AMPPD} = 0$ to make device in this mode.

POWER UP SEQUENCE

This device power up sequence is illustrated in the following figure:

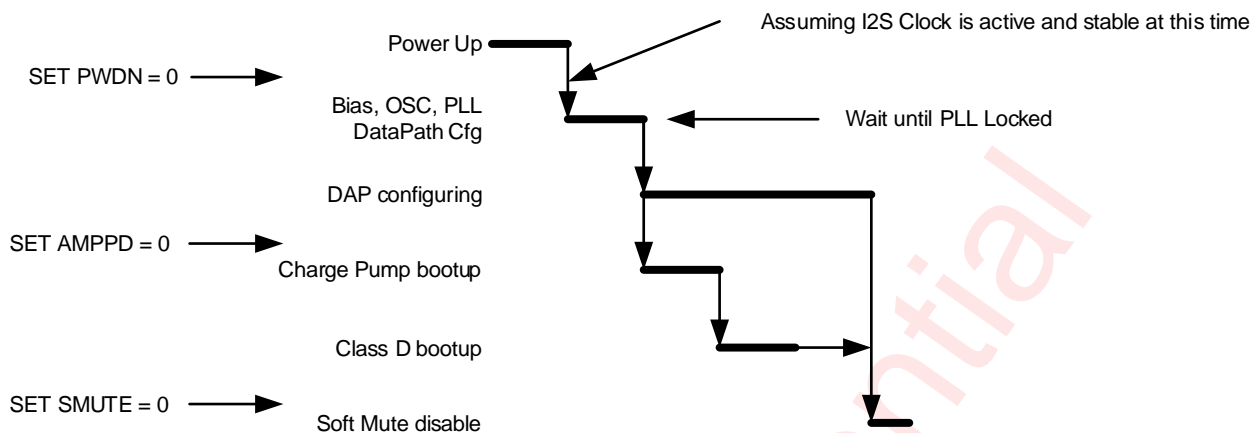


Figure 8 Power up sequence

Detail description for each step is listed in the following table.

Table 2 Detail Description of Power up sequence

| Index | Description | Mode |
|-------|---|-------------|
| 1 | Wait for VDD, DVDD supply power up | Power-Down |
| 2 | I ² S + Data Path Configuration | Stand-By |
| 3.1 | Enable system (SYSCTRL.PWDN = 0) | Configuring |
| 3.2 | Bias, OSC, PLL active | |
| 3.3 | Waiting for PLL locked | |
| 4a.1 | DAP Configuration | |
| 4a.2 | DAP enable | Operating |
| 4b.1 | Enable Charge Pump and amplifier (SYSCTRL.AMPPD = 0) Charge pump and Amplifier boot up | |
| 4b.2 | Wait SYSST.SWS = 1 | |
| 5 | Release Hard-Mute Data Path active | |

Power up sequence considering I²S, I²C timing shows as below:

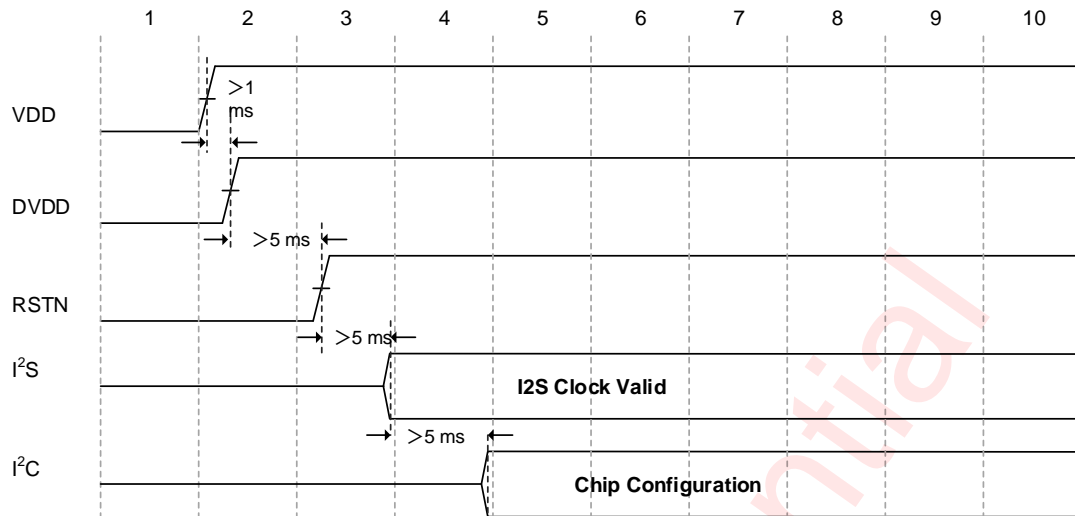


Figure 9 Power Up Sequence

Power down sequence considering I²S, I²C timing shows as below:

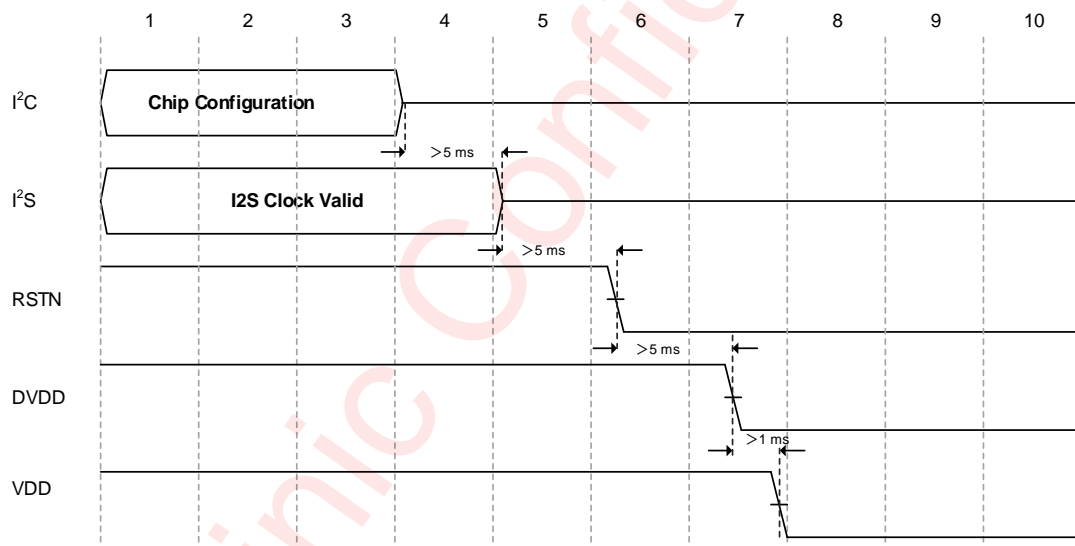


Figure 10 Power Down Sequence

SOFTWARE RESET

Writing 0x55AA to register ID via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK

- DATAI
- DATAO

Two-slot I²S is supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified mode, which can be configured via I2SCTRL.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (f_s): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz. It is selected via configurable register I2SCTRL.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL.I2SBCK. The frequency of BCK can be calculated according to the following equation:

$$BCK\ frequency = SampleRate \times SlotLength \times SlotNumber$$

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: 2-slot supported in I2S mode.

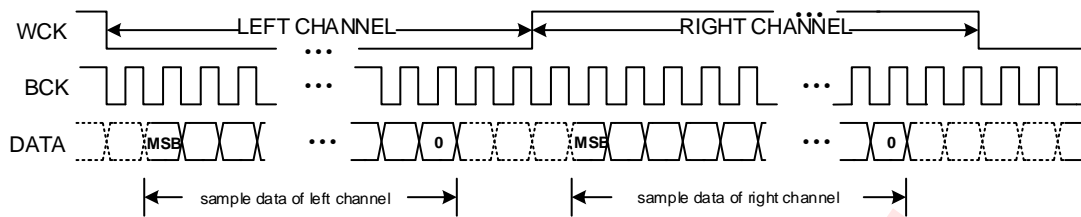
The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The input audio data can be attenuated -6dB in this module, by setting bit I2SCTRL.INPLEV. The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL.CHSEL.

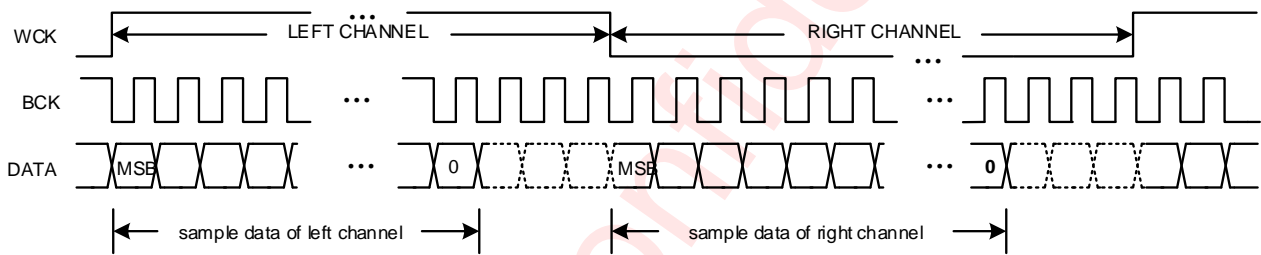
Table 3 Supported I²S interface parameters

| Interface format(MSB first) | Data width | BCK frequency |
|-----------------------------|-------------|---|
| Standard I ² S | 16b | 32 f _s /48 f _s /64 f _s |
| | 20b/24b/32b | 48 f _s /64 f _s |
| Left-justified | 16b | 32 f _s /48 f _s /64 f _s |
| | 20b/24b/32b | 48 f _s /64 f _s |
| Right-justified | 16b | 32 f _s /48 f _s /64 f _s |
| | 20b/24b/32b | 48 f _s /64 f _s |

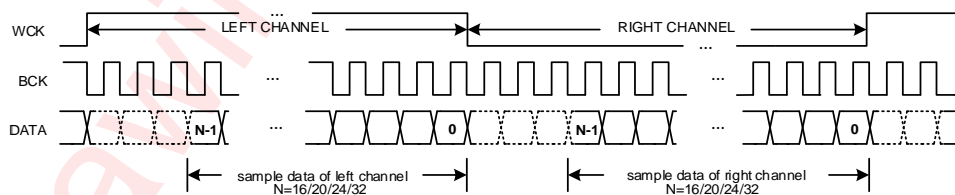
The output port DATAO, can be enabled or disabled via bit I2SCFG1.I2STXEN. The unused slots can be set to zero or Hi-Z, which is controlled by I2SCFG1.DOZH.

STANDARD I²S MODE:**Figure 11 I²S Timing for Standard I²S Mode**

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE:**Figure 12 I²S Timing for Left-Justified Mode**

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the rising edge of the word clock.

RIGHT-JUSTIFIED MODE:**Figure 13 I²S Timing for Right-Justified Mode**

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- DCC
- AGC
- Volume control
- Mute

The signal processing flow in the DAP(Digital Audio Processor) is illustrated in the following figure.

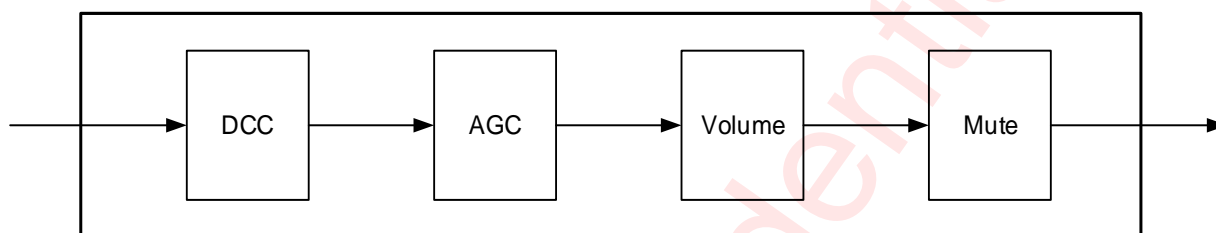


Figure 14 Block Diagram of DAP

DCC

This module perform DC canceling for the input audio stream. Blocking DC components into analog class D loop.

AGC

In the actual audio application, system output power tends to be more than rated power of speaker, such as in the 6V power supply, as for 8ohms speaker, the maximum undistorted power is about 1.8W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with AGC can protect the speaker effectively, When the output power is not exceeds the setting threshold, the AGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the AGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -96db with 0.5db/step

MUTE

This module perform mute control for the audio stream.

CHARGE PUMP

This device adopts a new generation of charge pump technology: K-Chargepump structure. It has higher efficiency and larger driving capability. Its operating frequency is 1.06MHz. With built-in soft-start circuit, current-limit control loop and over-voltage-protection (OVP) loop, charge pump of this configuration can provide more stable and reliable power supply. The Charge Pump can work in different mode via CPCTRL.CP_MD:

- **Pass-through mode:** the voltage of VDD is transparently passed to output of converter PVDD
- **Force CP mode:** the output voltage is 1.5 times of supply voltage VDD
- **Adaptive CP mode:** the output voltage can be switch between VDD and 1.5 times of VDD according to the input audio level.

Pass-through mode

The internal Charge Pump circuit is not working; the voltage of VDD is passed to PVDD directly.

Force CP mode

The Charge Pump circuit is always working and the output voltage is 1.5 times of supply voltage VDD.

Adaptive CP mode

The Charge Pump circuits working dynamically according to the input audio level. When the level of input audio signal is below the setting threshold, the Charge Pump circuit will not work. Till the level of input audio signal raised up and above the threshold, the Charge Pump circuit starts to work and boost the amplifier supply rail to 1.5 times of supply voltage VDD before the audio signal arriving amplifier power stage.

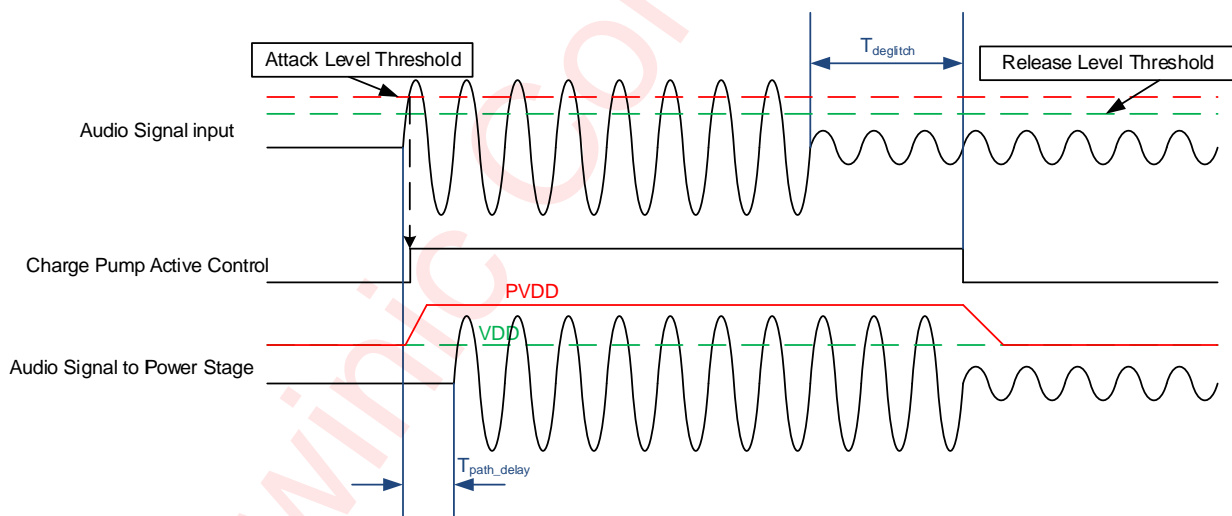


Figure 15 Charge Pump Circuit Behavior in Adaptive CP Mode

HIGH EFFICIENCY

The output voltage PVDD is 1.5 times of supply voltage VDD in K-Chargepump, of which the ideal efficiency can reach 100%. Actually, the K-Chargepump efficiency can be calculated as the ratio of output power to input power, that is

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\%$$

For example, in an ideal M-times charge pump, the input current I_{IN} is M times of the output current I_{OUT} , the efficiency formula can be written as:

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot M \cdot I_{OUT}} \times 100\% = \frac{V_{OUT}}{M \cdot V_{IN}} \times 100\%$$

Also, M is a parameter depending on the operating mode of a charge pump; V_{OUT} is the output voltage of a charge pump; V_{IN} is the input voltage (generally is also the power supply voltage) of a charge pump; I_{OUT} is also the load current. For K-Chargepump structure, the output voltage is 1.5 times of the input voltage. Due to the switch loss and quiescent current loss inside the charge pump, the actual efficiency can still be up to 93%. As a result, the power booster technology of K-Chargepump can greatly improve the power efficiency.

CHARGE PUMP STRUCTURE

As shown in Figure 16 is a Charge Pump fundamental functional diagram: Charge Pump integrated in AW8838 has seven switches, of which the output voltage PVDD is boosted to 1.5 times as input voltage V_{DD} through seven switches operating timing.

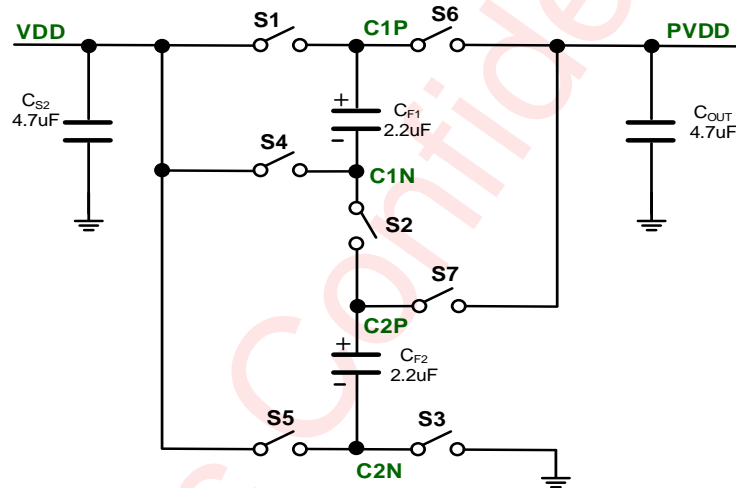


Figure 16 K-Chargepump Functional Diagram

The operation of the charge pump has two phases. In ϕ_1 , as shown in Figure 17, when switches S1, S2 and S3 are closed, VDD charges to the flying capacitor C_{F1} and C_{F2} .

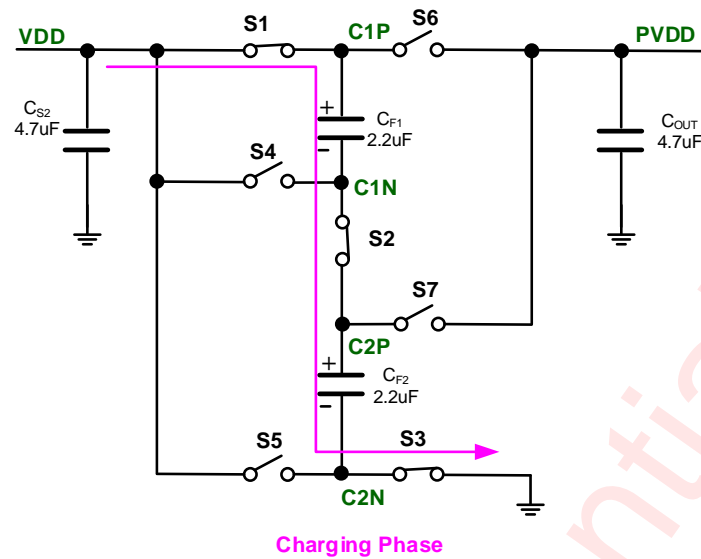


Figure 17 Φ_1 : Charge Flying Capacitors CF1 and CF2

In Φ_2 , as shown in Figure 18, switches S1, S2 and S3 are opened, and switches S4, S5, S6 and S7 are closed. Because the voltage across the capacitor can't change instantaneously, so either the voltage on flying capacitors C_{F1} or C_{F2} , is added to the VDD, realizing a PVDD boosted to a higher voltage.

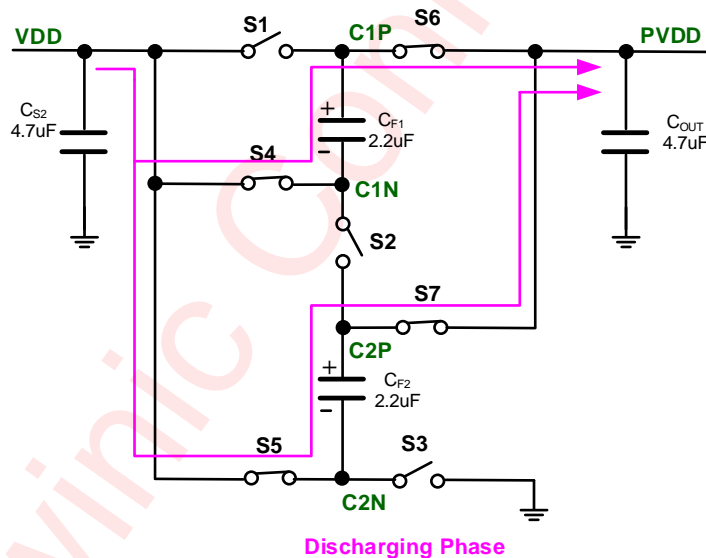


Figure 18 Φ_2 : Flying Capacitor Charges Transfer to the Output Capacitor COUT

SOFT START

K-chargepump has integrated soft start function in order to limit inrush current from power supply during start-up. The current from power supply can be limited to 300mA, and the start-up time is about 1ms.

PEAK CURRENT CONTROL

K-chargepump has integrated a peak current control circuit. In normal operation, when a heavy load or a situation that makes the charge pump extracts very large current from power supply, the peak current control circuit can limit the maximum output load current, which is typically 2A.

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

K-Chargepump keeps the output voltage PVDD a multiple of the input voltage VDD. It provides a high voltage power rail for internal power amplifier circuits, allowing the amplifiers provide greater output dynamic range in the lithium battery voltage range, realizing much larger volume, higher audio quality. K-Chargepump has integrated an over-voltage protection circuit. When the input voltage VDD is greater than 4V, the output voltage PVDD is no longer a multiple of VDD, but a controlled voltage by over-voltage protection (OVP) circuit and kept in 6V. The hysteresis voltage of OVP is about 50mV.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again.

Over current (short) protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to PVDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. Speaker and Receiver combo applications can be realized without changing any hardware.

When the device is set to receiver mode, the power supply of Class D driver stage is from VDD directly.

AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP_NORM_V \times D_{in}$$

D_{in} : the level of input signal with a range from -1 to +1

AMP_NORM_V: the equivalent amplifier output voltage when D_{in} is 1. In receiver mode the AMP_NORM_V is 4.5V. In speaker mode the default AMP_NORM_V is 10V, and it is selected via configurable register AMPCTRL.AMP_NORM_V.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) is decided by the connection of the AD pin. The connection of AD pin configures

the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7bit) or 0x37(7-bit).

Table 4 Address Selection

| AD pin | A1 | A0 | I ² C address (7-bit) |
|-----------------|----|----|----------------------------------|
| Connects to GND | 0 | 0 | 0x34 |
| Connects to VDD | 1 | 1 | 0x37 |

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

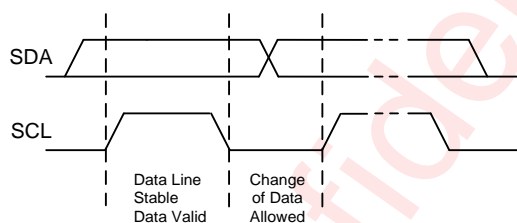


Figure 19 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

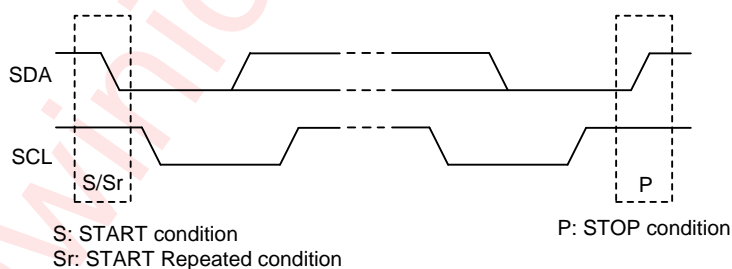


Figure 20 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

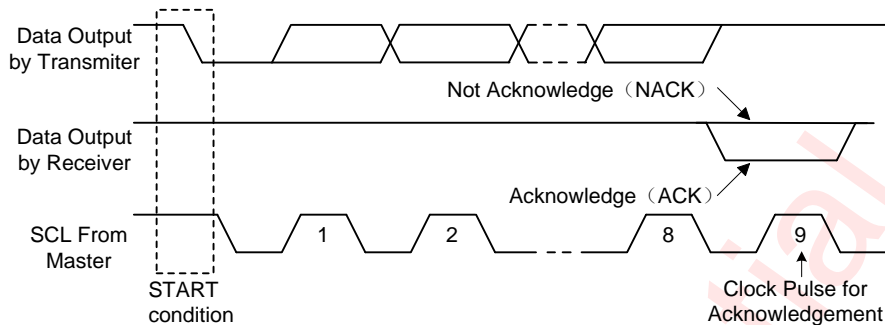


Figure 21 I²C ACK Timing

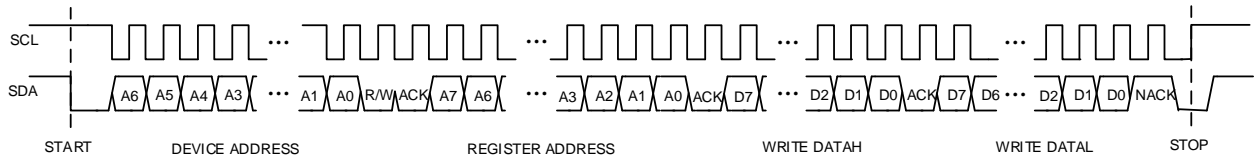
WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

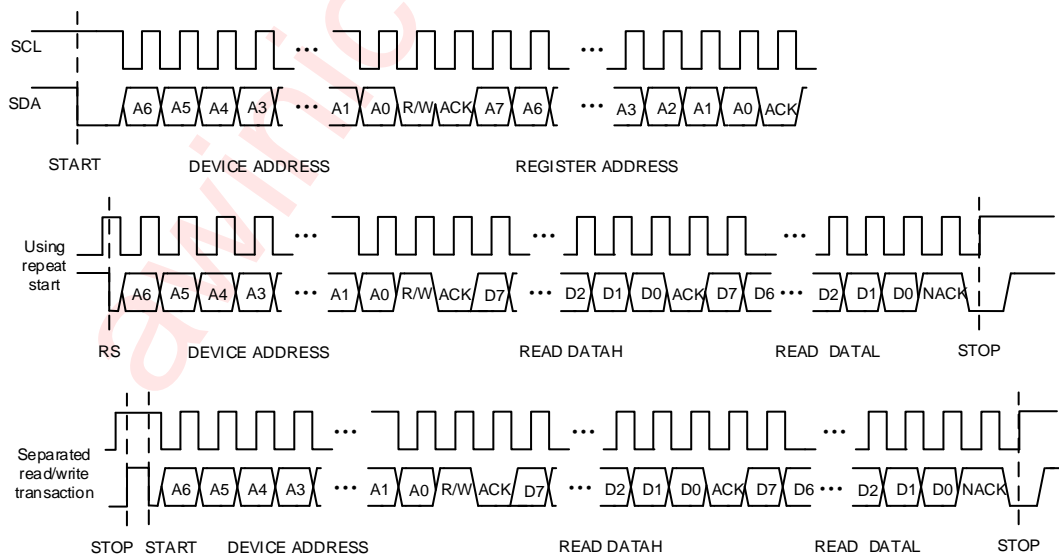
In a write process, the following steps should be followed:

- a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- b) Master device sends slave address (7-bit) and the data direction bit ($r/w = 0$).
- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit)
- e) Slave sends acknowledge signal
- f) Master sends high data byte of 16-bit data to be written to the addressed register
- g) Slave sends acknowledge signal
- h) Master sends low data byte of 16-bit data to be written to the addressed register
- i) Slave sends acknowledge signal
- j) If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)
- k) Master generates STOP condition to indicate write cycle end

Figure 22 I²C Write Byte Cycle**READ CYCLE**

In a read cycle, the following steps should be followed:

- a) Master device generates START condition
- b) Master device sends slave address (7-bit) and the data direction bit ($r/w = 0$).
- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit)
- e) Slave sends acknowledge signal
- f) Master generates STOP condition followed with START condition or REPEAT START condition
- g) Master device sends slave address (7-bit) and the data direction bit ($r/w = 1$).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends read high data byte of 16-bit data from addressed register.
- j) Master sends acknowledge signal.
- k) Slave sends read low data byte of 16-bit data from addressed register.
- l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.
- m) If the master device generates STOP condition, the read cycle is ended.

Figure 23 I²C Read Byte Cycle

REGISTER CONFIGURATION

Register List

| ADDR | NAME | BIT | | | | | | | | | | | | | | | | | | | |
|------|----------|--------|------|--------|----|------|-------|--------|----------|---|-------|----------|----------|--------|--------|------|------|-------|------------|--|--------|
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| 0x00 | ID | IDCODE | | | | | | | | | | | | | | | | | | | |
| 0x01 | SYSST | | UVLS | ADPS | | OVPS | | VOUTHS | SWS | | | NOCLKS | CLKS | OCDS | OTLS | OTHS | PLLS | | | | |
| 0x02 | SYSINT | | UVLI | ADPI | | OVPI | | VOUTHI | SWI | | | NOCLKI | CLKI | OCDI | OTLI | OTHI | PLLI | | | | |
| 0x04 | SYSCTRL | | | | | | | | | | | RCV_MODE | I2SEN | WSINV | BCKINV | IPLL | | AMPPD | PWDN | | |
| 0x05 | I2SCTRL | | | INPLEV | | | CHSEL | | I2SMD | | | I2SFS | | I2SBCK | | | | I2SSR | | | |
| 0x06 | I2SCFG1 | | | | | | | | | | | | DRVSTREN | DOHZ | | | | | I2STXEN | | |
| 0x08 | PWMCTRL | | | | | | | | | | | | | | | | | HDCCE | HMUTE | | |
| 0x10 | HAGCCFG0 | | | | | | | | | | | | | | | | | | AVTH | | |
| 0x13 | HAGCCFG1 | | | | | | | | | | | | | | | | | | ATTH_NORM | | |
| 0x14 | HAGCCFG2 | | | | | | | | | | | | | | | | | | RVTH | | |
| 0x15 | HAGCCFG3 | | | | | | | | | | | | | | | | | | RTTH | | |
| 0x16 | HAGCCFG4 | | | | | | | | | | | | | | | | | | HOLDTH | | |
| 0x17 | HAGCCFG5 | | | | | | | | HPFE | | | | | | | | | | AGCE | | |
| 0x18 | HAGCCFG5 | | | | | | | | HPFE | | | | | | | | | | AGCE | | |
| 0x21 | I2SCFG2 | | | | | | | | | | | | | | | | | | I2SRXEN | | |
| 0x50 | HPFCFG1 | | | | | | | | | | | | | | | | | | a1 | | |
| 0x51 | HPFCFG2 | | | | | | | | | | | | | | | | | | a2 | | |
| 0x52 | HPFCFG3 | | | | | | | | | | | | | | | | | | b0 | | |
| 0x53 | HPFCFG4 | | | | | | | | | | | | | | | | | | b1 | | |
| 0x54 | HPFCFG5 | | | | | | | | | | | | | | | | | | b2 | | |
| 0x60 | CPCTRL | | | | | | | | VPWR_SEL | | CP_MD | | | | | | | | CP_RTH | | CP_ATH |
| 0x63 | AMPCTRL | | | | | | | | | | | | | | | | | | AMP_NORM_V | | |

REGISTER DETAILED DESCRIPTION**ID: Chip ID Register (Address 00h)**

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|--|---------|
| 15:0 | IDCODE | R | Chip ID (1730h) will be returned after read. All configuration registers will be reset to default value after 0x55aa is written | 0x1730 |

SYSST: System Status Register (Address 01h)

| Bit | Symbol | R/W | Description | Default |
|-----|----------|-----|---|---------|
| 15 | Reserved | - | Reserved | |
| 14 | UVLS | R | VDD under voltage indicator 1: VDD < 2.5V; 0: VDD > 2.6V | |
| 13 | ADPS | R | Charge Pump Adaptive status 0: transparent; 1: 1.5X | |
| 12 | Reserved | - | Reserved | |
| 11 | OVPS | R | Charge Pump OVP status indicator | |
| 10 | Reserved | - | Reserved | |
| 9 | VOUTH5 | R | Charge Pump voltage indicator 1: PVDD > VDD + 0.2V; 0: PVDD < VDD + 0.2V | |
| 8 | SWS | R | Amplifier switching status 1:switching; 0:not switching | |
| 7:6 | Reserved | - | Reserved | |
| 5 | NOCLKS | R | The reference clock of PLL is not available | |
| 4 | CLKS | R | All internal clock are stable | |
| 3 | OCDS | R | Over current status in amplifier | |
| 2 | OTLS | R | Junction temperature is above 150°C | |
| 1 | OTHS | R | Junction temperature is above 160°C | |
| 0 | PLLS | R | PLL locked status 1: locked; 0: unlocked | |

SYSINT: System Interrupt Register (Address 02h)

| Bit | Symbol | R/W | Description | Default |
|-----|----------|-----|---|---------|
| 15 | Reserved | RC | Reserved | |
| 14 | UVLI | RC | Interrupt indicator for Power On and UVLS | |
| 13 | ADPI | RC | Interrupt indicator for ADPS | |
| 12 | Reserved | - | Reserved | |
| 11 | OVPI | RC | Interrupt indicator for OVPS | |
| 10 | Reserved | - | Reserved | |
| 9 | VOUTH1 | RC | Interrupt indicator for VOUTH5 | |

| Bit | Symbol | R/W | Description | Default |
|---|----------|-----|--------------------------------|---------|
| 8 | SWI | RC | Interrupt indicator for SWS | |
| 7:6 | Reserved | - | Reserved | |
| 5 | NOCLKI | RC | Interrupt indicator for NOCLKS | |
| 4 | CLKI | RC | Interrupt indicator for CLKS | |
| 3 | OCDI | RC | Interrupt indicator for OCDS | |
| 2 | OTLI | RC | Interrupt indicator for OTLS | |
| 1 | OTHI | RC | Interrupt indicator for OTHS | |
| 0 | PLLI | RC | Interrupt indicator for PLLS | |
| Note: It will be set to '1' once corresponding interrupt bit changed | | | | |

SYSCTRL: System Control Register (Address 04h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|--|---------|
| 15:8 | Reserved | - | Reserved | |
| 7 | RCV_MODE | RW | Receiver mode enable | 0x0 |
| 6 | I2SEN | RW | Enable/Disable whole I2S interface module 0: disable 1: enable | 0x0 |
| 5 | WSINV | RW | I2S Left/Right channel switch 0: No switch 1: Left/Right switch | 0x0 |
| 4 | BCKINV | RW | I2S bit clock invert control 0: not invert 1: inverted | 0x0 |
| 3 | IPLL | RW | PLL reference clock selection 0: bit clock 1: word selection signal | 0x0 |
| 2 | Reserved | - | Reserved | |
| 1 | AMPPD | RW | Amplifier power down control bit 0: Amplifier active 1: Amplifier power down | 0x1 |
| 0 | PWDN | RW | System power down control bit 0: active 1: All circuits will enter power down mode | 0x1 |

I2SCTRL: I2S interface Control Register (Address 05h)

| Bit | Symbol | R/W | Description | Default |
|-------|----------|-----|---|---------|
| 15:14 | Reserved | - | Reserved | |
| 13 | INPLEV | RW | Input level selection 0: All input signal will not be attenuated at first 1: All input signal will be attenuated by -6dB at first | 0x0 |
| 12 | Reserved | - | Reserved | |

| Bit | Symbol | R/W | Description | Default |
|-------|--------|-----|---|---------|
| 11:10 | CHSEL | RW | Left/right channel selection for I2S input 0: reserved 1: left 2: right 3: mono;(L+R)/2 | 0x1 |
| 9:8 | I2SMD | RW | I2S interface mode 0: Philip standard I2S 1: MSB justified 2: LSB justified 3: Reserved | 0x0 |
| 7:6 | I2SFS | RW | I2S data width 0: 16 bits 1: 20 bits 2: 24 bits 3: 32 bits | 0x3 |
| 5:4 | I2SBCK | RW | I2S BCK mode 0: 32 fs 1: 48 fs 2: 64 fs 3: Reserved | 0x2 |
| 3:0 | I2SSR | RW | I2S interface sample rate configuration: 0: 8 kHz 1: 11.025 kHz 2: 12 kHz 3: 16 kHz 4: 22.05 kHz 5: 24 kHz 6: 32 kHz 7: 44.1 kHz 8: 48 kHz 9: 96 kHz 10: Reserved 11~15: 48 kHz | 0x8 |

I2SCFG1: I2S Channel Configuration Register 1(Address 06h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|--|---------|
| 15:6 | Reserved | - | Reserved | |
| 5 | DRVSTREN | RW | I2S_DATA0 PAD driving strength setting 0: 2mA 1: 8mA | 0x1 |
| 4 | DOHZ | RW | Unused channel data mode 0: 0 1: HiZ | 0x1 |
| 3:1 | Reserved | - | Reserved | |
| 0 | I2STXEN | RW | Enable/Disable I2S transmitter module 0: disable 1: enable | 0x0 |

PWMCTRL: PWM Control Register (Address 08h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|--|---------|
| 15:2 | Reserved | - | Reserved | |
| 1 | HDCCE | RW | Hardware DC Canceling control 0: hard DC cancel disable 1: hard DC cancel enable | 0x1 |
| 0 | HMUTE | RW | Hardware mute control 0: hard mute disable 1: hard mute enable | 0x1 |

HAGCCFG0: Hardware AGC Configuration Register 0 (Address 10h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|--|---------|
| 15:8 | Reserved | - | Reserved | |
| 7:0 | AVTH | RW | Attack amplitude threshold of AGC, in percent of signal full scale | 0x7F |

HAGCCFG1: Hardware AGC Configuration Register 1 (Address 13h)

| Bit | Symbol | R/W | Description | Default |
|------|-----------|-----|---|---------|
| 15:0 | ATTH_NORM | RW | Attack time threshold of AGC in unit of 20.83uS 0: reserved n: gain decreased 0.5dB per n x 20.83uS | 0x7 |

HAGCCFG2: Hardware AGC Configuration Register 2 (Address 14h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|--|---------|
| 15:8 | Reserved | - | Reserved | |
| 7:0 | RVTH | RW | Release amplitude threshold, in percent of signal full scale | 0x70 |

HAGCCFG3: Hardware AGC Configuration Register 3 (Address 15h)

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|---|---------|
| 15:0 | RTTH | RW | Release time threshold in unit of 20.83uS 0: reserved n: gain increased 0.5dB per n x 20.83uS | 0x30 |

HAGCCFG4: Hardware AGC Configuration Register 4 (Address 16h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|---|---------|
| 15:8 | Reserved | - | Reserved | |
| 7:0 | HOLDTH | RW | Hold time threshold in unit of 166uS 0: reserved n: attack counter holding as least n x 166uS | 0x60 |

HAGCCFG5: Hardware AGC Configuration Register 5 (Address 17h)

| Bit | Symbol | R/W | Description | Default |
|-------|----------|-----|--|---------|
| 15:11 | Reserved | - | Reserved | |
| 10 | HPFE | RW | HPF control 0: HPF disable 1: HPF enable | 0x0 |
| 9 | Reserved | - | Reserved | |
| 8 | AGCE | RW | AGC control 0: AGC disable 1: AGC enable | 0x0 |
| 7:0 | Reserved | - | Reserved | |

HAGCCFG6: Hardware AGC Configuration Register 6 (Address 18h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|---|---------|
| 15:8 | VOL | RW | Volume control, from 0 to -96dB [3:0] : in unit of -0.5dB [7:4] : in unit of -6dB | 0x00 |
| 7:0 | Reserved | - | Reserved | 0x00 |

I2SCFG2: I2S Channel Configuration Register 2 (Address 21h)

| Bit | Symbol | R/W | Description | Default |
|------|----------|-----|---|---------|
| 15:1 | Reserved | - | Reserved | |
| 0 | I2SRXEN | RW | Enable/Disable I2S receiver module 0: disable 1: enable | 0x1 |

HPFCFG1: HPF Configuration Register 1 (Address 50h)

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|---------------------------|---------|
| 15:0 | a1 | RW | HPF filter coefficient a1 | 0xE04C |

HPFCFG2: HPF Configuration Register 2 (Address 51h)

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|---------------------------|---------|
| 15:0 | a2 | RW | HPF filter coefficient a2 | 0xFB5 |

HPFCFG3: HPF Configuration Register 3 (Address 52h)

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|---------------------------|---------|
| 15:0 | b0 | RW | HPF filter coefficient b0 | 0x1000 |

HPFCFG4: HPF Configuration Register 4 (Address 53h)

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|---------------------------|---------|
| 15:0 | b1 | RW | HPF filter coefficient b1 | 0xE000 |

HPFCFG5: HPF Configuration Register 5 (Address 54h)

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|---------------------------|---------|
| 15:0 | b2 | RW | HPF filter coefficient b2 | 0x1000 |

CPCTRL: CP Control Register (Address 60h)

| Bit | Symbol | R/W | Description | Default |
|-------|----------|-----|--|---------|
| 15:11 | Reserved | - | Reserved | |
| 10 | PWL_SEL | RW | Supply power selection 0: normal option 1: high voltage option | 0x0 |
| 9:8 | CP_MD | RW | Charge Pump mode selection 0: Transparent Mode 1: Adaptive Mode 2: Force 1.5X Mode 3: Reserved | 0x0 |
| 7:4 | CP_RTH | RW | Adaptive Charge Pump release threshold in unit of 3.125% | 0x3 |
| 3:0 | CP_ATH | RW | Adaptive Charge Pump attack threshold in unit of 3.125% | 0x8 |

AMPCTRL: AMP Control Register (Address 63h)

| Bit | Symbol | R/W | Description | Default |
|-------|------------|-----|--|---------|
| 15:14 | Reserved | - | Reserved | |
| 13 | AMP_NORM_V | RW | Amplifier output gain selection in speaker mode 0: 7V 1: 10V | 0x1 |
| 12:0 | Reserved | - | Reserved | |

APPLICATION INFORMATION

EXTERNAL COMPONENTS

SELECTION OF SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically $0.1\mu\text{F}$. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW8838 is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the $0.1\mu\text{F}$ ceramic capacitor, place a $10\mu\text{F}$ capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

SELECTION OF CHARGE PUMP FLYING CAPACITOR

Value of charge pump flying capacitors (C_{F1}, C_{F2}) affects load regulation and output impedance of the charge pump. Small capacitance may degrade driving capability of AW8838. A $2.2\mu\text{F}/6.3\text{V}$ ceramic capacitor is usually recommended.

SELECTION OF CHARGE PUMP OUTPUT CAPACITOR

Capacitance and ESR of charge pump output capacitors (C_{OUT}) directly affect ripple magnitude of charge pump output voltage (PVDD). Increasing C_{OUT} Capacitance reduces variations of PVDD and decreasing C_{OUT} ESR also reduces both ripple and output resistance. A $4.7\mu\text{F}/10\text{V}$ ceramic capacitor is usually recommended.

USAGE OF FERRITE BEAD AND FILTER CAPACITOR

Without ferrite beads and filter capacitors, AW8838 can still pass the specifications of FCC and CE. If there is any EMI sensitive device near AW8838 and/or there are long traces routing from the amplifier to a speaker, use ferrite beads and filter capacitors and place beads and capacitors as close as possible to output pins (VOP&VON), as Figure 22 below.

In Speaker Mode, outputs of AW8838 are square-wave PWM signals, which charge and discharge filter capacitors in each period, and result in additional static power consumption. Bigger filter capacitance, larger current consumption. Therefore, 0.1nF ceramic capacitor is usually recommended for low power application.

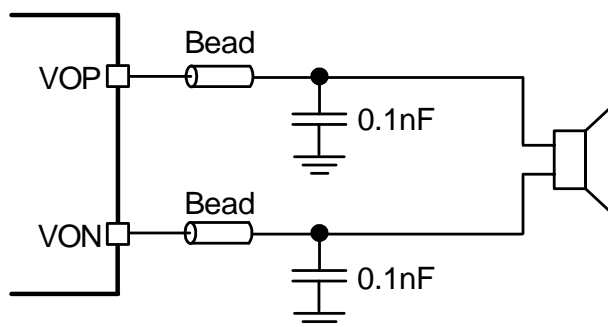


Figure 24 Ferrite Beads and Filter Capacitors

PCB LAYOUT CONSIDERATIONS

EXTERNAL COMPONENTS PLACEMENT

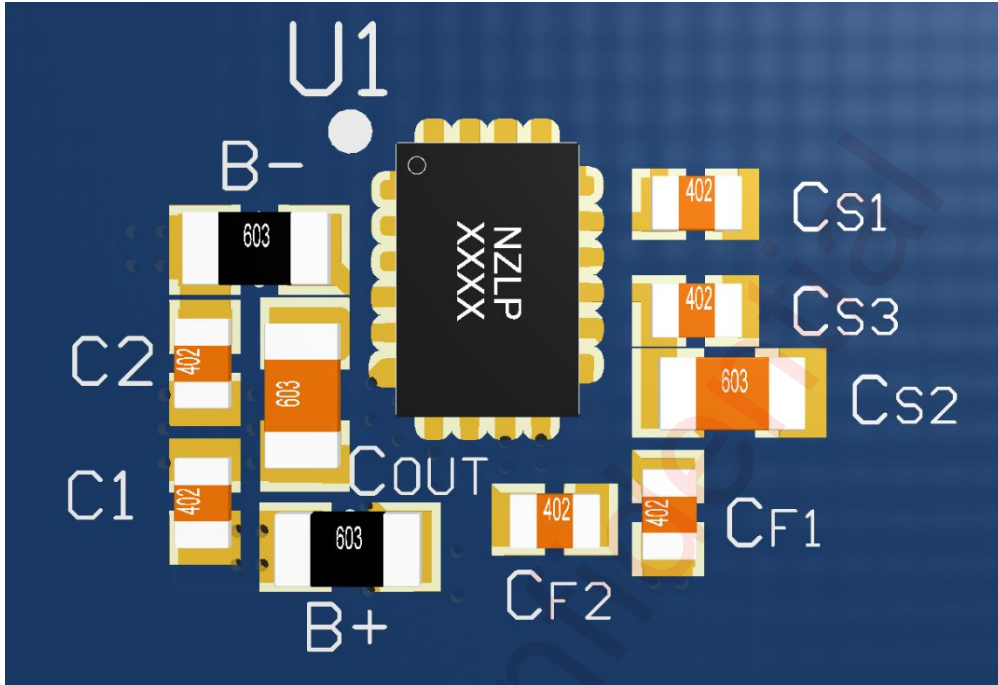


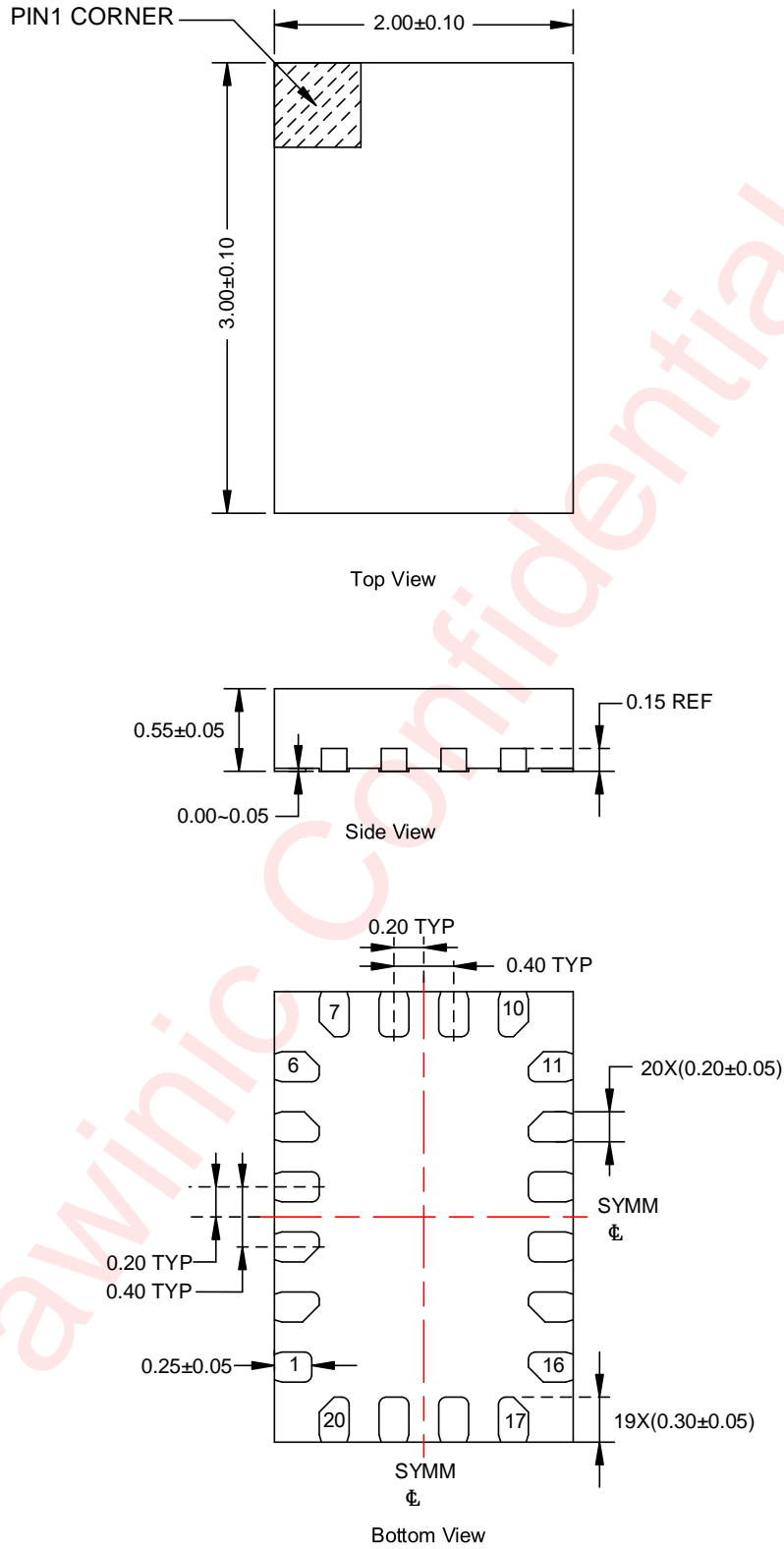
Figure 25 AW8838 External Components Placement

LAYOUT CONSIDERATIONS

In order to exploit best performance of AW8838, PCB layout must be carefully considered. A recommended PCB layout is illustrated as Figure 24 shown. Design consideration should be followed as below:

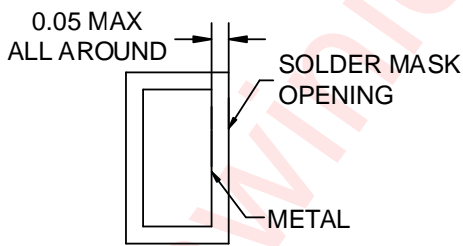
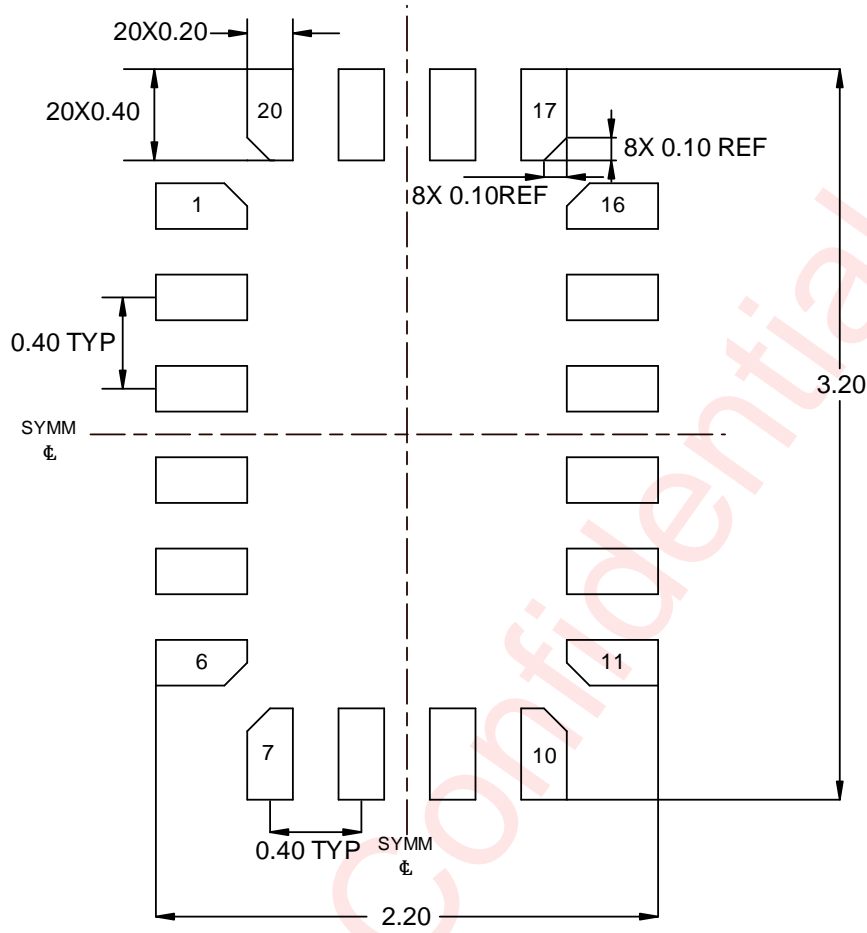
1. Isolated, short and wide power lines for both VDD pin and GND pin are required for better driving-capability of AW8838. The copper width is recommended to be larger than 0.75mm (30mil). Power supply decoupling capacitors should be placed as close as possible to power supply pins.
2. Flying capacitors C_{F1} , C_{F2} should be placed as close as possible to C1N, C1P pins and C2N, C2P pins. Likewise, capacitor C_{OUT} should be close to PVDD pin. The trace from C_{OUT} to both PVDD pin and GND pin should be short and wide.
3. Ferrite beads and filter capacitors should be close to VON and VOP pins. The trace from output pins to speaker should be short and wide. The copper width is recommended to be larger than 0.5mm (20mil).

PACKAGE DESCRIPTION

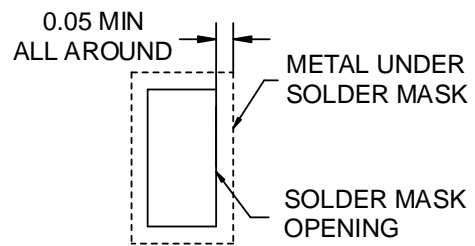


Unit : mm

LAND PATTERN DATA



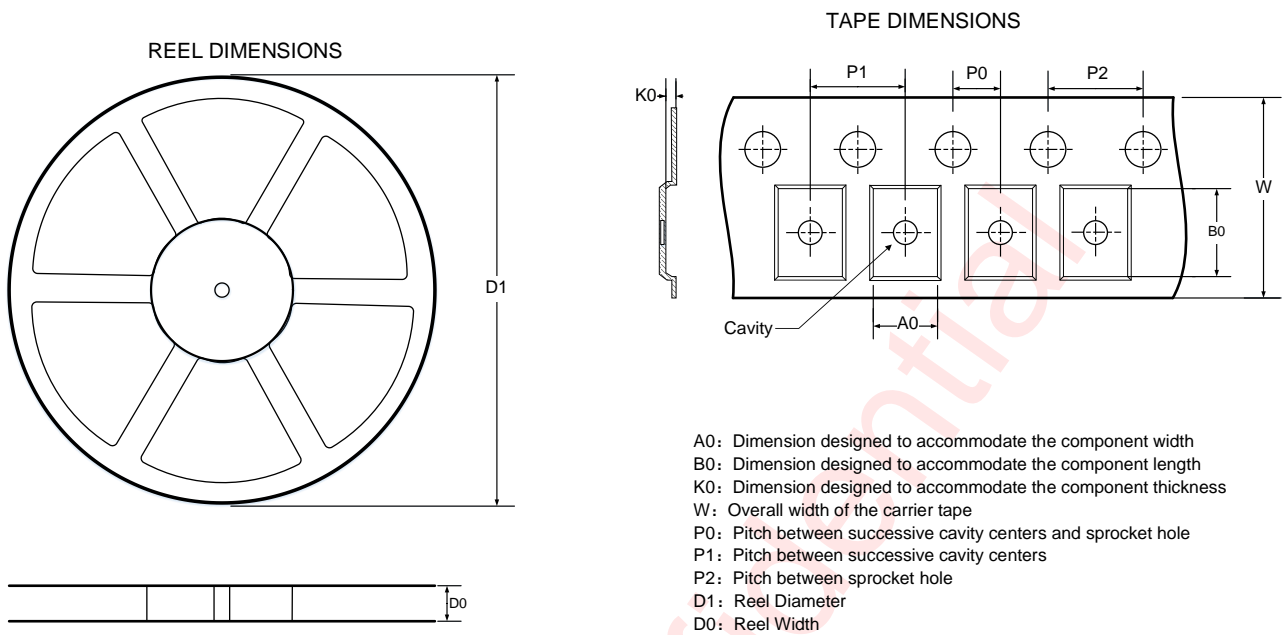
NON-SOLDER MASK DEFINED



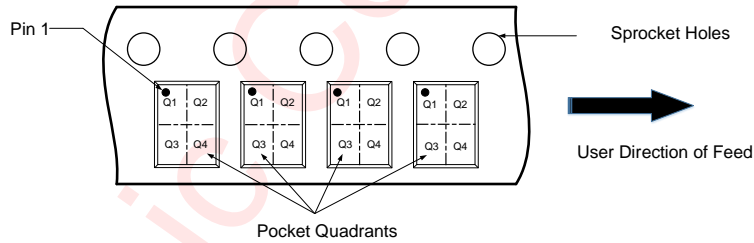
SOLDER MASK DEFINED

Unit: mm

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All Dimensions are nominal

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---------|---------|---------|---------|---------|---------|---------|---------|--------|---------------|
| 330 | 12.4 | 2.3 | 3.3 | 0.75 | 2 | 4 | 4 | 12 | Q1 |

REVISION HISTORY

| Vision | Date | Change Record |
|--------|--------------|---|
| V1.0 | August 2018 | Officially Released |
| V1.1 | January 2019 | Updated Package Description and Land Pattern Data |
| V1.2 | January 2019 | Updated Package Information |
| V1.3 | March 2019 | Updated Power-up and Power-down Sequence |
| V1.4 | July 2019 | Updated Land Pattern Data |
| V1.5 | July 2020 | Updated Registers |
| V1.6 | July 2023 | Updated I ² C Address Information |

awinic Confidential

DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.