1. Description

The XinJi Technology Micro-Point-of-Load (µPOL) XPC0126x and XPC1126x are very efficient, high-frequency DC-DC voltage regulators. Operating up to 10MHz or 8MHz respectively, they allow the use of small external components in both value and footprint. Different versions are available with a fixed output voltage between 1.2V and 3.3V, delivered from an input voltage supply of 2.3V to 5.5V.

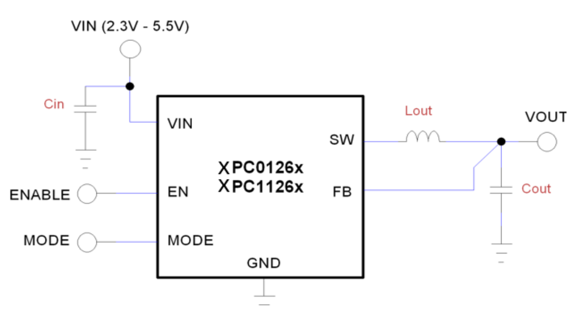
At medium and light current loads, the regulators will automatically enter Pulse Frequency Modulation (PFM) operation mode for best possible efficiency over the entire range of load currents. A low quiescent current of only 18µA enables high efficiency even with exceptionally light loads. If PFM mode is not desired, the MODE pin can be used to force fixed frequency operation (PWM) and disable PFM mode.

The µPOL comes in a 6-pin WLCSP package with 400µm pin pitch and a 1.2 x 0.9 x 0.6 mm size.

2. Applications

- Cellular Phones
- Tablets
- Wireless Data Cards
- Embedded Power Supply
- Wearables
- IoT

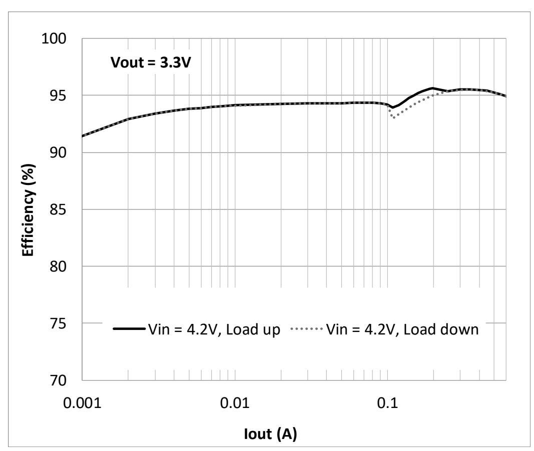
Figure 1. Typical Application Circuit



3. Features

- 600mA Output Current
- Up to 10MHz or 8MHz Switching Frequency
- PFM Light Load Operation
- 18uA Quiescent Current
- 95% Peak Efficiency
- 2.3V to 5.5V Input Voltage Range
- 1.2V to 3.3V Fixed Output Voltage
- Fast Load Transient Response
- 100% Duty Cycle
- Logic Enable Input
- Soft-Start
- Input Under-Voltage Lockout
- Thermal Shutdown
- Overload Protection
- Output Discharge
- Current Limit
- Small External 0.47µH Inductor
- EU RoHS Compliant, Pb Free

Figure 2. Efficiency vs Load Current, Mode = Auto



Contents

4. Product Family Table and Ordering information

Table 1. List of parts

Family	Part Number	Frequency (MHz)	VOUT (V)	Package Marking	MPQ
XPC0126x	XPC0126E	10	1.8	0126E	3,000
	XPC0126F	10	2.1	0126F	3,000
XPC1126x	XPC1126A	6.5	1.2	1126A	3,000
	XPC1126B	6.5	1.35	1126B	3,000
	XPC1126C	8	1.5	1126C	3,000
	XPC1126D	8	1.6	1126D	3,000
	XPC1126E	8	1.8	1126E	3,000
	XPC1126F	8	2.1	1126F	3,000
	XPC1126L	8	2.4	1126L	3,000
	XPC1126G	8	2.5	1126G	3,000
	XPC1126K	8	3.3	1126K	3,000

MPQ = Minimum Packing Quantity. For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

5. PIN Configuration and Description

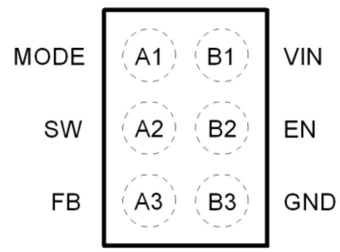


Figure 3. Top View

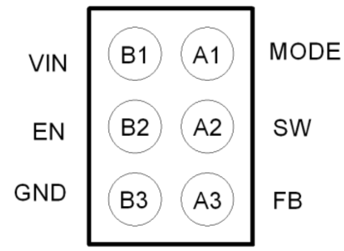


Figure 4. Bottom View

Table 2. Pin Definition

Pin	Name	Description
A1	MODE	MODE = LOW: Allows the regulator to automatically switch between pulse frequency modulation (PFM) at light current loads and pulse width modulation (PWM) at high current loads. MODE = HIGH: Forces the regulator to stay in PWM mode.
B1	VIN	Power supply input. Connect to power source.
A2	SW	Switching node. Connect to the output inductor.
B2	EN	Enable. Part is active when EN > 1.2V. Part is disabled when EN < 1.07V. Do not leave this pin floating.
A3	FB	Feedback input. Connect to output voltage.
B3	GND	Ground pin.

6. Absolute Maximum Ratings

Table 3. Maximum Ratings[1]

Parameter	Min	Max	Units
DC Supply Voltage, VIN	-0.3	6	V
Voltage on other pins, MODE, SW, FB, EN	-0.3	V_{IN} + 0.3	V
Storage Temperature Range	-40	+150	°C
Junction Temperature	-40	+150	°C
Electrostatic Discharge (HBM)	-4000	4000	V
Electrostatic Discharge (CDM)	-2000	2000	V

7. Recommended Operating Conditions

Table 4. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{IN}	2.3		5.5[2]	V
Output Current	I_{OUT}	0		0.6	A
Output Inductor	L	220	470	2200	nH
Input Capacitor	C_{IN}	2.2	4.7		µF
Output Capacitor	C_{OUT}	2.2	4.7		µF
Operating Temperature, Ambient	T_{OA}	-40		+85	°C
Operating Temperature, Junction	T_{OJ}	-40		+125	°C

Table 5. Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance to JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	130	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	33	°C/W

[1] Operation of the device outside of these parameters may cause permanent damage.
[2] Vin above 5.5V over extended periods may affect device reliability.

8. Electrical Specifications

Typical values unless otherwise noted: V_{IN} = 3.6V, V_{OUT} = 1.8V, MODE = 0V, Temp = +25°C
Maximum and minimum values are: V_{IN} = EN = 2.3V to 5.5V, $T_{AMBIENT}$ = -40 to +85˚C
Circuit of **Figure 1** unless otherwise noted.

Table 6. DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	V_{IN}		2.3		5.5	V
Quiescent Current	I_Q	PWM Mode		6.5		mA
		No Load, Not Switching		18		µA
Shutdown Current	I_{SHDN}	EN = GND		0.1	1	µA
Under-Voltage Lockout Threshold	V_{UVLO}	Rising V_{IN}		2.0	2.25	V
Under-Voltage Lockout Hysteresis	$V_{UVLOHYST}$			150		mV
Thermal Shutdown	T_{TSD}			135		°C
Thermal Shutdown Hysteresis	T_{HYST}			15		°C

Table 7. Output Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Switching Frequency	F_{SW}	CPC1126A		6.5		MHz
		CPC1126 Family		8		
		CPC0126 Family		10		
Output Voltage Accuracy	V_{OUT}	I_{LOAD} = 0 to 1A, Vin = 5.5V max	-2%	V_{OUT}	+2%	V
		PWM Mode, Vin = 5.5V max	-1.5%	V_{OUT}	+1.5%	V
Soft-Start Time	T_{SS}			280		µs
Enable Turn On Delay	T_{EN}			100		µs
PMOS On Resistance	R_{DSONP}	V_{IN} = V_{GS} = 3.6V		148		mΩ
NMOS On Resistance	R_{DSONN}	V_{IN} = V_{GS} = 3.6V		77		mΩ
PMOS Peak Current Limit	I_{LIM}	V_{IN} = 3.6V, Open Loop		960		mA
Output Discharge Resistance	R_{DIS}	EN = 0V		17		Ω

Table 8. Logic inputs: EN and Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Logic High Voltage	V_{IH}		1.2			V
Logic Low Voltage	V_{IL}				1.07	V
Logic Pin Leakage Current	I_{LPIN}				1	µA
Logic Input Hysteresis	V_{LHYST}			130		mV

9. Typical Performance and Operating Characteristics

Typical test conditions unless otherwise noted: circuit of **Figure 1**, V_{IN} = 3.6V, V_{OUT} = 1.8V, f_{SW} = 10MHz for 1.8V devices, f_{SW} = 6.5MHz for 1.2V and f_{SW} = 8MHz for 3.3V devices, MODE = 0V, Temp = +25°C.

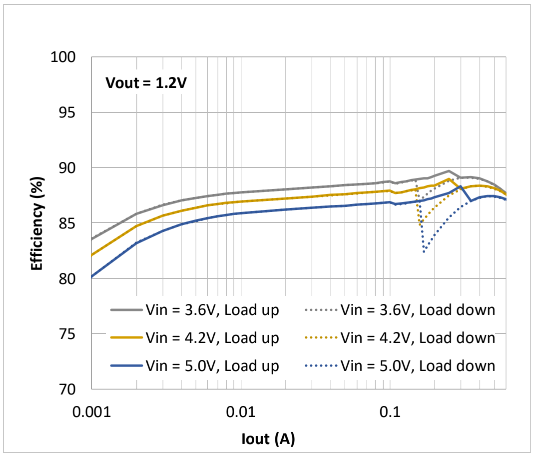


Figure 5. Efficiency vs I_{LOAD}, PFM/PWM, V_{OUT} = 1.2V

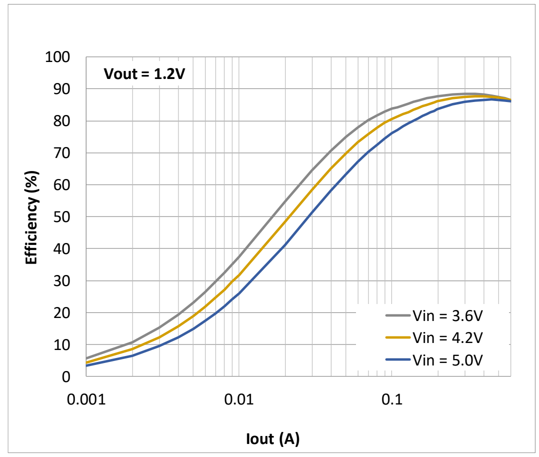


Figure 6. Efficiency vs I_{LOAD}, PWM, V_{OUT} = 1.2V

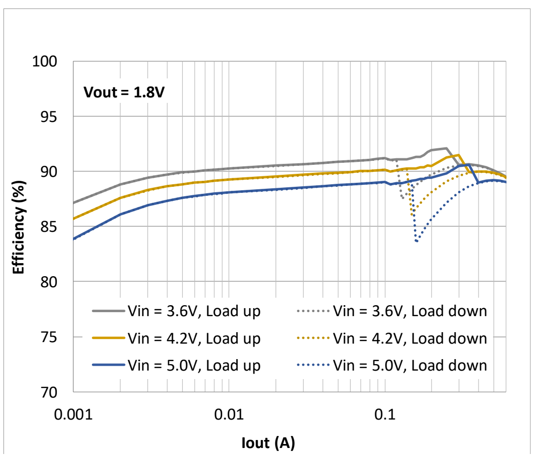


Figure 7. Efficiency vs I_{LOAD}, PFM/PWM, V_{OUT} = 1.8V

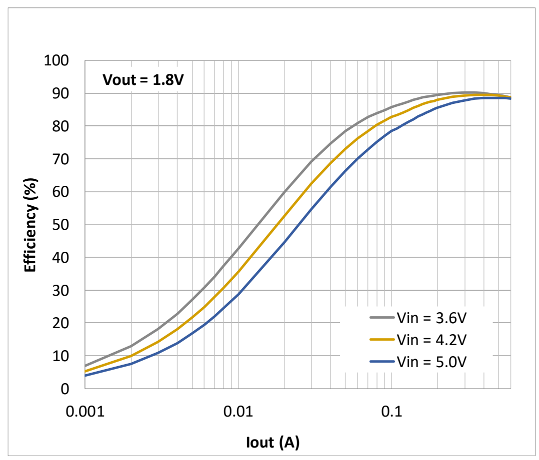


Figure 8. Efficiency vs I_{LOAD}, PWM, V_{OUT} = 1.8V

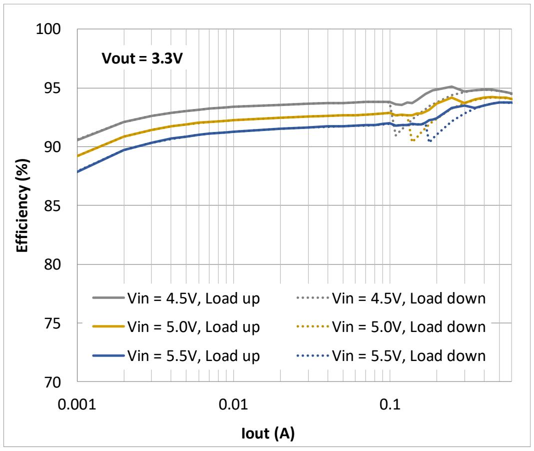


Figure 9. Efficiency vs I_{LOAD}, PFM/PWM, V_{OUT} = 3.3V

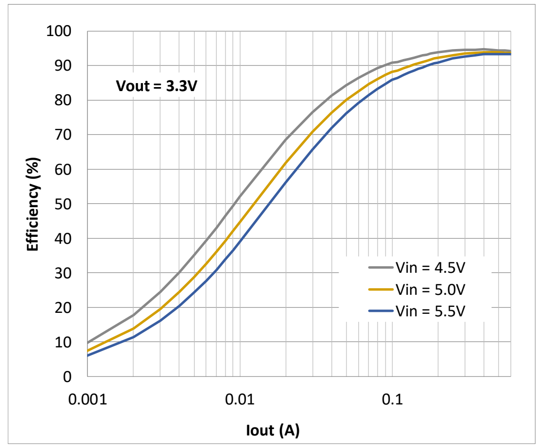


Figure 10. Efficiency vs I_{LOAD}, PWM, V_{OUT} = 3.3V

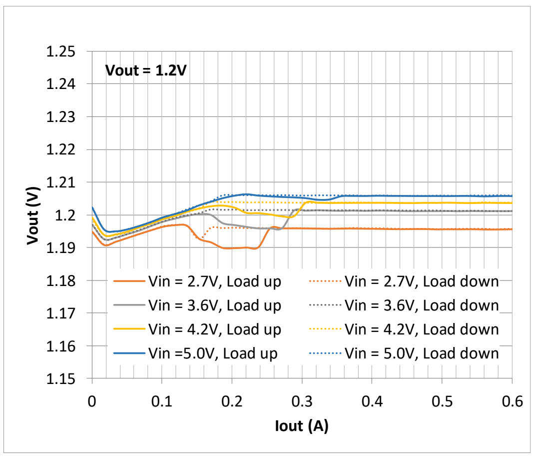


Figure 11. V_{OUT} vs I_{LOAD}, PFM/PWM, V_{OUT} = 1.2V

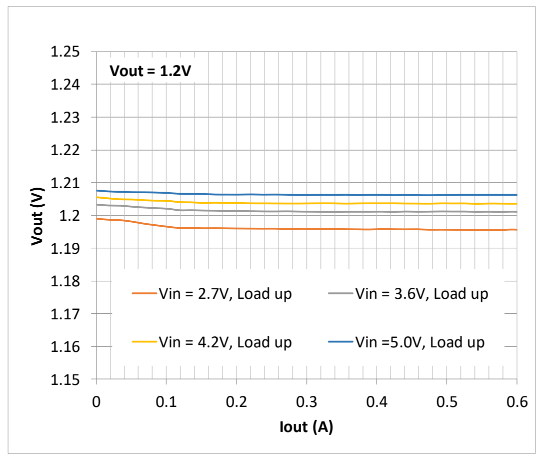


Figure 12. V_{OUT} vs I_{LOAD}, PWM, V_{OUT} = 1.2V

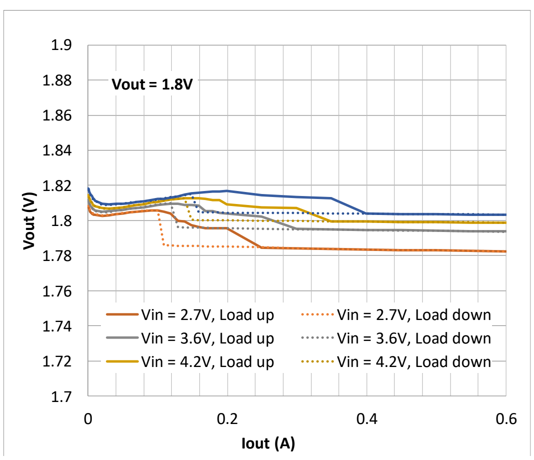


Figure 13. V_{OUT} vs I_{LOAD}, PFM/PWM, V_{OUT} = 1.8V

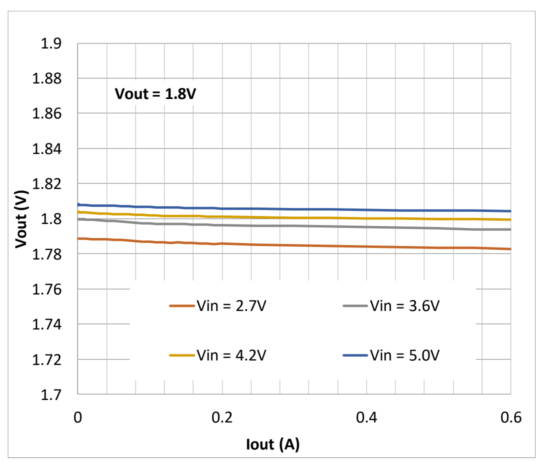


Figure 14. V_{OUT} vs I_{LOAD}, PWM, V_{OUT} = 1.8V

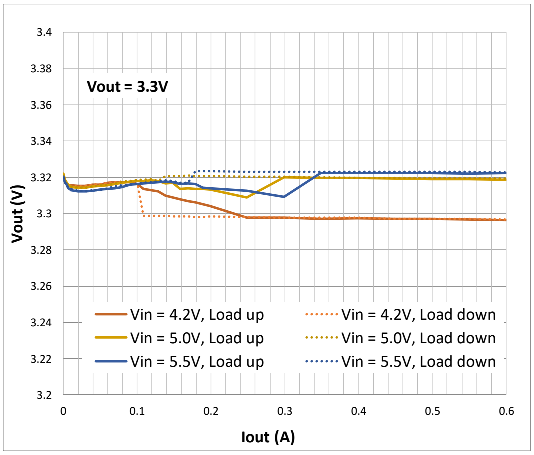


Figure 15. V_{OUT} vs I_{LOAD}, PFM/PWM, V_{OUT} = 3.3V

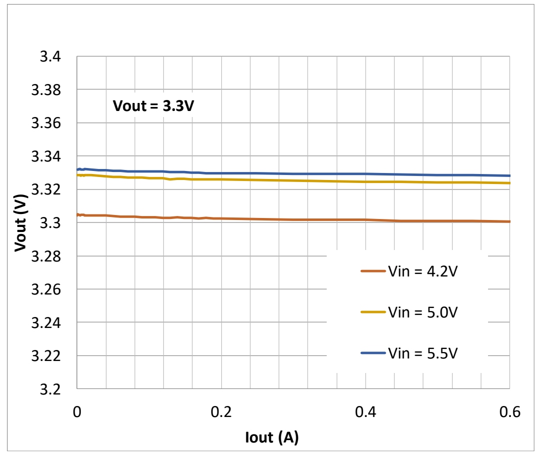


Figure 16. V_{OUT} vs I_{LOAD}, PWM, V_{OUT} = 3.3V

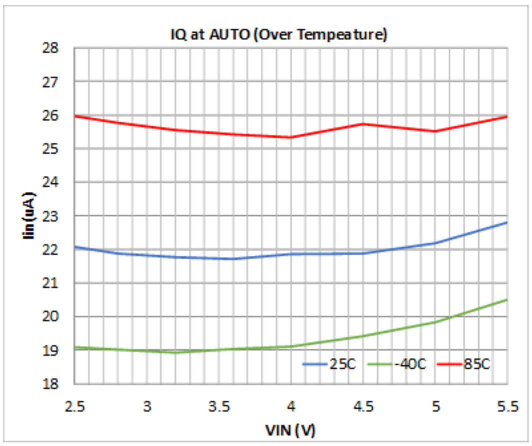


Figure 17. I_Q vs V_{IN} over Temperature, Auto Mode (Vout=1.8V)

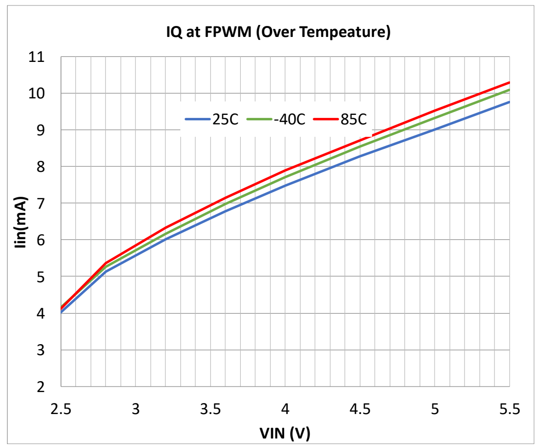


Figure 18. I_Q vs V_{IN} over Temperature, PWM, (Vout=1.8V)

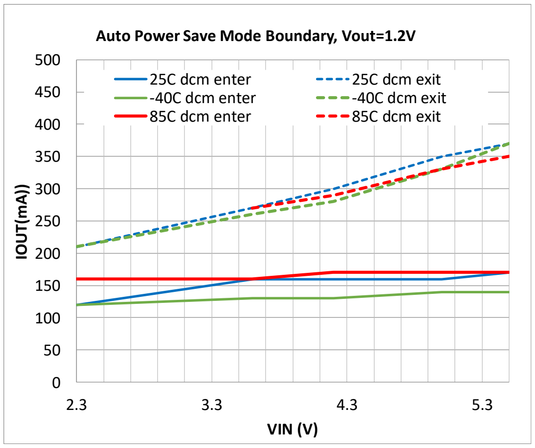


Figure 19. PFM/PWM Boundaries, V_{OUT} = 1.2V

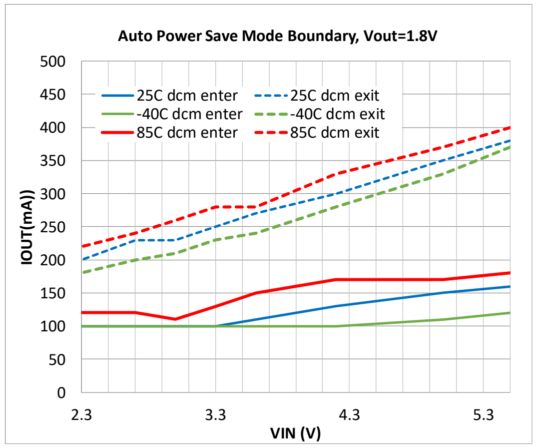


Figure 20. PFM/PWM Boundaries, V_{OUT} = 1.8V

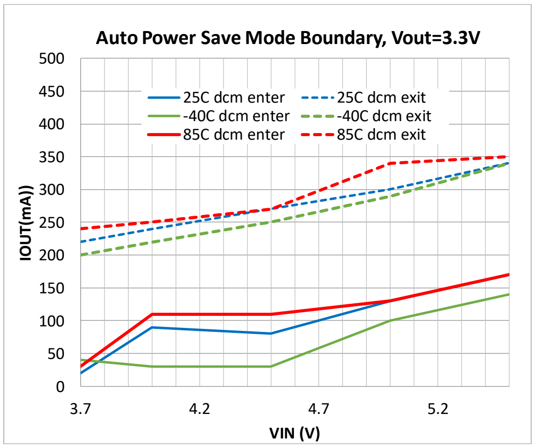


Figure 21. PFM/PWM Boundaries, V_{OUT} = 3.3V

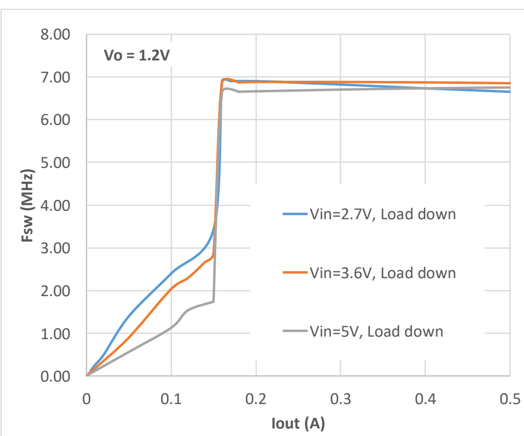


Figure 22. FSW, V_{OUT} = 1.2V, Auto

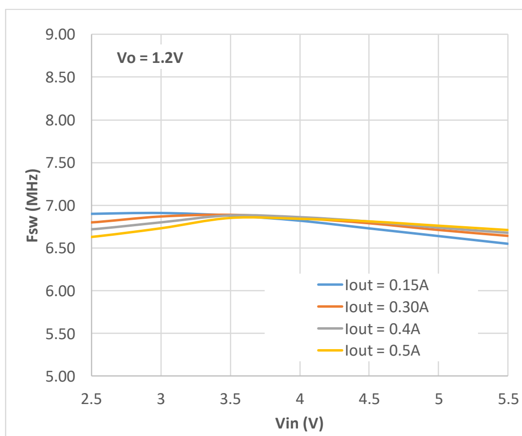


Figure 23. FSW, V_{OUT} = 1.2V, Forced PWM

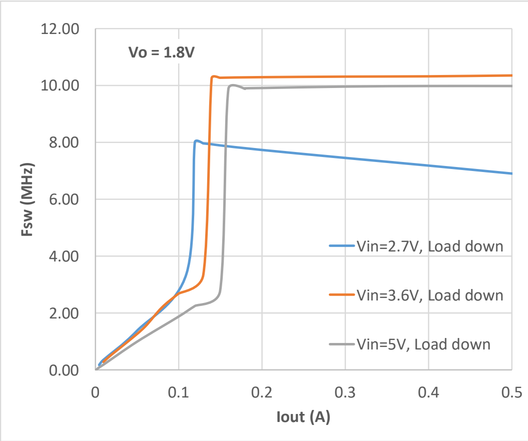


Figure 24. F_{SW}, V_{OUT} = 1.8V, Auto

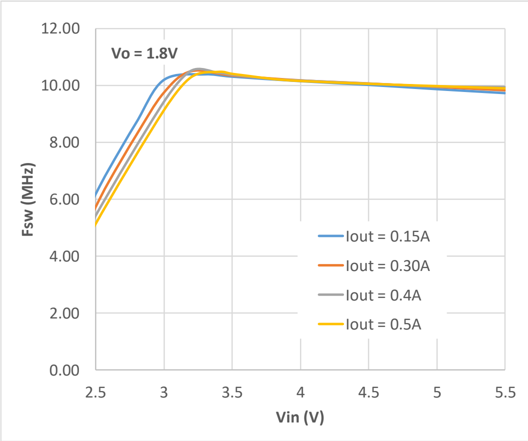


Figure 25. F_{SW}, V_{OUT} = 1.8V, Forced PWM

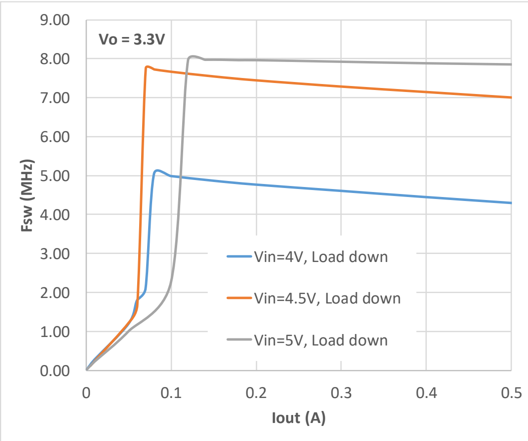


Figure 26. F_{SW}, V_{OUT} = 3.3V, Auto

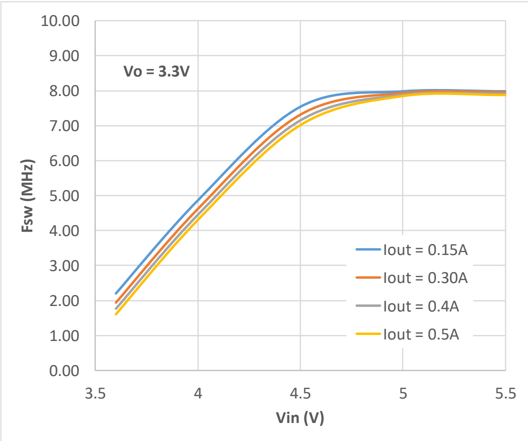


Figure 27. F_{SW}, V_{OUT} = 3.3V, Forced PWM

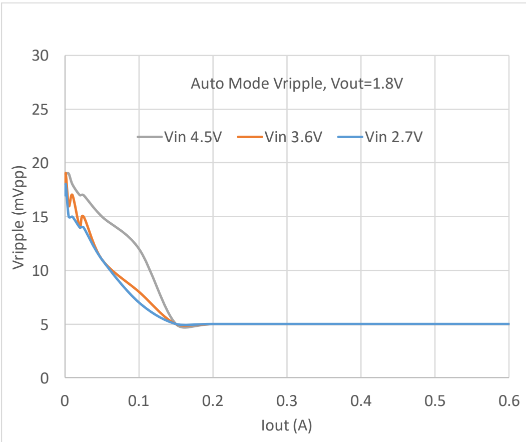


Figure 28. Peak to Peak Output Voltage Ripple vs Load Current, V_{OUT} = 1.8V, Auto

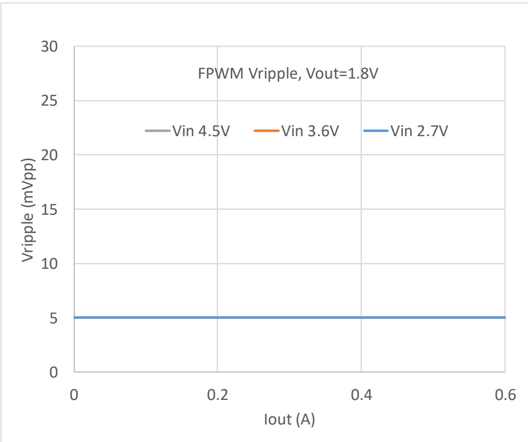


Figure 29. Peak to Peak Output Voltage Ripple vs Load Current, V_{OUT} = 1.8V, Forced PWM

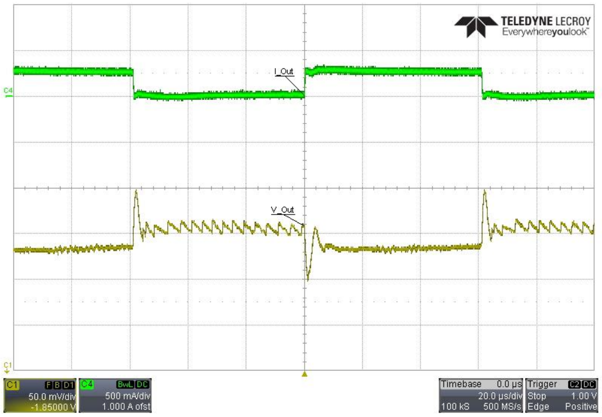


Figure 30. Load Transient Response in PFM/PWM
V_{IN}=3.6V, V_{OUT} = 1.8V, I_{LOAD} = 10 to 310 mA Step

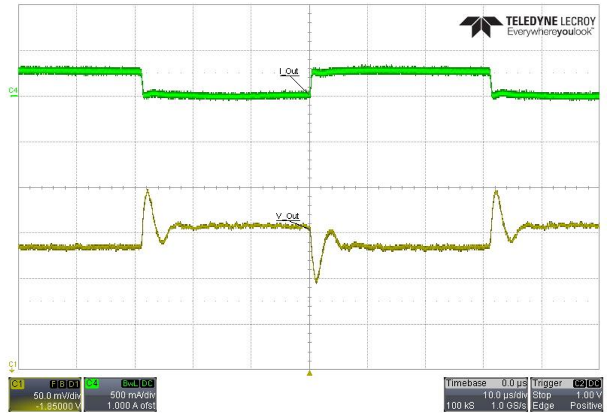


Figure 31. Load Transient Response in PWM/PWM
V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{LOAD} = 10 to 310 mA Step

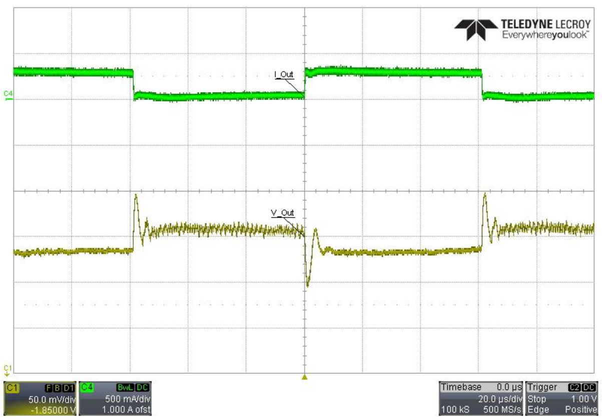


Figure 32. Load Transient Response in PWM/PWM
V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{LOAD} = 50 to 350 mA Step

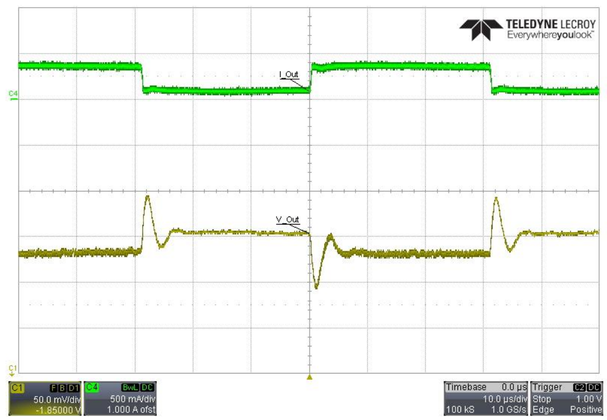


Figure 33. Load Transient Response in PWM/PWM
V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{LOAD} = 150 to 450 mA Step

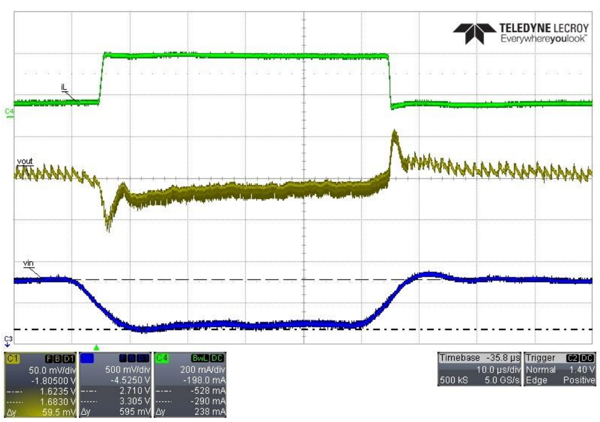


Figure 34. Figure 25 Combined Line/Load Transient
V_{IN} = 2.7 to 3.3V Step, I_{LOAD} = 30 to 300mA Step

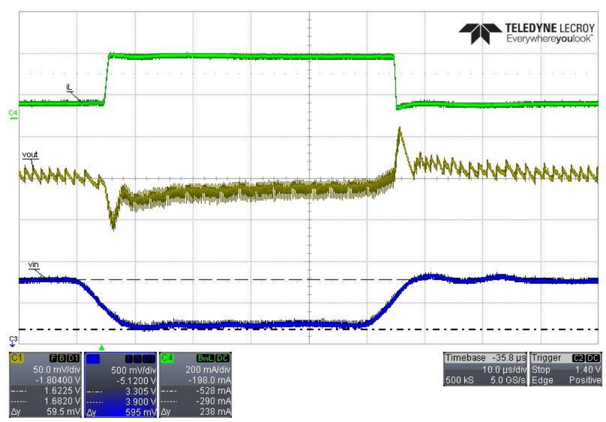


Figure 35. Combined Line/Load Transient Response: V_{IN} = 3.3 to 3.9V Step, I_{LOAD} = 10 to 400mA Step

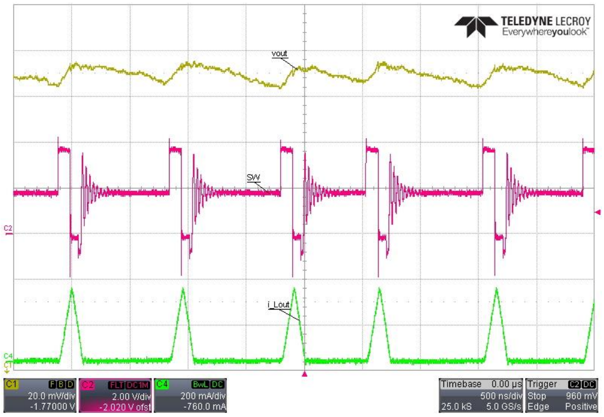


Figure 36. Typical Power Save Mode Operation: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{LOAD} = 40mA

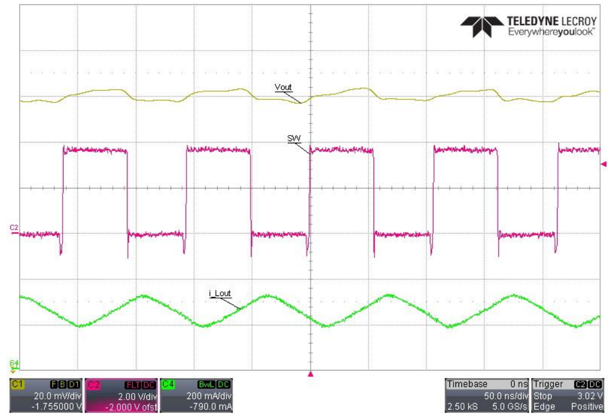


Figure 37. Typical PWM Mode Operation: V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{LOAD} = 300mA

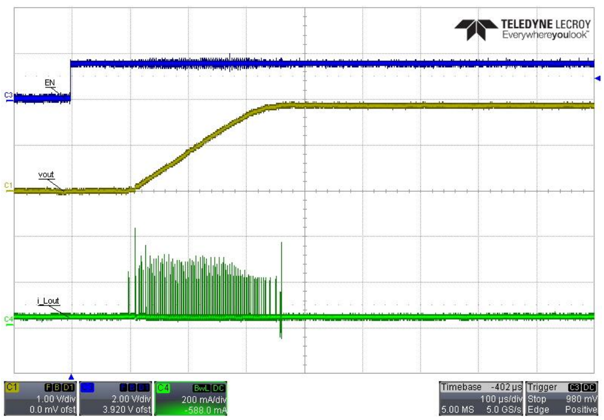


Figure 38. Start-Up: MODE = Low, V_{IN} = 3.6V, V_{OUT} = 1.8V, No load

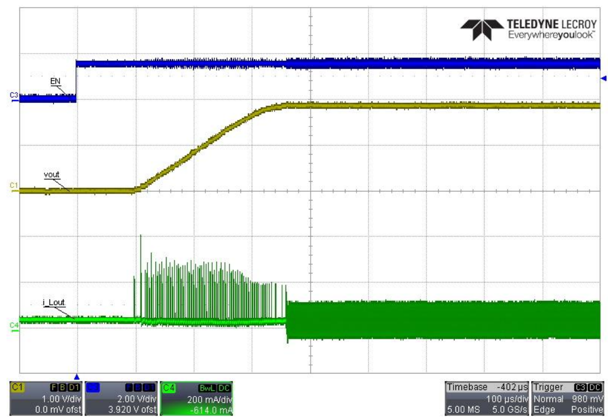


Figure 39. Start-Up: MODE = High, V_{IN} = 3.6V, V_{OUT} = 1.8V, No load

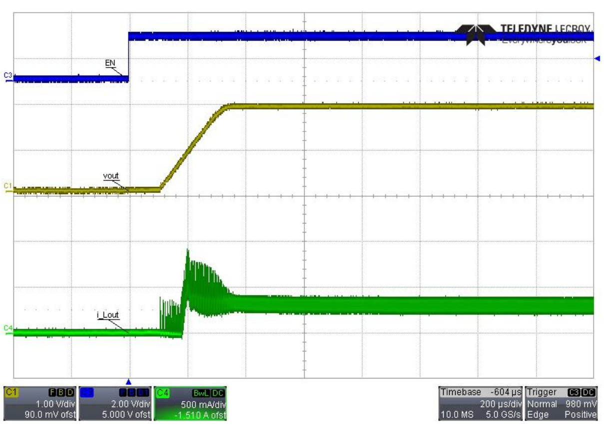


Figure 40. Shut-Down: MODE = Low, V_{IN} = 3.6V, V_{OUT} = 1.8 V, 0.6A load

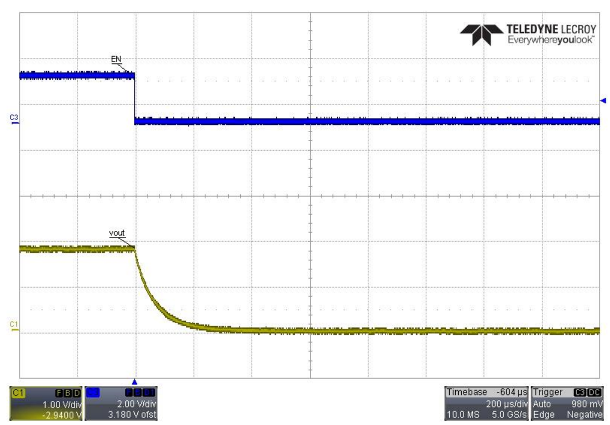


Figure 41. Shut-Down: MODE = High, V_{IN} = 3.6V, V_{OUT} = 1.8 V, No load

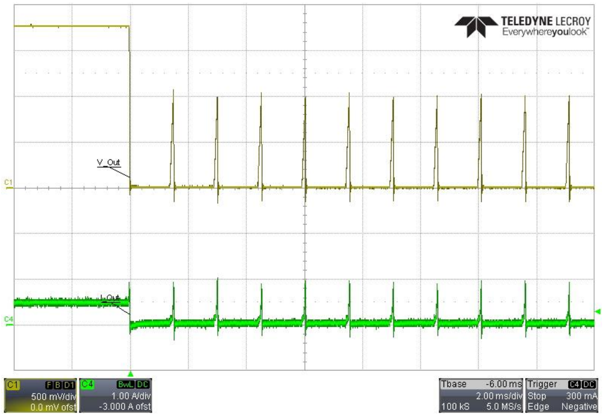


Figure 42. OCP hiccup: V_{IN} = 3.6V, V_{OUT} = 1.8V

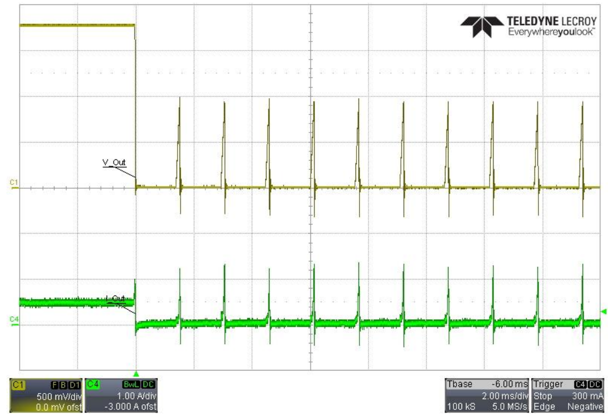
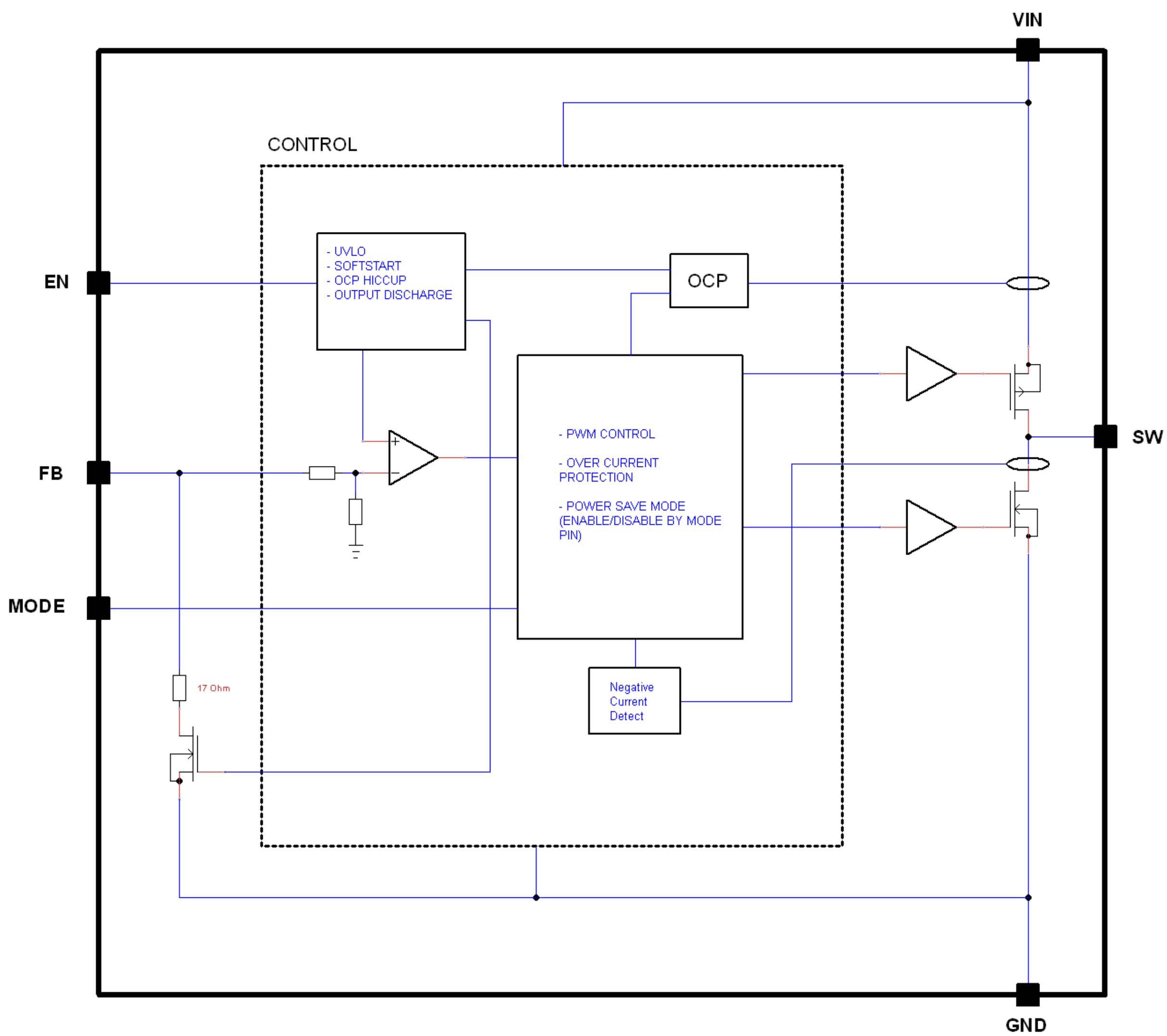


Figure 43. OCP hiccup: V_{IN} = 5.5V, V_{OUT} = 1.8V

10. Functional Description

The XP0126x and XP1126x family of parts are synchronous DC/DC voltage regulators available with switching frequencies up to 8MHz or 10MHz, respectively. Operating from an input voltage between 2.3V and 5.5V the regulator can deliver up to 600mA of load current at a fixed output voltage.

Figure 44. Block Diagram



Enable

Setting the EN voltage to logic level High enables the device. Alternatively, the device is disabled when the EN voltage is set to logic level Low. In this state the IC draws less than 1µA of current and the output is pulled to ground through a resistive load (R_{DS}). V_{OUT} starts to ramp up after 100µs delay.

Under voltage Lockout (UVLO)

The under-voltage lockout feature prevents the device from turning on if V_{IN} is below the UVLO level of 2.0V. If the device is enabled under UVLO conditions, the circuitry will not turn on until the input voltage is increased. Once active, the UVLO circuit has 150mV of hysteresis and the device will turn off if V_{IN} drops below 1.85V.

Soft-Start

When the device is enabled, internal soft-start circuitry causes V_{OUT} to ramp up over a period of 280µs to limit inrush current. This feature protects a high impedance source from being pulled to a lower voltage as the device turns on.

Active Output Discharge

When the device is disabled through the EN pin, a discharge path for the output capacitor is created between V_{OUT} and ground through a 17 Ohm resistor (R_{DS}).

Modes of Operation

The MODE pin selects the device’s mode of operation. When connected to logic High, the converter always operates in pulse width modulation (PWM) mode regardless of load current. PWM is a continuous switching mode where the duty cycle is modulated to achieve the required output power.

When connected to logic Low, the converter automatically switches to pulse frequency modulation (PFM) operation at light current loads. In PFM mode the frequency of pulses is varied to deliver the best possible efficiency. The device switches between PFM and PWM as the load current changes and thus optimizes performance.

If the input voltage ever gets too close to the target output voltage, such that regulation can no longer be maintained, the regulator will enter 100% duty cycle mode. In this mode the high side switch is ON, connecting the input and output together to deliver a voltage as close to the target as possible.

Overcurrent Protection

The device has overcurrent protection to prevent damage to the device and inductor during overcurrent conditions.

Peak current protection occurs at 960mA. After hitting 16 consecutive cycles of peak current limit, the output will be disabled. After being disabled for 1.5ms, the device will be re-enabled, and a new soft-start cycle will begin.

Thermal Shutdown

The device thermal shutdown protection is enabled if the chip temperature exceeds 135°C. Once the temperature drops below 120°C, the device will be re-enabled, and a new soft-start cycle will begin.

11. Typical Application

Figure 45. Application Circuit

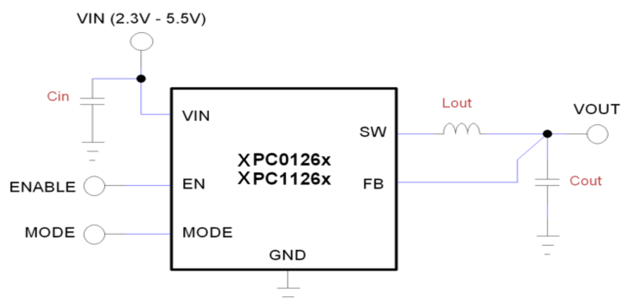


Table 9 Recommended Components

Part	Value	Package	Manufacturer	Part Number
C1	4.7uF, 10V	0402	AVX	0402ZD475MATA2A
	2.2uF, 10V	0402	AVX	0402ZD225MATA2A
C2	4.7uF, 10V	0402	AVX	0402ZD475MATA2A
	2.2uF, 10V	0402	AVX	0402ZD225MATA2A
L1	470nH, DCR 54mΩ	1.6mm x 1.0mm x 0.8mm	Murata	DFE18SANR47MG0L
	470nH, DCR 32mΩ	2.0mm x 1.6mm x 1.0mm	Murata	DFE201610ER47M
	470nH, DCR 40mΩ	2.0mm x 1.6mm x 1.0mm	FDK	MIPSZ2016DR47FR
	470nH, DCR 125mΩ	1.6mm x 0.8mm x 0.6mm	Cyntec	16010F100E
	470nH, DCR 80mΩ	2.0mm × 1.2mm × 1.0mm	Sunlord	MPH201210QR47MT

12. Layout Guidelines and Example

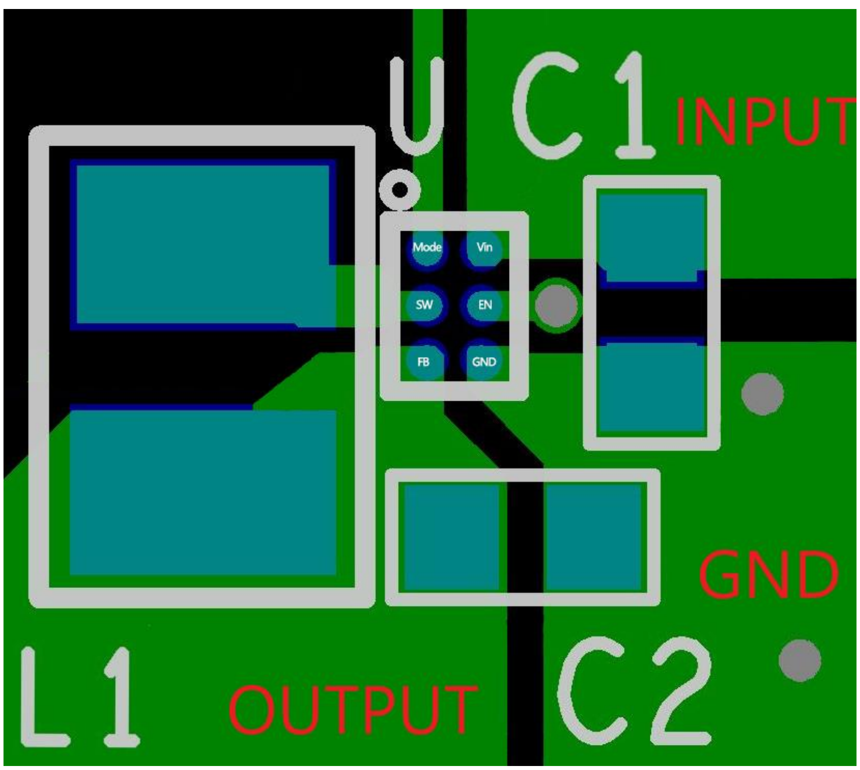
A well-designed and manufactured PCB is important for all switching power supplies, especially for those operate at high switching frequency.

If the layout is not fulfilled carefully, not only regulator performance could be degraded but also stability or EMI issue may be introduced. Hence, care must be taken in board layout to achieve the specified performance.

Please use the following guidelines when designing PCBs:

1) Keep components placement as compact as possible.
2) Place a low-ESR input capacitor as close to VIN and GND as possible.
3) Minimize the area between SW pin trace and inductor to limit high frequency radiation.
4) Keep FB trace away from noisy components and traces (e.g., SW and inductor).
5) Use wide and short traces for the main current paths.
6) Ground pins of regulator must be strongly connected to PCB ground with low inductance and impedance.
7) Place common and unbroken ground for CIN and COUT.
8) Reduce excessive thermal relief vias and keep them away from SW and inductor.

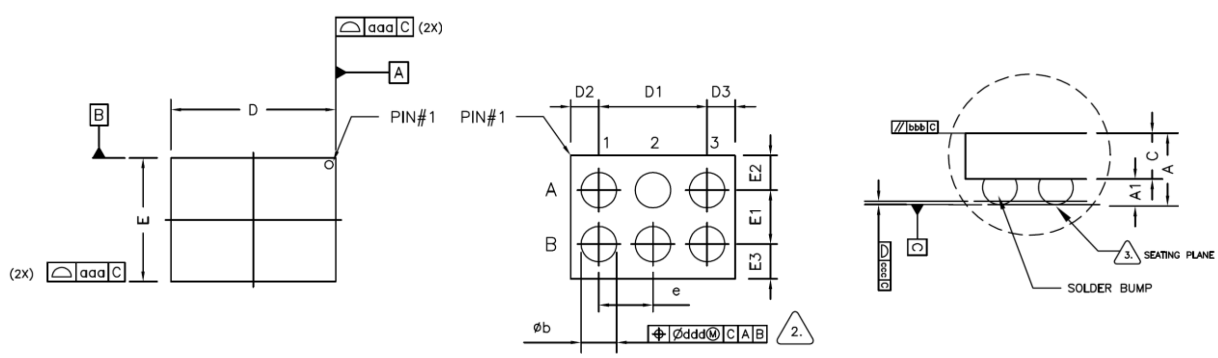
Figure 46 Layout Top Layer



13. Physical Dimensions

Table 10. Chip Dimensions

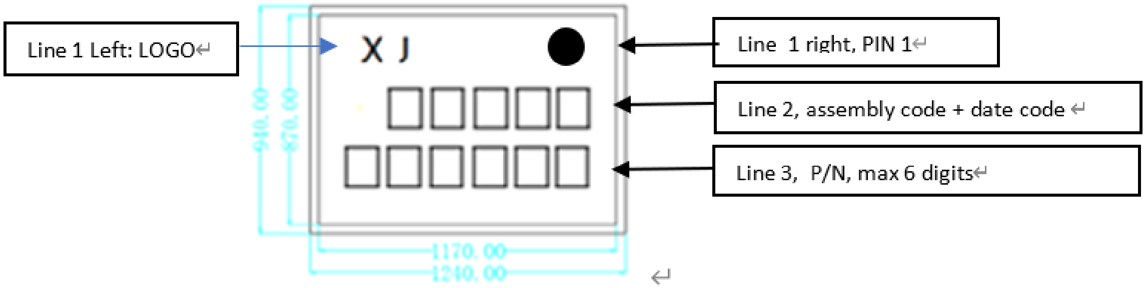
Symbol	Dimensions in mm			Dimensions in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.5364	0.5820	0.6276	0.0211	0.0229	0.0247
A1	0.1818	0.2020	0.2222	0.0072	0.0080	0.0087
C	0.3546	0.3800	0.4054	0.0140	0.0150	0.0160
D	1.1600		1.2400	0.0457		0.0488
E	0.8600		0.9400	0.0339		0.0370
B	0.2227	0.2620	0.3013	0.0088	0.0103	0.0119
D1		0.8000			0.0315	
D2		0.2080			0.0082	
D3		0.2080			0.0082	
E1		0.4000			0.0157	
E2		0.2580			0.0102	
E3		0.2580			0.0102	
E		0.4000			0.0157	
aaa		0.100			0.00394	
bbb		0.100			0.00394	
ccc		0.030			0.00118	
ddd		0.050			0.01969	



TOP(Marking) VIEW

BOTTOM(bump) VIEW

14. Top Marking



15. Package Material Information

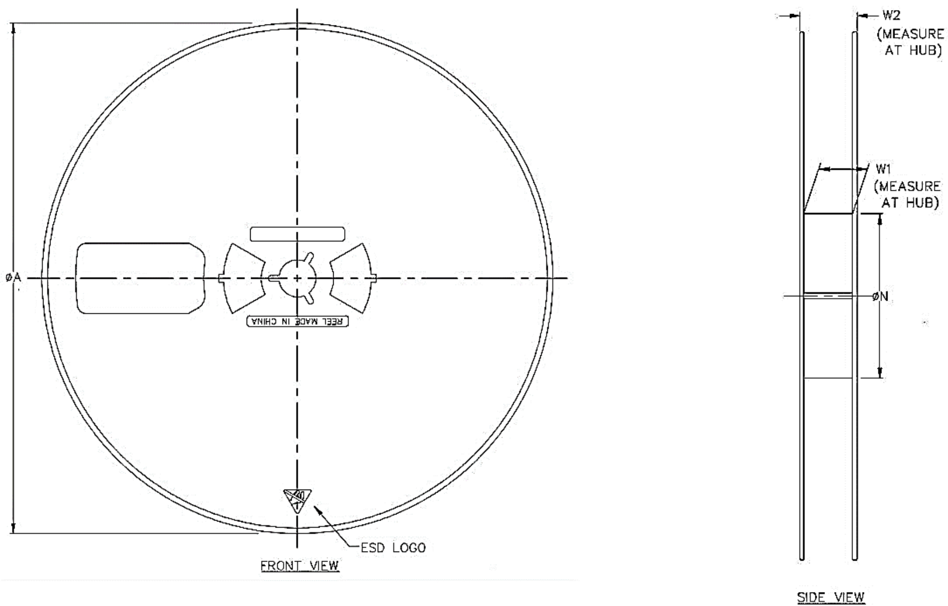


Table 11. Reel Dimensions

Tape Width	ØA	ØN	W1	W2
8.0 mm	178.0 mm	54.0 mm	9.5 mm	15 mm (max)

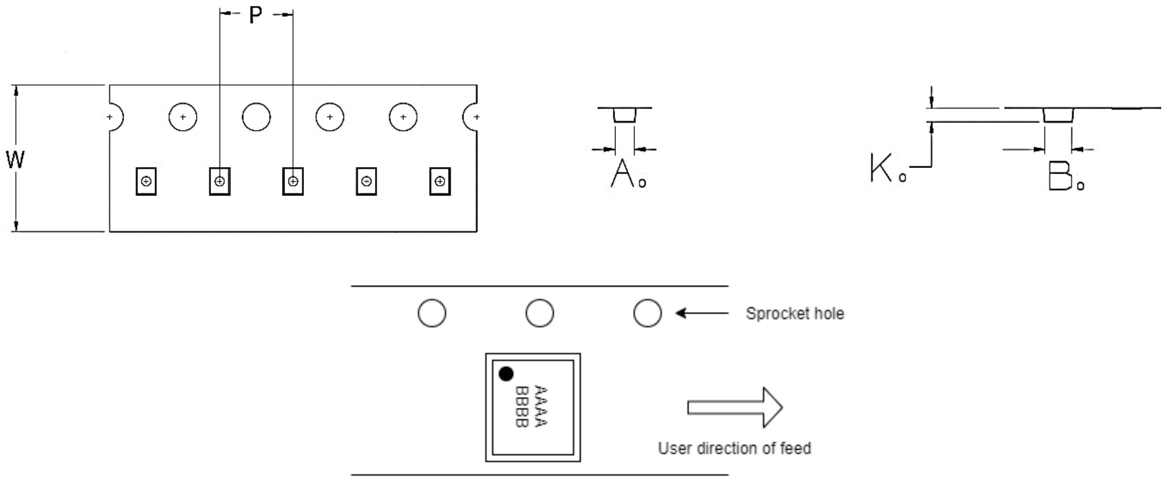


Table 12. Carrier Tape Dimensions

Symbol	Description	Value (mm)
W	Carrier tape overall width	8.00
P	Pitch between successive cavity centers	4.00
A0	Cavity dimension designed to accommodate the component width	0.99
B0	Cavity dimension designed to accommodate the component length	1.38
K0	Cavity dimension designed to accommodate the component thickness	0.69