8V High Efficiency, Low Noise, Constant Large Volume, Multi-Level AGC 8th-Generation Smart K Audio Amplifier

FEATURES

- Multi-Level AGC audio algorithm, effectively eliminates noise and makes sound smooth
- Adaptive DO-Charge pump technology：
  - Low Quiescent current：4mA@3.6V
- Output Power：2.3W@8Ω ;
- Low Noise：
  - RCV：7.5μV
  - SPK：28μV
- Low THD+N：0.02%
- Support high power receiver stereo application
- Support D speaker , D receiver 2-in-1 application
  - LRCV receiver：0dB，En=7.5μV，0.14W@THD+N=1%
  - SRCV receiver：0dB，En=9μV，0.55W@THD+N=1%
- Support 1.2V&1.8V logic I²C Control
- Over current protection, over-temperature protection and short-circuit protection
- Super TDD-Noise suppression
- Excellent pop-click suppression
- High PSRR：84dB
- FCQFN 2.5mmX2.0mmX0.55mm-15L package

APPLICATIONS

- **Smart phone、Tablet PC、Tactile feedback**

DESCRIPTION

AW87394 is specifically designed to improve the musical output dynamic range, enhance the overall sound quality, which is a new high efficiency, low noise, constant large volume, Smart K audio amplifier. AW87394 integrates awinic's proprietary Multi-Level AGC audio algorithm, effectively eliminating music noise and improving sound quality and volume. AW87394 integrated efficiency up to 92% of Adaptive DO-Charge pump technology, significantly improving the dynamic range of the music output and power consumption of audio system. AW87394 noise floor is as low as to 28μV at speaker mode, with 102dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.02% and unique Multi-Level AGC technology bring high quality music enjoyment.

AW87394 controls internal registers through the I²C interface. Register parameters include output voltage, power amplifier gain, Multi-Level AGC parameters etc.

AW87394 built-in over current protection, over temperature protection and short circuit protection function, effectively protect the chip. AW87394 features small FCQFN 2.5mmX2.0mmX0.55mm-15L package.

TYPICAL APPLICATION CIRCUIT

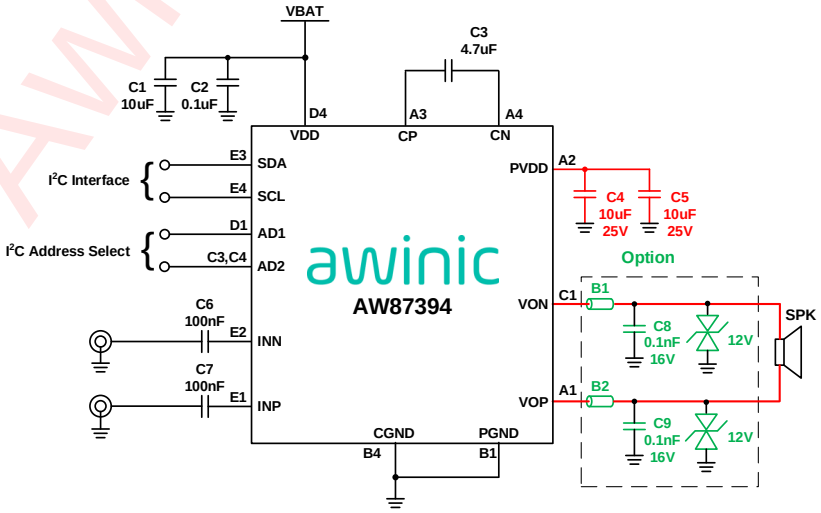
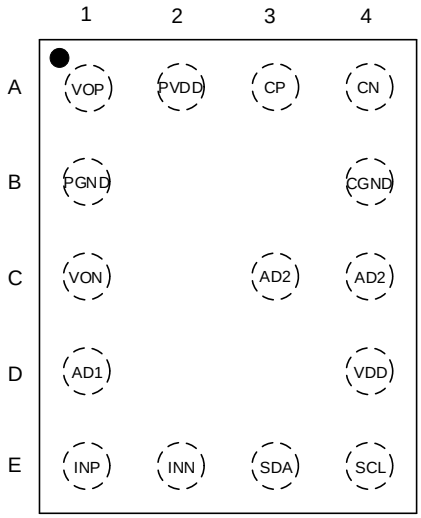


Figure 1　AW87394 Typical Application Diagram

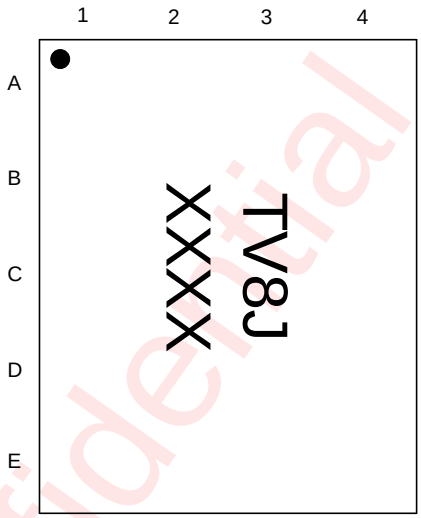
Note: Traces carry high current are marked in red in the above figure

PIN CONFIGURATION AND TOP MARK

AW87394FCR
(Top View)



AW87394FCR Marking
(Top View)



TV8J - AW87394FCR
XXXX - Production Tracing Code

Figure 2 AW87394 Pin configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
A1	VOP	Positive audio output terminal
A2	PVDD	Charge Pump output voltage
A3	CP	Positive input Charge Pump Flying Capacitance
A4	CN	Negative input Charge Pump Flying Capacitance
B1	PGND	Amplifier power ground
B4	CGND	Charge Pump power ground
C1	VON	Negative audio output terminal
C3,C4	AD2	I^2C address pin2
D1	AD1	I^2C address pin1
D4	VDD	Power supply
E1	INP	Positive audio input terminal
E2	INN	Negative audio input terminal
E3	SDA	I^2C-bus data input/output
E4	SCL	I^2C-bus clock input

FUNCTIONAL DIAGRAM

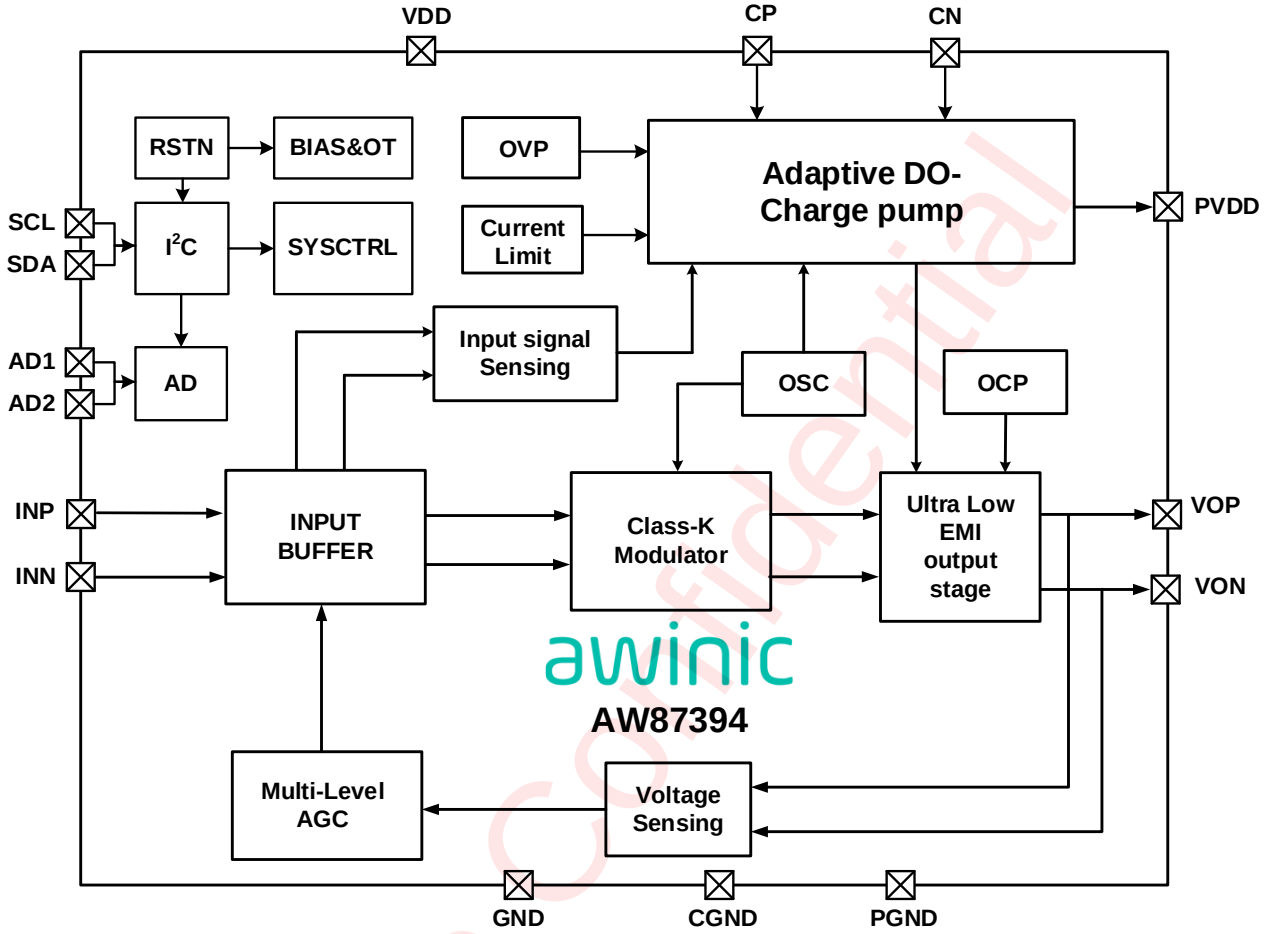


Figure 3 AW87394 Functional Diagram

Typical Application Circuits

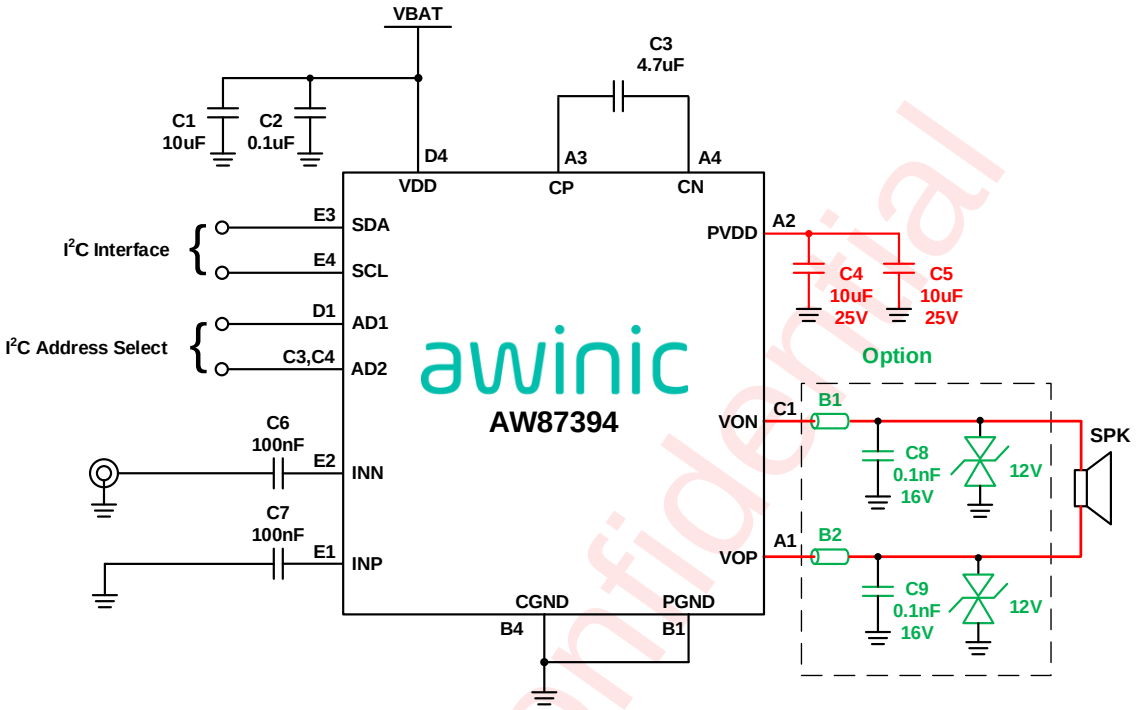


Figure 4 AW87394 Single-ended Input Mode Application Diagram(Note 1)

Note1：*When single-ended input, audio signal line from audio DAC (HPL or HPR) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPREF) through input capacitor and resistor.*

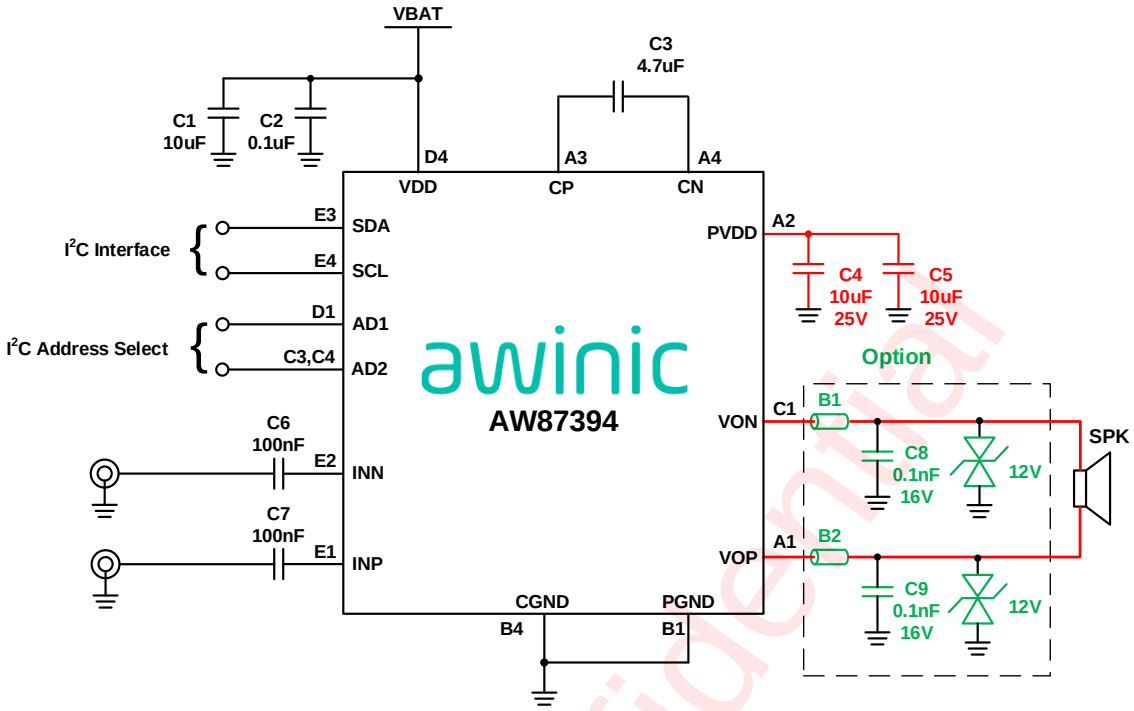


Figure 5 AW87394 Differential Inputs Mode Application Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87394FCR	-40°C～85°C	FCQFN 2.5x2-15L(0.55)	TV8J	MSL1	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

Parameter	Range
Supply Voltage V_{DD}	-0.3V to 6V
INN,INP	-0.3V to VDD+0.3V
Charge pump output voltage PVDD	-0.3V to 9.5V
VOP,VON	-0.6V to PVDD+0.6V
CP	-0.3V to PVDD+0.3V
CN	-0.3V to VDD+0.3V
Minimum load resistance R_L	5Ω
Package Thermal Resistance θ_{JA}	82°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C

Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature（Soldering 10 Seconds）	260°C
ESD Rating (Note 3)	
HBM（human body model）	±2kV
CDM（charged-device model）	±1.5kV
Latch-up	
Test Condition：JESD78F.02-2023	+IT：200mA -IT：-200mA

NOTE2: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2023.

Test method of the charge device model: ANSI/ESDA/JEDEC JS-002-2022.

Electrical Characteristics

Test condition: T_A=25°C, VDD=3.6V, PVDD OVP=8.0V, R_L=8Ω+33μH, f=1kHz (unless otherwise noted)

Parameter		Test conditions		Min	Typ	Max	Units
V_{DD}	Power supply voltage			2.7		5.5	V
UVLO	Under-voltage protection voltage				2.3		V
	Under-voltage protection hysteresis voltage				80		mV
V_{IH}(Note5)	SCL, SDA, AD1, AD2 high-level input voltage			0.84		V_{DD}	V
V_{IL}(Note5)	SCL, SDA, AD1, AD2 low-level input voltage			0		0.36	V
I_{SB}	Standby current	V_{DD}=3.6V			3.5		μA
T_{SD}	Over temperature protection threshold				160		°C
T_{SDR}	Over temperature protection recovery threshold				130		°C
T_{ON}	Turn-On time	Cin=100nF			45		ms
ADP DO-Charge pump							
PVDD	The maximum Output voltage	V_{DD}=2.7V to 4.0V, PVDD OVP=8.0V			2*VDD		V
		V_{DD} >4.0V			8.0 (Note4)		V
OVP	OVP voltage	V_{DD} >4.0V			8.0 (Note4)		V
	OVP hysteresis voltage	V_{DD} >4.0V			50		mV
F_{CP}	Charge pump operating frequency	V_{DD}=2.7V to 5.5V		1.18	1.6	2	MHz
η_{CP}	Charge pump efficiency	V_{DD} = 4.2V, I_{load} = 200mA			92		%
T_{ST}	Softstart Time	No load, COUT=4.7μF			0.5		ms
LSPK MODE							
V_{OS}(Note5)	Output offset voltage	No input		-6	0	6	mV
I_q	Speaker quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			9.3		mA
η	Total efficiency(CP+Class D)	V_{DD}=4.2V, Po=1.0W, R_L=8Ω+33μH, PVDD OVP=8.0V			81		%
Vinp	Recommended input signal amplitude	V_{DD}=2.7V to 5.5V				1.414	Vp
Fosc	Modulation frequency	V_{DD}=2.7V to 5.5V		600	800	1000	kHz
Pagc(Note5)	Multi-Leval AGC power	R_L=8Ω+33μH		0.72	0.8 (Note4)	0.88	W
		R_L=6Ω+33μH		0.96	1.067(Note4)	1.17	W
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vpp_sin=200mV	217Hz		83		dB
			1kHz		84		dB
SNR	Signal-to-noise ratio	V_{DD}=4.2V, PVDD OVP=8.0V, Av=18dB , THD+N=1%,R_L=8Ω+33μH,			102		dB
		V_{DD}=4.2V, PVDD OVP=8.0V, Av=18dB, Po=0.8W, R_L=8Ω+33μH			97		dB
E_N	Speaker Output noise	Av=24dB, LSPK Mode	20Hz to 20kHz, input ac grounded, A-weighting		38		μV
		Av=18dB, LSPK Mode			28		μV
Av	Speaker gain	V_{DD}=2.7V to 5.5V			18 (Note4)		dB
Rini	Speaker Inner input resistance	Av=18dB, LSPK Mode			15		kΩ
Fin	Speaker input Cut-off frequency	Cin=100nF, Av=18dB, LSPK Mode			110		Hz

Parameter		Test conditions		Min	Typ	Max	Units
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.6W, RL=8Ω+33μH, f=1kHz, PVDD OVP=8.0V			0.02		%
Rdson	Drain-Source on-state resistance	High side MOS + Low side MOS			550		mΩ
Po	Speaker Output Power	THD+N=1%, RL=8Ω+33μH, VDD=4.2V, PVDD OVP=8.0V			2.3		W
		THD+N=10%, RL=8Ω+33μH, VDD=4.2V, PVDD OVP=8.0V			2.8		W
		THD+N=1%, RL=6Ω+33μH, VDD=4.2V, PVDD OVP=8.0V			2.45		W
		THD+N=10%, RL=6Ω+33μH, VDD=4.2V, PVDD OVP=8.0V			2.9		W
		THD+N=1%, RL=8Ω+33μH, VDD=3.6V, PVDD OVP=8.0V			1.65		W
		THD+N=10%, RL=8Ω+33μH, VDD=3.6V, PVDD OVP=8.0V			2.1		W
		THD+N=1%, RL=6Ω+33μH, VDD=3.6V, PVDD OVP=8.0V			1.8		W
		THD+N=10%, RL=6Ω+33μH, VDD=3.6V, PVDD OVP=8.0V			2.15		W
ADP MODE							
V_{OS} (Note5)	Output offset voltage	No input		-6	0	6	mV
I_q	Speaker quiescent current	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			4		mA
PO_{TH}	Adaptive power threshold	V_{DD}=2.7V to 5.5V, R_L=8Ω+33μH			0.3		W
η	Total efficiency(CP+Class D)	V_{DD}=4.2V, Po=1W, R_L=8Ω+33μH, PVDD OVP=8.0V			81		%
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vpp_sin=200mV	217Hz		80		dB
			1kHz		80		dB
E_N	Speaker Output noise	Av=24dB,LADP Mode	20Hz to 20kHz, input ac grounded, A-weighting		38		μV
		Av=18dB,LADP Mode			28		μV
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.3W, RL=8Ω+33μH, f=1kHz, PVDD OVP=8.0V			0.02		%
Receiver MODE (1X Charge pump)							
V_{OS} (Note5)	Output offset voltage	No input		-6	0	6	mV
I_q	Receiver quiescent current (overall)	V_{DD}=3.6V, input ac grounded, R_L=8Ω+33μH			4		mA
η	SRCV efficiency	V_{DD}=4.2V, Po=0.6W, R_L=8Ω+33μH			86		%
Av	Receiver gain	V_{DD}=2.7V to 5.5V			0 (Note4)		dB
Rini	SRCV Inner input resistance	Av=0dB			24		kΩ
		Av=6dB			8		kΩ
	LRCV Inner input resistance	Av=0dB			24		kΩ
Fin	SRCV input cut-off frequency	Cin=100nF, Av=0dB			70		Hz
E_N	SRCV Output noise	Av=0dB	20Hz to 20kHz, input ac grounded, A-weighting		9		μV
		Av=6dB			13.8		μV
	LRCV Output noise	Av=0dB			7.5		μV
THD+N	Total harmonic distortion + noise	VDD=4.2V, Po=0.1W,RL=8Ω+33μH, f=1kHz			0.02		%
PSRR		V_{DD}=4.2V,	217Hz		82		dB

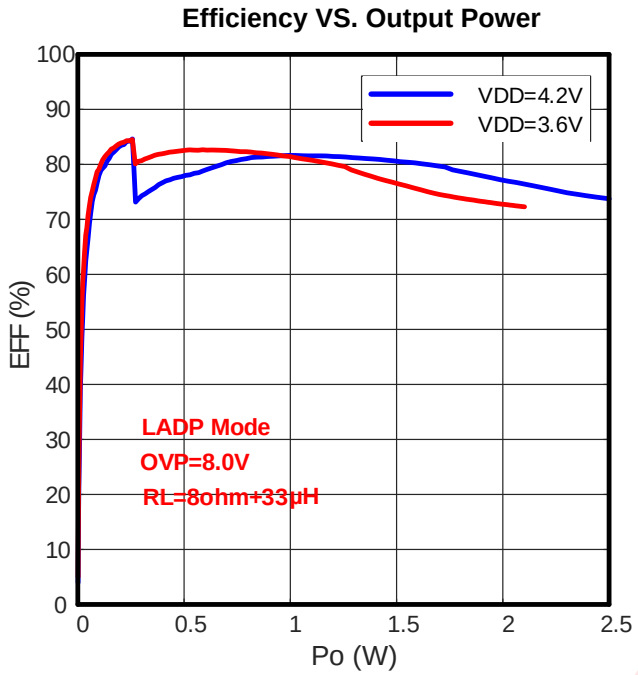
Parameter		Test conditions		Min	Typ	Max	Units
	Receiver Power supply rejection ratio	Vp-p_sin=200mV	1kHz		82		dB
Po	SRCV Output Power	Av=0dB,THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.55		W
		Av=0dB,THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V			0.68		W
		Av=9dB,THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.86		W
		Av=9dB,THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V			1.06		W
	LRCV Output Power	Av=0dB,THD+N=1%, R_L=8Ω+33μH, V_{DD}=4.2V			0.14		W
		Av=0dB,THD+N=10%, R_L=8Ω+33μH, V_{DD}=4.2V			0.17		W
Multi-Level AGC							
T_{AT1}	AGC1 Attack Time				0.08 (Note4)		ms/dB
T_{AT2}	AGC2 Attack Time				41 (Note4)		ms/dB
T_{RLT}	Release time				21 (Note4)		ms/dB
A_{MAX}	The maximum attenuation gain	V_{DD}=2.7V to 5.5V			-13.5		dB

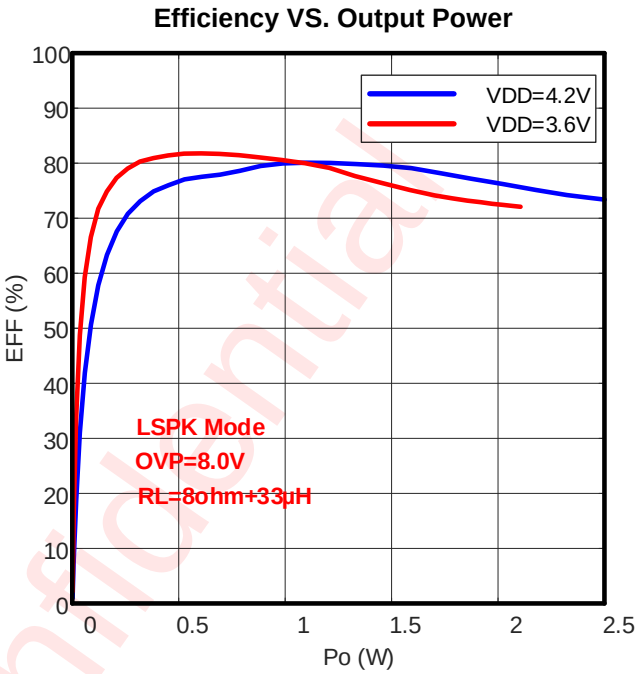
Note 4: *Registers are adjustable; Refer to the list of registers.*

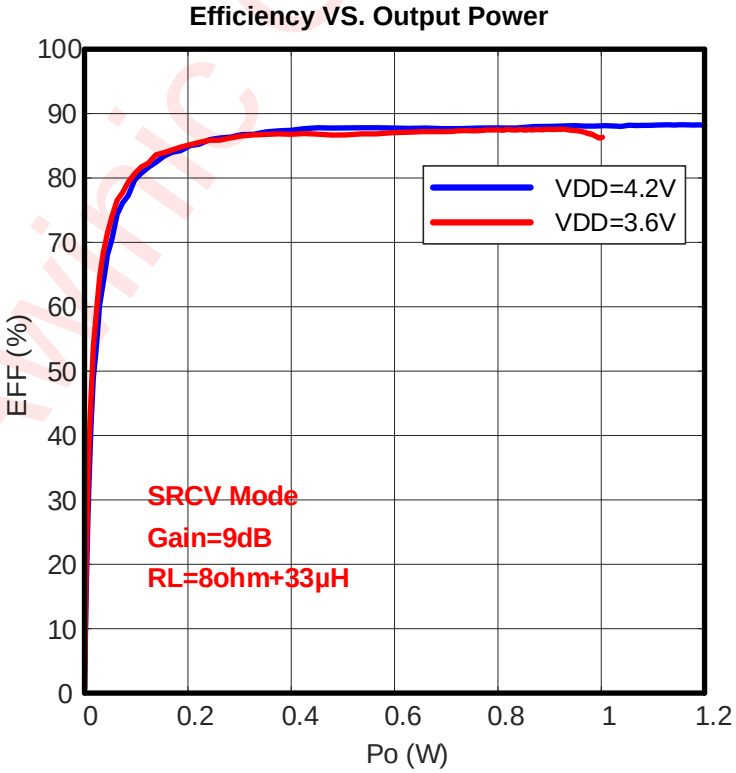
Note 5: *Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.*

Typical Characteristics

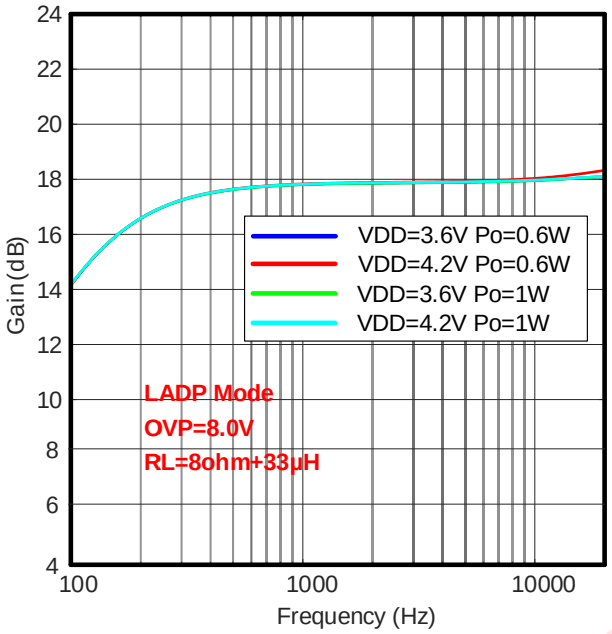
T_A=25°C



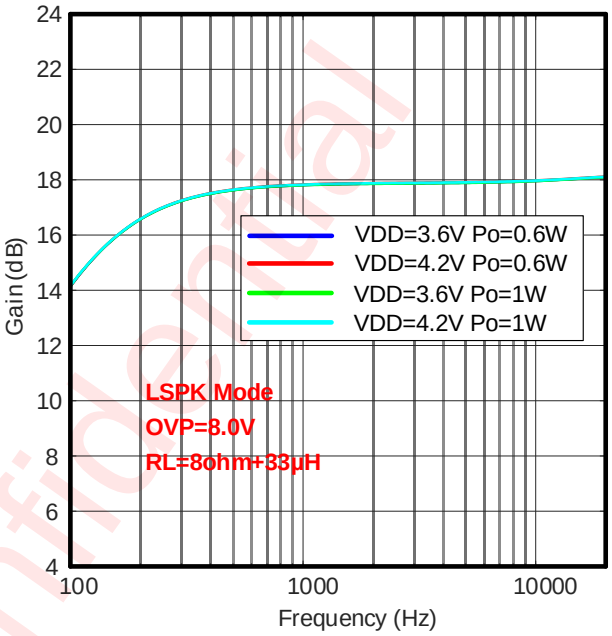




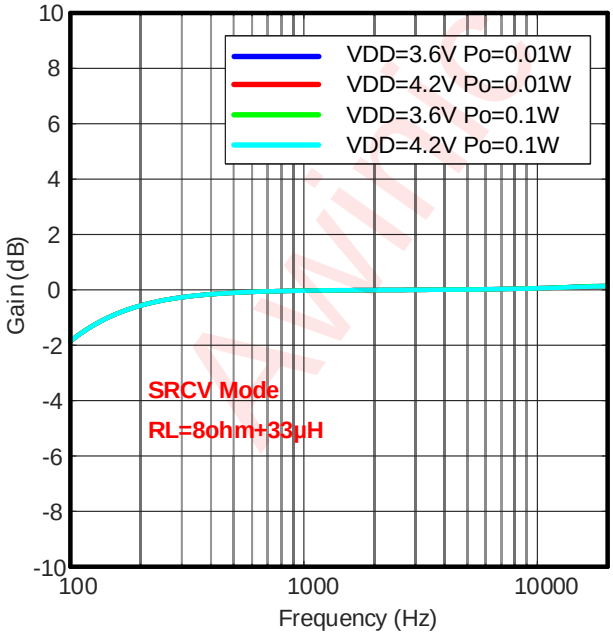
Gain VS. Frequency



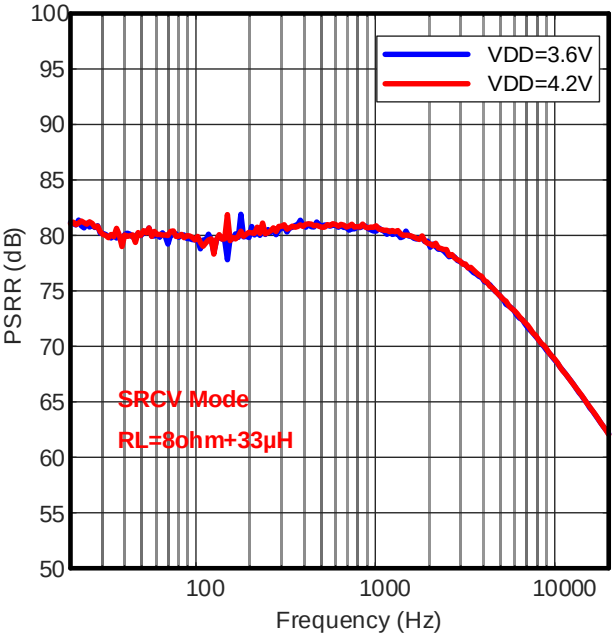
Gain VS. Frequency



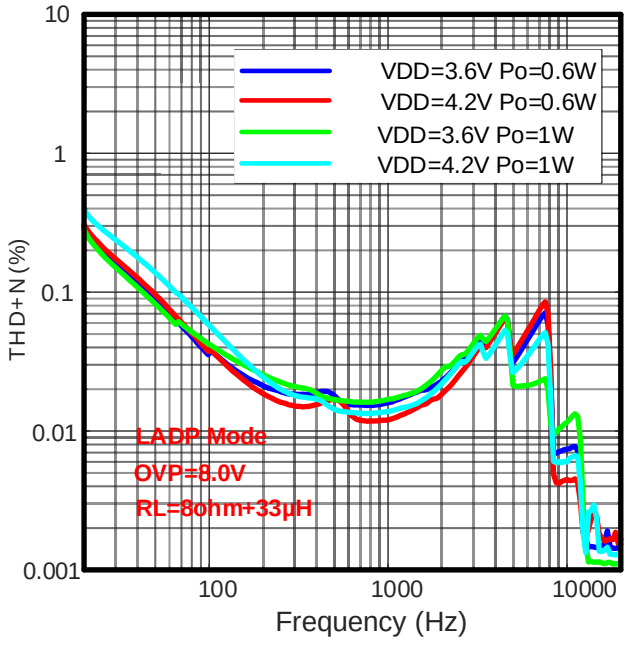
Gain VS. Frequency



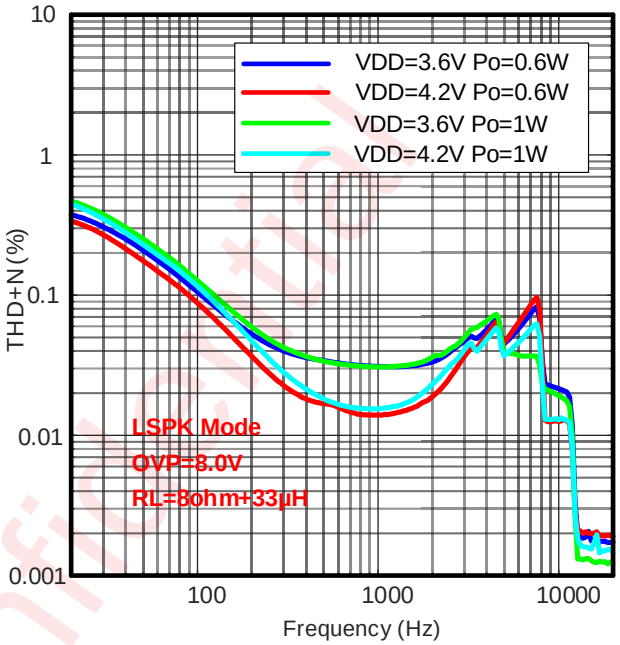
PSRR VS. Frequency



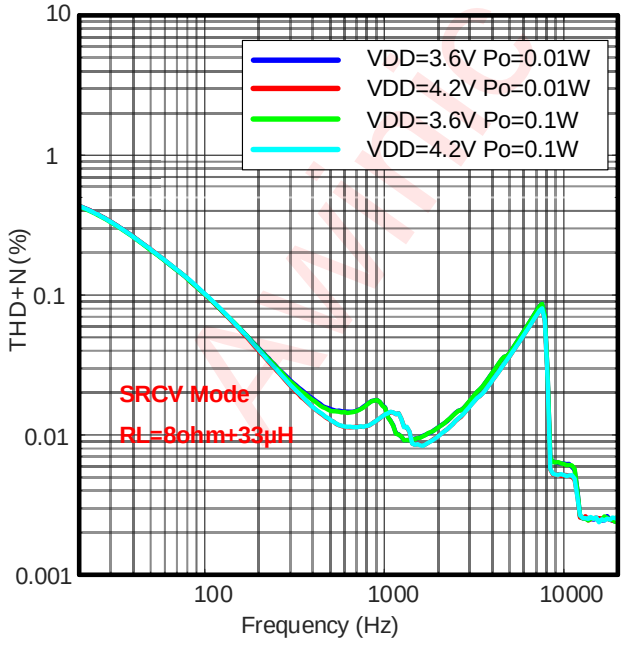
THD+N VS. Frequency



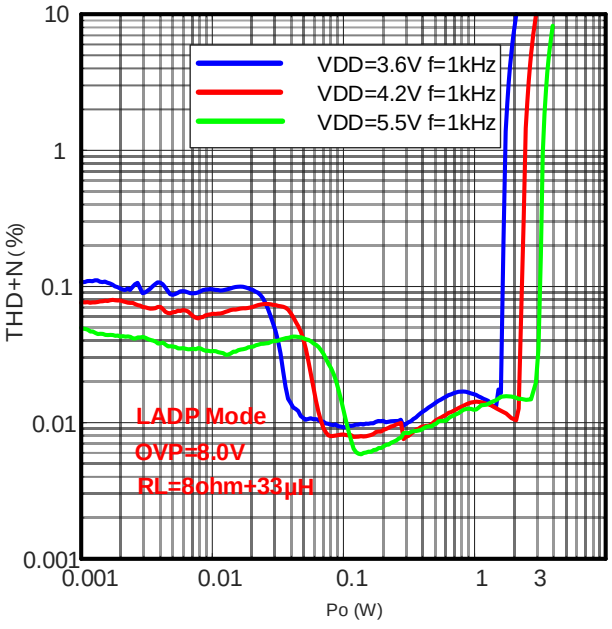
THD+N VS. Frequency



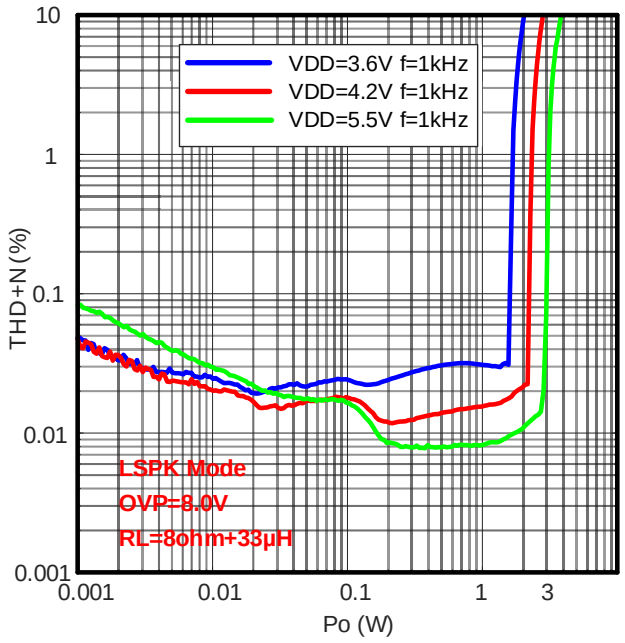
THD+N VS. Frequency



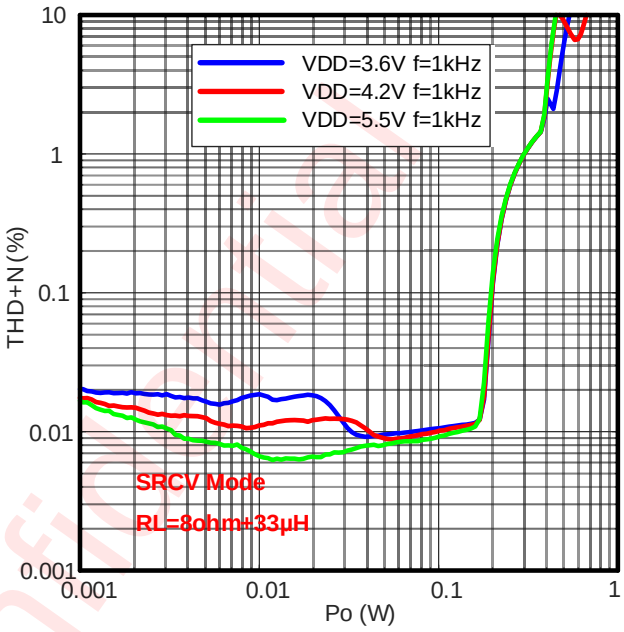
THD+N VS. Po



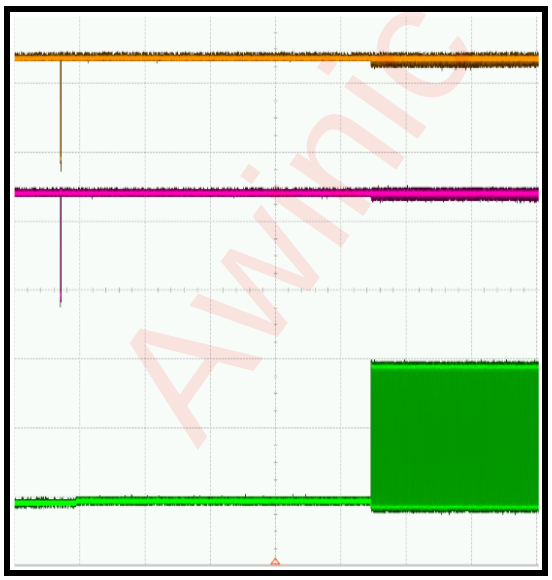
THD+N VS. Po



THD+N VS. Po

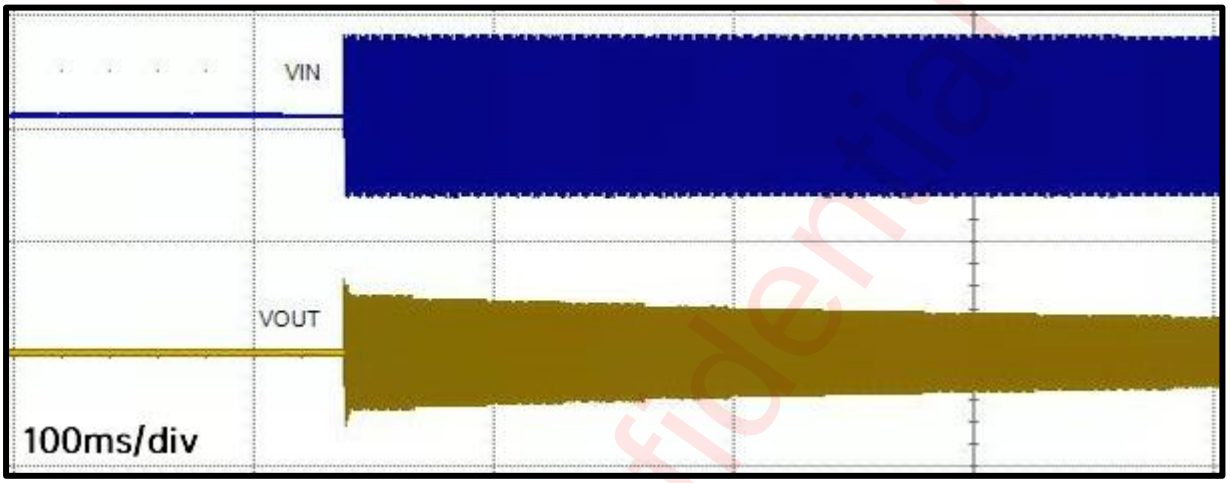


Start-up Sequence

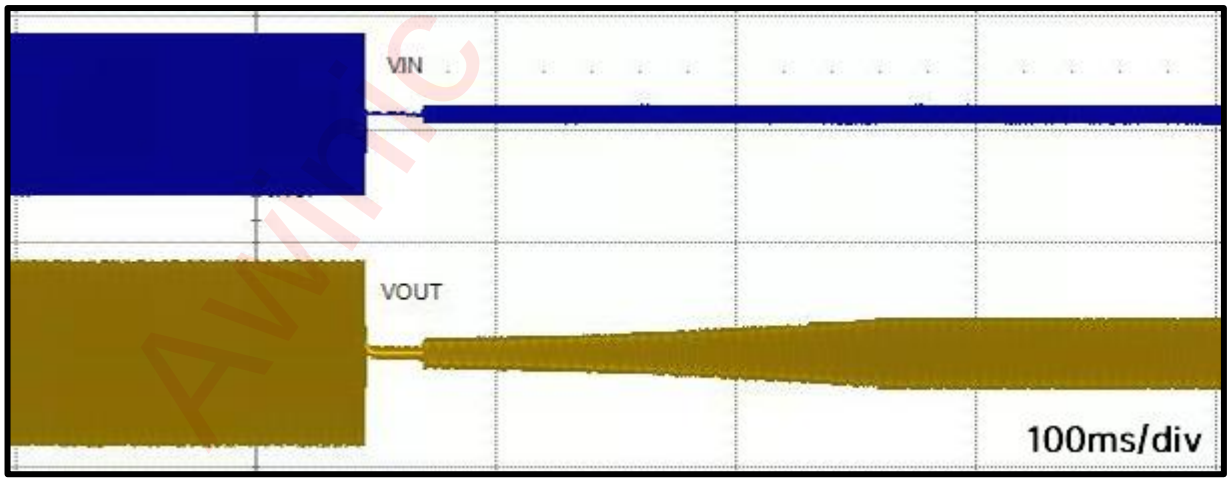


Shutdown Sequence

Multi-Level AGC Attack Timing



Multi-Level AGC Release Timing



Working Principle

I²C Timing feature

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

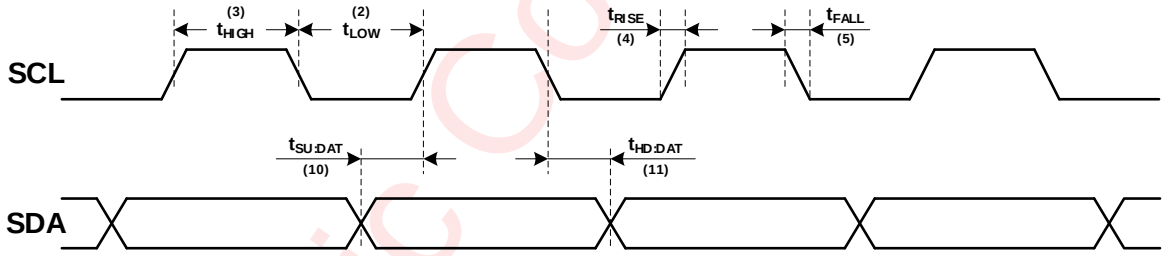


Figure 6 SCL and SDA timing relationships in the data transmission process

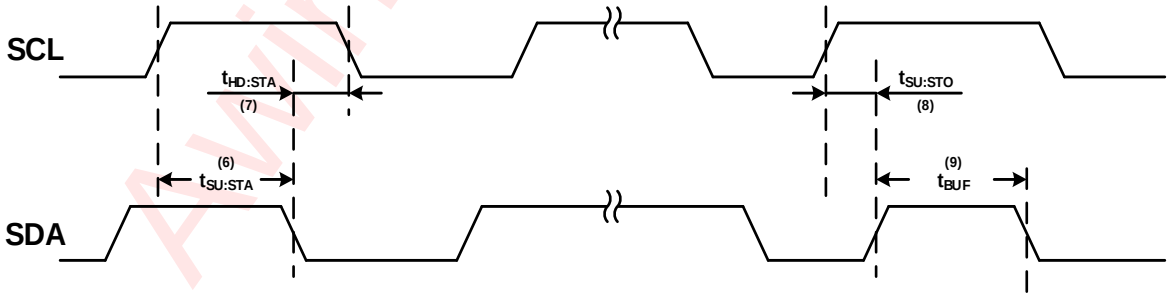


Figure 7 the Timing Relationship between START and STOP State

General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. All data to start transmission and end of transmission requires the main device to issue START state and STOP status:

START state：The SCL maintain a high level, SDA from high to low level

STOP state：The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure 8.

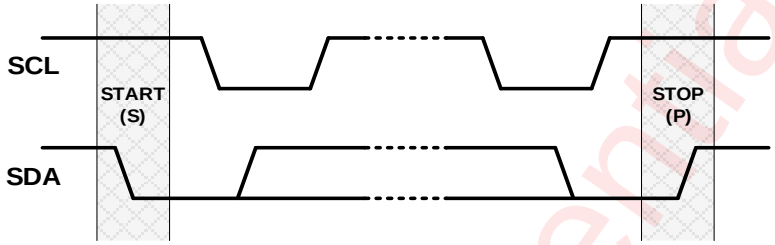


Figure 8 START and STOP State Generation Process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 9. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 10. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

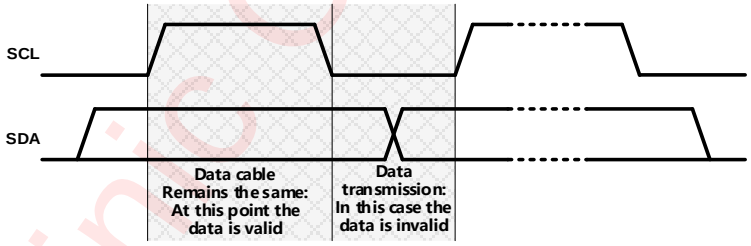


Figure 9 The Data Transfer Rules on the I²C Bus

The whole process of actual data transmission is shown in Figure 10. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

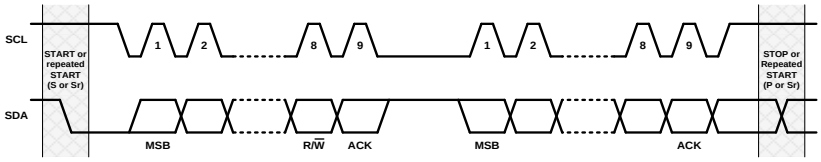


Figure 10 Data Transmission on the I²C Bus

I²C Read/Write Processes

The following describes two kinds of ways of the I²C bus data transmission:

Write Process

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, AW87394 as the slave device, the transmission process in accordance with the following steps, as shown in Figure 11:

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit AW87394 register address to which the first data byte will written；

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data, it does not need further to send the register address for AW87394, within AW87394 each send confirmation bit(ACK) regret automatic accumulation register address then only need to repeat the sixth step and seven step:

The master device generates the STOP state to end the data transmission.

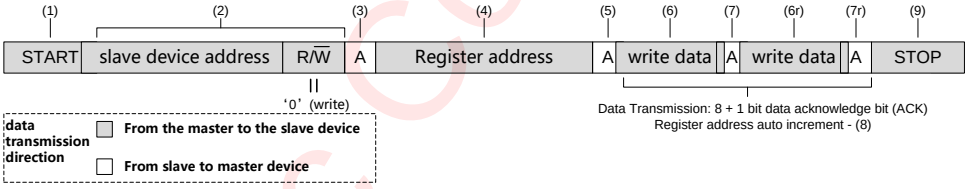


Figure 11 Writing Process (Data Transmission Direction Remains the Same)

Read Process

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW87394 as the slave device, the transmission process carried out by following steps listed in Figure 12:

(1) Master device asserts a start condition;

(2) Master device transmits the 7 bits address of AW87394, and followed by a "read / write" flag ($R/\overline{W}$ =0);

(3) The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

(4) The master device sends the 8bit address that the AW87394 register needs to read the data;

(5) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

(6) The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

(7) Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1)

again;

(8) The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

(9) The slave transmits 8 bits of data to register which needs to be read;

(10) The master device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

(11) AW87394 automatically increment register address once after the slave sent each acknowledge bit (ACK);

(12) The master device generates the STOP state to end the data transmission;

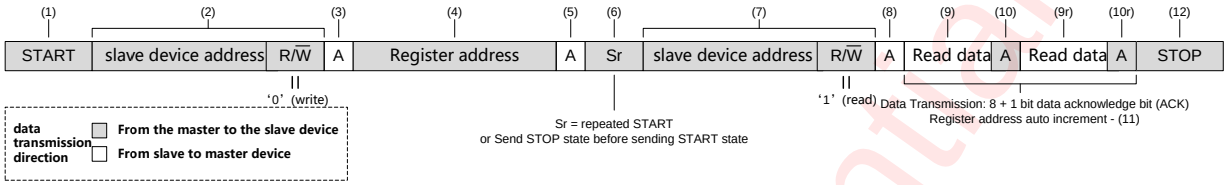
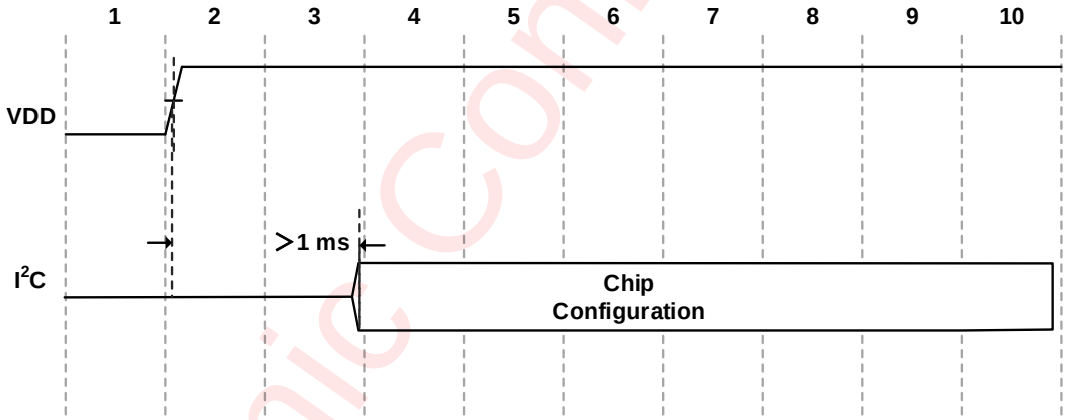


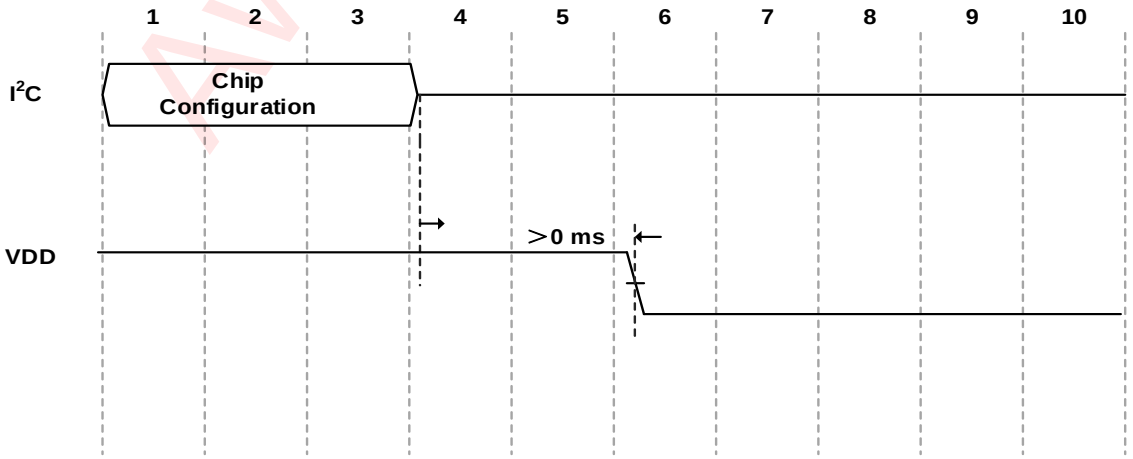
Figure 12 Reading Process (Data Transmission Direction Remains the Same)

Power Up and Power Down Sequence

Power up sequence considering I²C timing shows as below:



Power down sequence considering I²C timing shows as below:



Register Configuration

Register List

Write AA to the 00 register of the AW87394 to reset the register.

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	ID	RO	IDCODE							
0x01	IIC_EN	RW							I2C_WEN	
0x02	SYSCTRL	RW		EN_SRCV	EN_ADAP	EN_2X	EN_SPK	EN_PA	EN_CP	EN_SW
0x03	CP	RW					CP_OVP			
0x04	PA	RW	PD_AGC1	AGC2PO				GAIN		
0x05	AGC	RW	AK1_S		RK_S		AK2_S		AK2F_S	
0x06	SYSST	RO	UVLO	OTN		ADAP	STARTOK	OVP	PORN	
0x07	SYSINT	RC	UVLOI	OTNI		ADAPI	STARTOKI	OVPI	PORNI	

Any register address which is more than 0x07 and all reserved bits are reserved for debugging and testing purposes. Changing their values may affect the normal function of the power amplifier; Reading them will get any possible values. AW87394's I²C address is 10110A2A1, as shown in Table 1, in order to avoid conflict with other I²C devices address, you can pull up or pull-down AW87394 of AD2 and AD1 pins to set the value of A2 and A1, respectively. The following lists specific information about all visible registers, including default values and programmable ranges.

AD2/A2	AD1/A1	I²C Address
0	0	0x58
0	1	0x59
1	0	0x5A
1	1	0x5B

Table 1 AW87394 Address Byte

Register Detailed Description

ID: (Address 00h)				
Bit	Symbol	R/W	Description	Default
7:0	IDCODE	RO	Chip ID will be returned after read	0x23
IIC_EN: (Address 01h)				
Bit	Symbol	R/W	Description	Default
7:2	Reserved	RW	Not used	0
1:0	I2C_WEN	RW	I2C write enable open only by write 0x2	0x0
SYSCTRL: (Address 02h)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6	EN_SRCV	RW	PA Version Select 0: Low noise Version 1: Super RCV Mode (Note: Only EN_SPK=0 valid)	0x0

5	EN_ADAP	RW	ADAP Function setting 0:ADP disable 1:ADP enable	0x1
4	EN_2X	RW	2X Charge Pump Mode enable. Only when EN_CP=0, this bit can be written. 0: 2X Charge Pump Mode disable, 1X Direct Through Mode enable 1: 2X Charge Pump Mode enable, 1X Direct Through Mode disable	0x1
3	EN_SPK	RW	SPK Mode or RCV Mode enable. Changing this bit results in reconfiguration of gain scope. 0: SPK Mode disable 1: SPK Mode enable	0x1
2	EN_PA	RW	Power Amplifier enable 0: Power Amplifier disable 1: Power Amplifier enable	0x1
1	EN_CP	RW	Charge Pump enable. 0:Charge Pump disable, PVDD=0 1: Charge Pump enable, the CP working mode depends on EN_2X	0x1
0	EN_SW	RW	Chip software enable. If EN_PA=EN_CP=1, when change EN_CP from 1 to 0, only set EN_SW=0. 0: software disable 1: software enable	0x0

CP: (Address 03h)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	0x3
3:0	CP_OVP	RW	Charge Pump OVP Threshold 0000：6.50V 0001：6.75V 0010：7.00V 0011：7.25V 0100：7.50V 0101：7.75V 0110：8.00V 0111：8.25V 1000：8.50V 1001-1111 reserved. If set, turns to default.	0x6

PA: (Address 04h)

Bit	Symbol	R/W	Description	Default
7	PD_AGC1	RW	AGC1 function power-down 0: AGC1 function power-up 1: AGC1 function power-down	0x0

6:3	AGC2PO	RW	AGC2 Output Power setting: when EN_SPK=1 0000: 0.5w@8Ω 0001: 0.6w@8Ω 0010: 0.7w@8Ω 0011: 0.8w@8Ω 0100: 0.9w@8Ω 0101: 1.0w@8Ω 0110: 1.1w@8Ω 0111: 1.2w@8Ω 1000: 1.3w@8Ω 1001: 1.4w@8Ω 1010: 1.5w@8Ω 1011: 1.6w@8Ω 1100-1110: not used, and set to 1011 1111: AGC2 OFF	0x7
2:0	GAIN	RW	Power Amplifier Gain setting: when EN_SPK=1 000：12.0dB 001：15.0dB 010：18.0dB 011：21.0dB 100：24.0dB 101-111: reserved. If set, turns to default Power Amplifier Gain setting: when EN_SPK=0 000：0.0dB 001：3.0dB 010：6.0dB 011：9.0dB 100-111: reserved. If set, turns to 000	0x2

AGC: (Address 05h)

Bit	Symbol	R/W	Description	Default
7:6	AK1_S	RW	AGC1_FAST Attack Time setting 00: 0.04ms/dB 01: 0.08ms/dB 10: 0.16ms/dB 11: 0.32ms/dB	0x1
5:4	RK_S	RW	AGC1 and AGC2 Release Time setting 00: 10.24ms/dB 01: 20.48ms/dB 10: 41ms/dB 11: 82ms/dB	0x1
3:2	AK2_S	RW	AGC2_SLOW Attack Time setting 00: 2.56ms/dB 01: 10.24ms/dB 10: 41ms/dB 11: 82ms/dB	0x2
1:0	AK2F_S	RW	AGC2_SLOW First Attack Time setting 00: 10.24ms/dB 01: 20.48ms/dB 10: 41ms/dB 11: 82ms/dB	0x2

SYSST: (Address 06h)

Bit	Symbol	R/W	Description	Default
7	UVLO	RO	None	0x0
6	OTN	RO	None	0x1
5	Reserved	RO	Not used	0x0

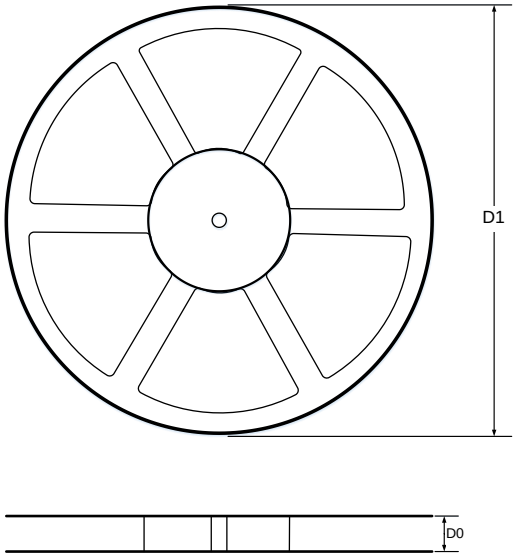
4	ADAP	RO	None	0x0
3	STARTOK	RO	None	0x0
2	OVP	RO	None	0x0
1	PORN	RO	None	0x1
0	Reserved	RO	Not used	0

SYSINT: (Address 07h)

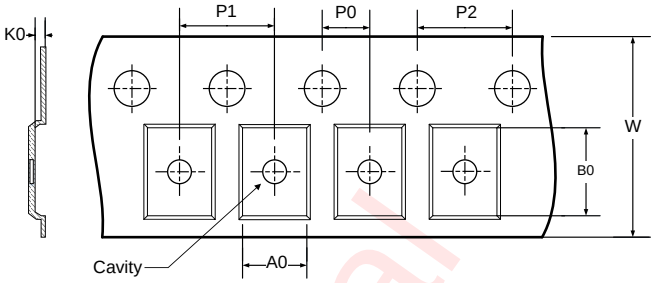
Bit	Symbol	R/W	Description	Default
7	UVLOI	RC	None	0x0
6	OTNI	RC	None	0x1
5	Reserved	RO	Not used	0x0
4	ADAPI	RC	None	0x0
3	STARTOKI	RC	None	0x0
2	OVPI	RC	None	0x0
1	PORNI	RC	None	0x1
0	Reserved	RC	Not used	0

TAPE AND REEL INFORMATION

REEL DIMENSIONS

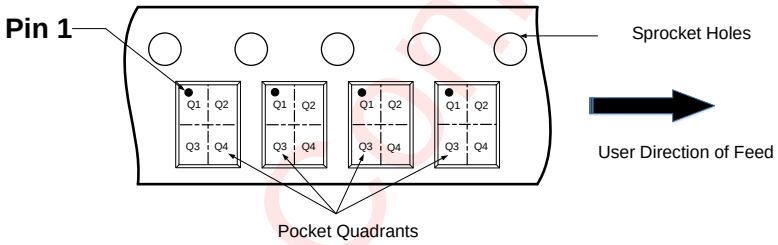


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



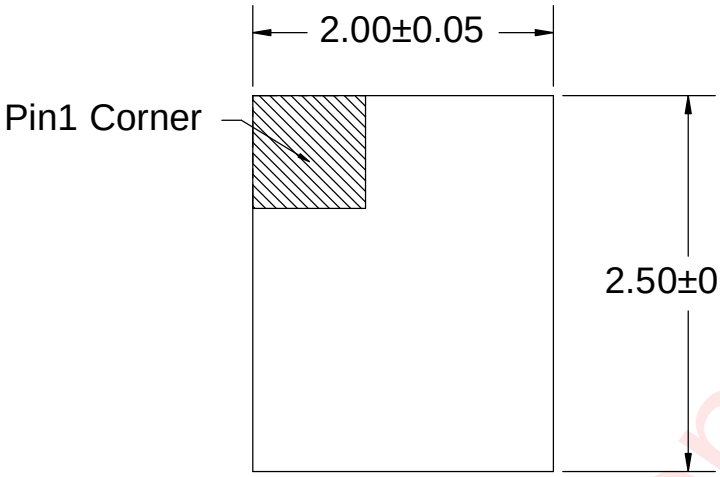
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

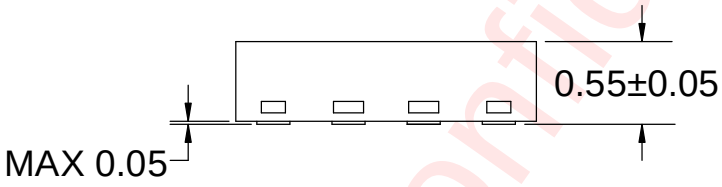
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.60	2.25	2.75	0.75	2.00	8.00	4.00	12.00	Q1

All dimensions are nominal

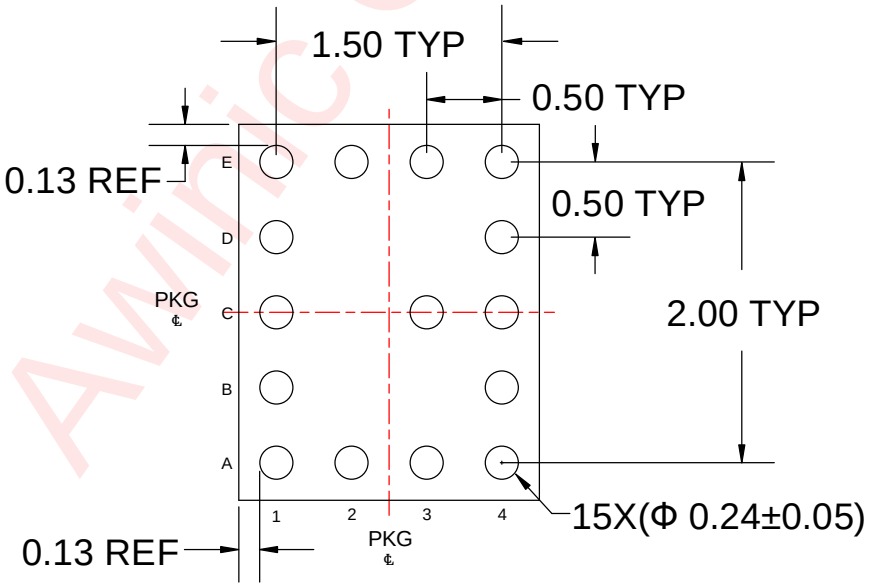
PACKAGE DESCRIPTION



TOP VIEW



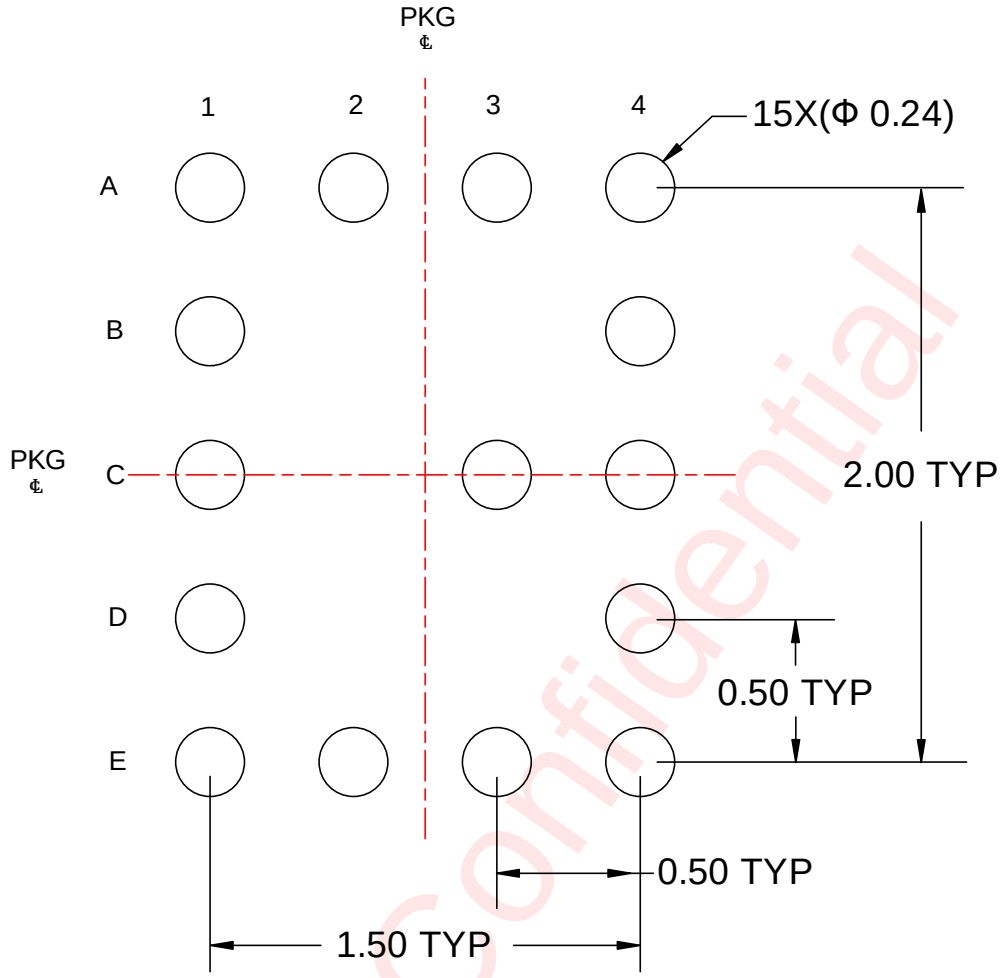
SIDE VIEW

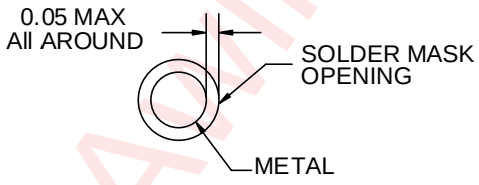


BOTTOM VIEW

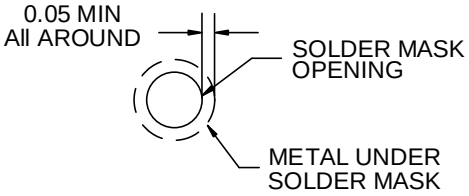
Unit: mm

LAND PATTERN DATA





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Nov.2024	Officially Released
V1.1	Dec.2024	Fixed some register information.
V1.2	Feb.2025	Fixed some Electrical Characteristics and typical characteristics.

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