

N and P Channel Enhancement Mode Power MOSFET

Description

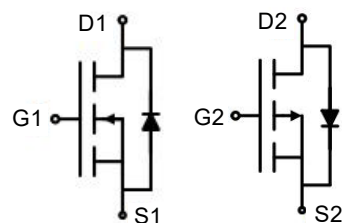
The G100C04D52 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

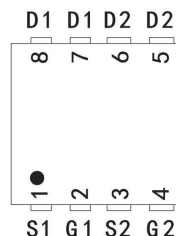
- NMOS
- V_{DS} 40V
- I_D (at $V_{GS} = 10V$) 60A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 9m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 12m Ω
- 100% Avalanche Tested
- RoHS Compliant
- PMOS
- V_{DS} -40V
- I_D (at $V_{GS} = -10V$) -40A
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 15m Ω
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 20m Ω
- 100% Avalanche Tested
- RoHS Compliant

Application

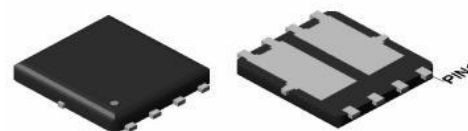
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



DFN5X6-8L Dual

Ordering Information

Device	Package	Marking	Packaging
G100C04D52	DFN5*6-8L Dual	G100C04	5000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Continuous Drain Current	I_D	60	-40	A
		38	-25	
Pulsed Drain Current (note1)	I_{DM}	240	-160	A
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Power Dissipation	P_D	65	58	W
Single pulse avalanche energy (note2)	E_{AS}	81	64	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	R_{thJC}	1.9	2.2	$^\circ\text{C/W}$

NMOS Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.9	2.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 30A	--	7.5	9	mΩ
		V _{GS} = 4.5V, I _D = 30A	--	10	12	
Forward Transconductance	g _{FS}	V _{GS} = 5V, I _D = 12A	--	22	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 20V, f = 1.0MHz	--	2350	--	pF
Output Capacitance	C _{oss}		--	170	--	
Reverse Transfer Capacitance	C _{rss}		--	153	--	
Total Gate Charge	Q _g	V _{DD} = 20V, I _D = 30A, V _{GS} = 10V	--	42	--	nC
Gate-Source Charge	Q _{gs}		--	7	--	
Gate-Drain Charge	Q _{gd}		--	9	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20V, I _D = 30A, R _G = 3Ω	--	17	--	ns
Turn-on Rise Time	t _r		--	7	--	
Turn-off Delay Time	t _{d(off)}		--	30	--	
Turn-off Fall Time	t _f		--	17	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	60	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} =30A, V _{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Q _{rr}	I _F = 30A, V _{GS} = 0V di/dt=100A/us	--	26	--	nC
Reverse Recovery Time	T _{rr}		--	29	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}$, $V_{DD} = 40V$, $V_{GS} = 10V$, $L = 0.5mH$, $R_G = 25\Omega$

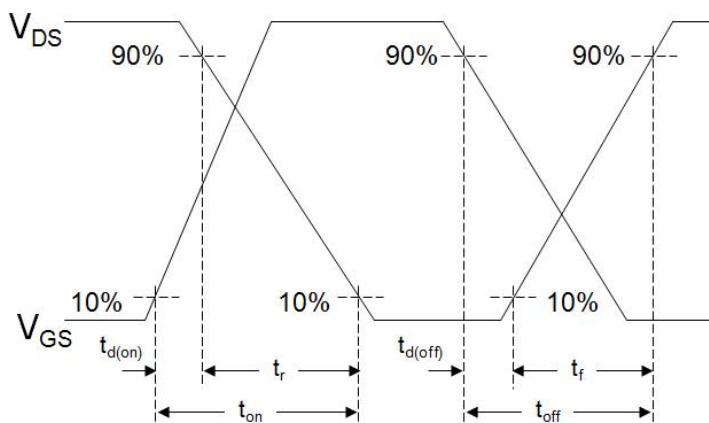
The table shows the minimum avalanche energy, which is 225mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

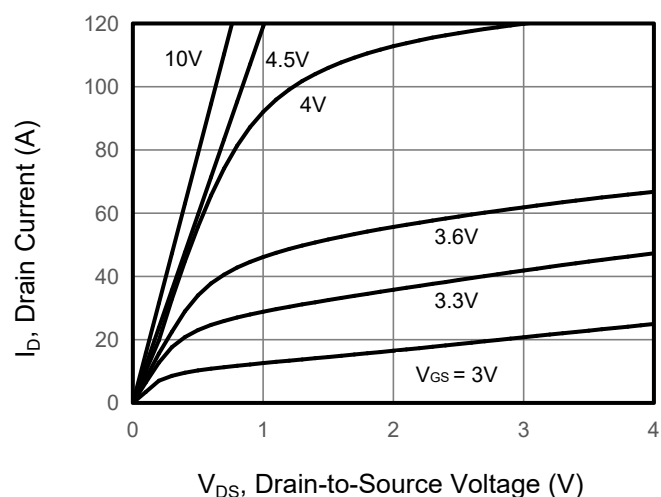


Figure 2. Transfer Characteristics

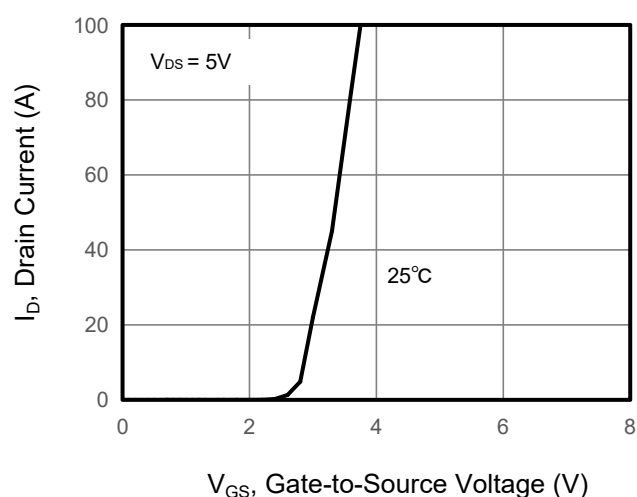


Figure 3. Drain Source On Resistance

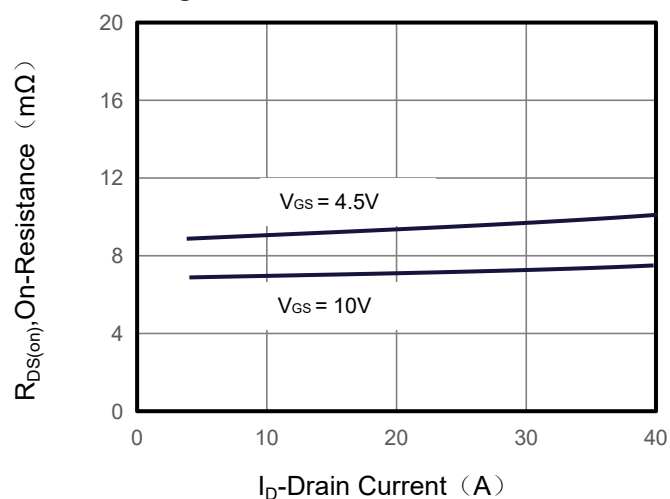


Figure 4. Gate Charge

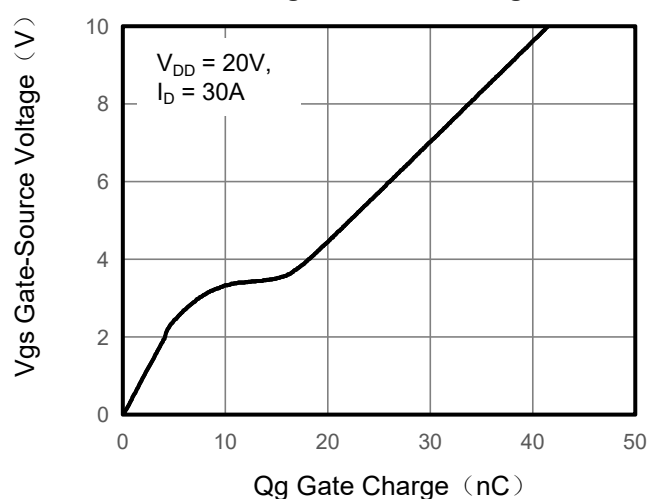


Figure 5. Capacitance

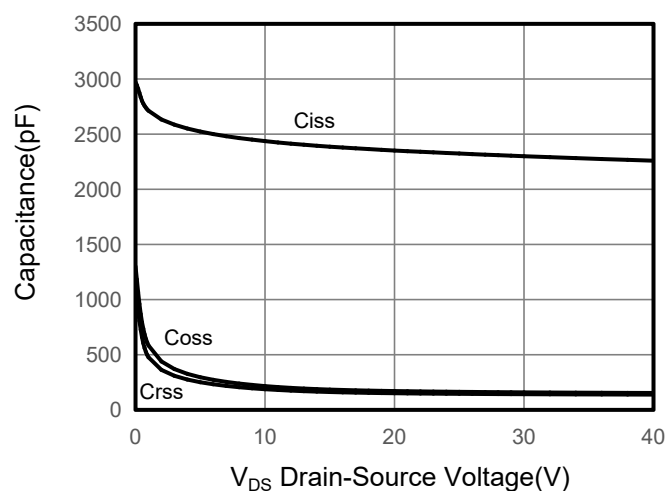
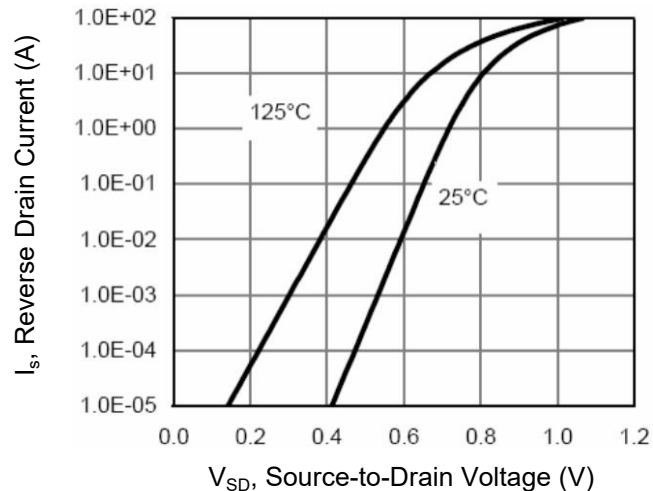


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

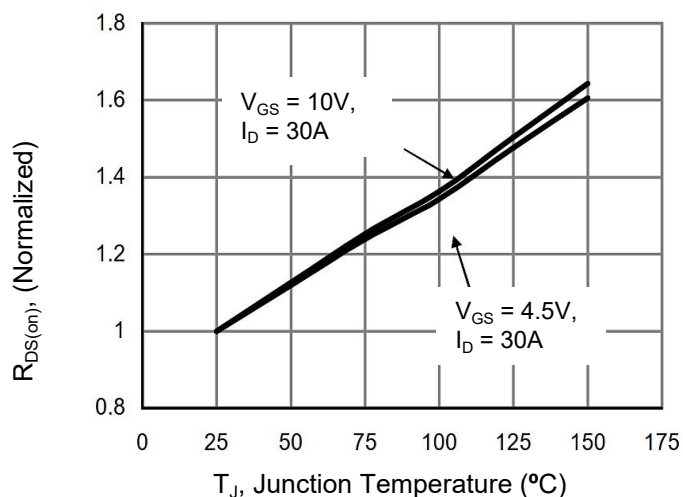


Figure 8. Safe Operation Area

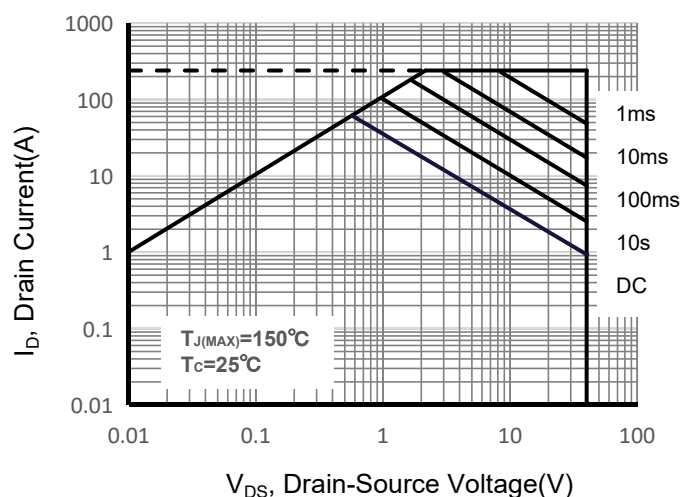


Figure 9. Maximum Continuous Drain Current vs Case Temperature

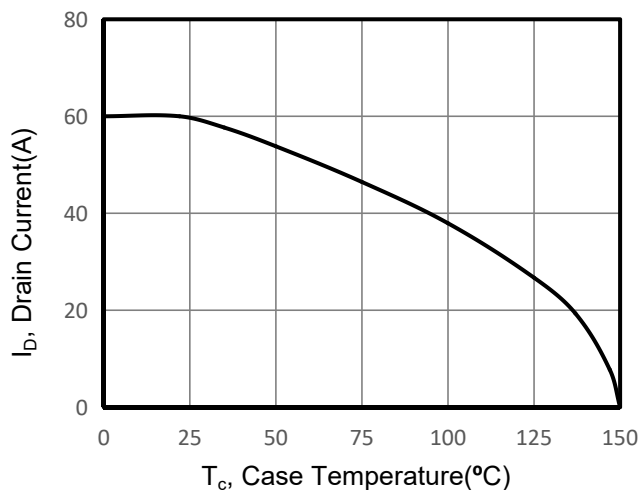
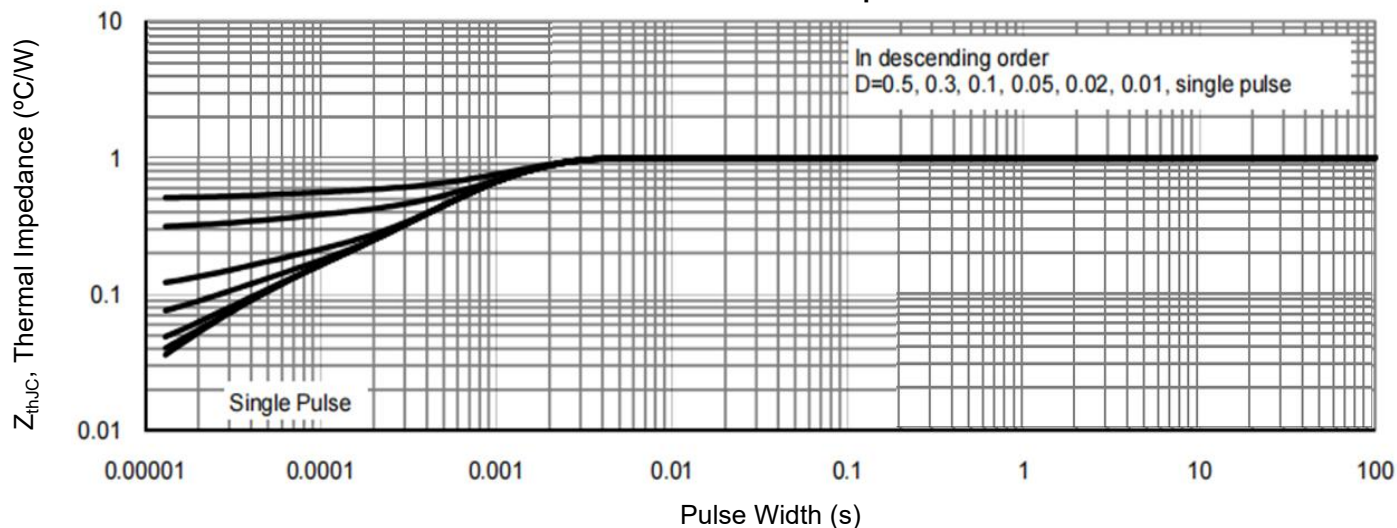


Figure 10. Normalized Maximum Transient Thermal Impedance



PMOS Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-40	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -40V, V _{GS} = 0V	--	--	-1	uA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.5	-2.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D = -10A	--	12.5	15	mΩ
		V _{GS} = -4.5V, I _D = -10A	--	16	20	
Forward Transconductance	g _{FS}	V _{DS} = -5V, I _D = -10A	--	0.7	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -20V, f = 1.0MHz	--	2300	--	pF
Output Capacitance	C _{oss}		--	220	--	
Reverse Transfer Capacitance	C _{rss}		--	207	--	
Total Gate Charge	Q _g	V _{DD} = -20V, I _D = -10A, V _{GS} = -10V	--	33	--	nC
Gate-Source Charge	Q _{gs}		--	5	--	
Gate-Drain Charge	Q _{gd}		--	8	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = -20V, I _D = -10A, R _G = 3Ω	--	8	--	ns
Turn-on Rise Time	t _r		--	14	--	
Turn-off Delay Time	t _{d(off)}		--	29	--	
Turn-off Fall Time	t _f		--	18	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	-40	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = -10A, V _{GS} = 0V	--	--	-1.2	V
Reverse Recovery Time	T _{rr}	I _S = -10A, V _{GS} = 0V di/dt=-100A/us	--	32	--	ns
Reverse Recovery Charge	Q _{rr}		--	31	--	ns

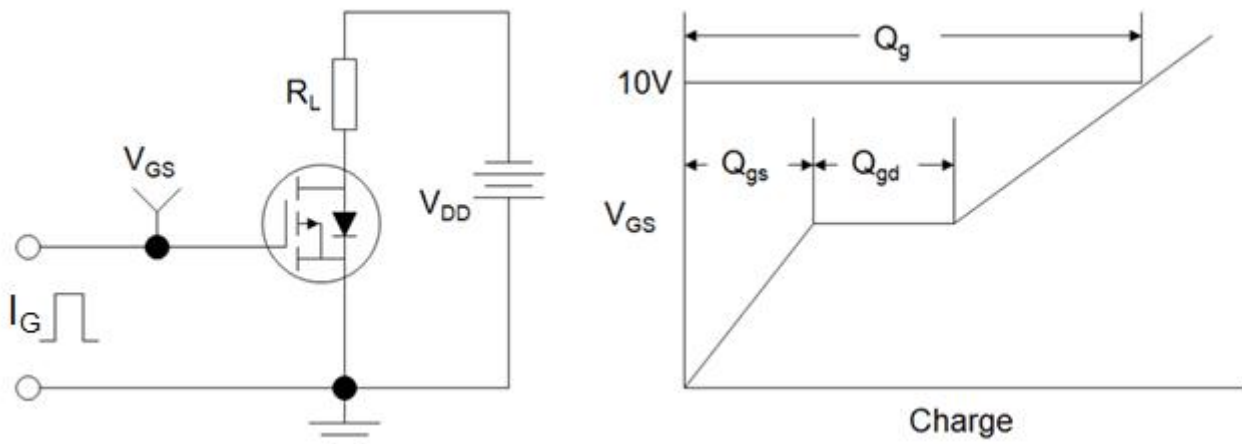
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^\circ\text{C}$, $V_{DD} = -40V$, $V_{GS} = -10V$, $L = 0.5mH$, $R_G = 25\Omega$

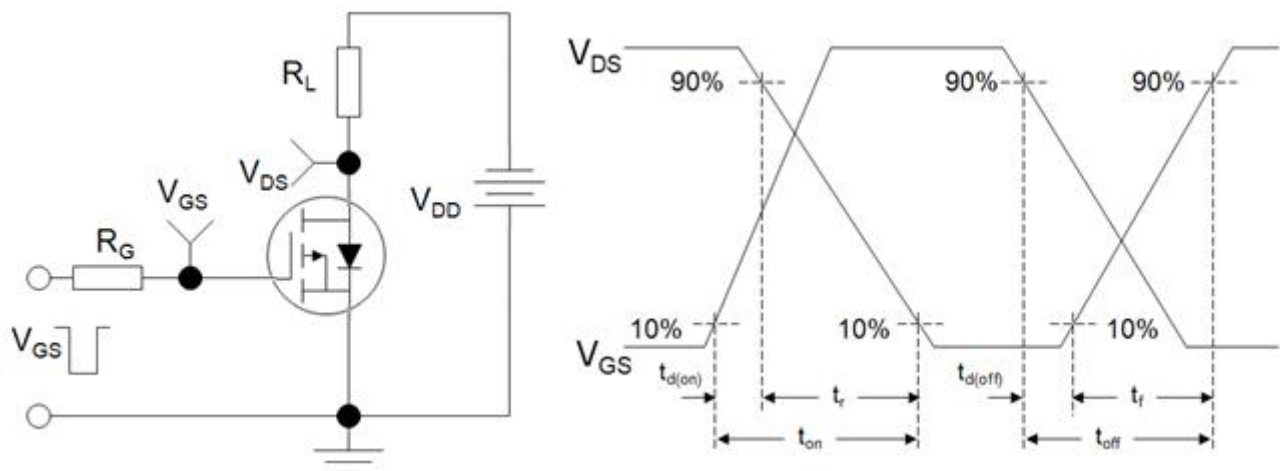
The table shows the minimum avalanche energy, which is 169mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

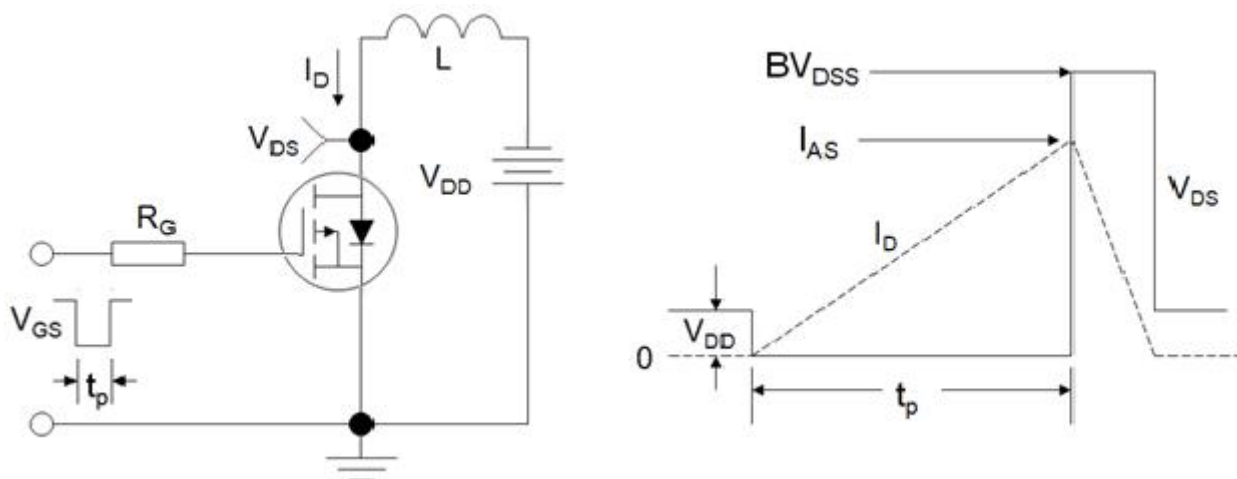
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

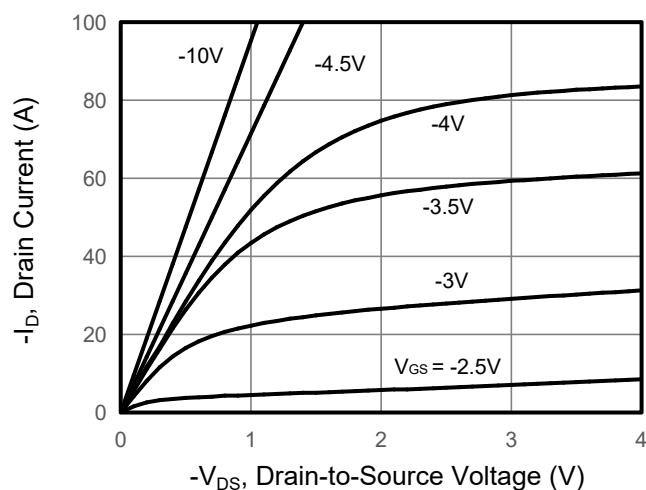


Figure 2. Transfer Characteristics

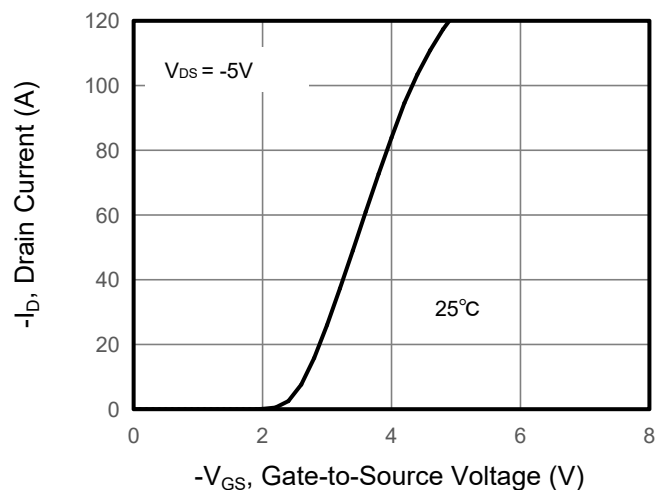


Figure 3. Drain Source On Resistance

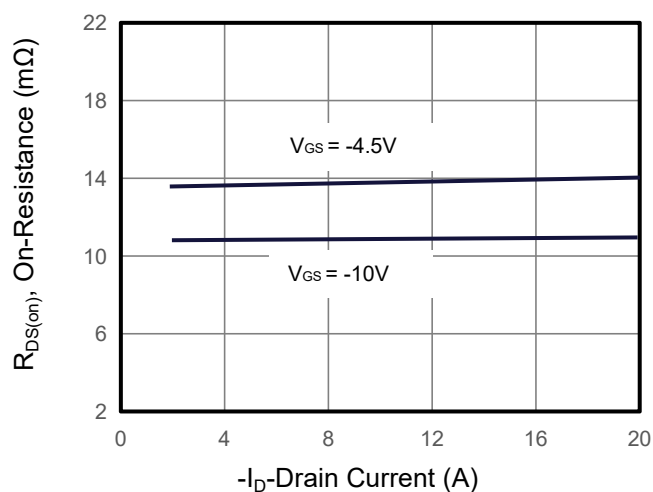


Figure 4. Gate Charge

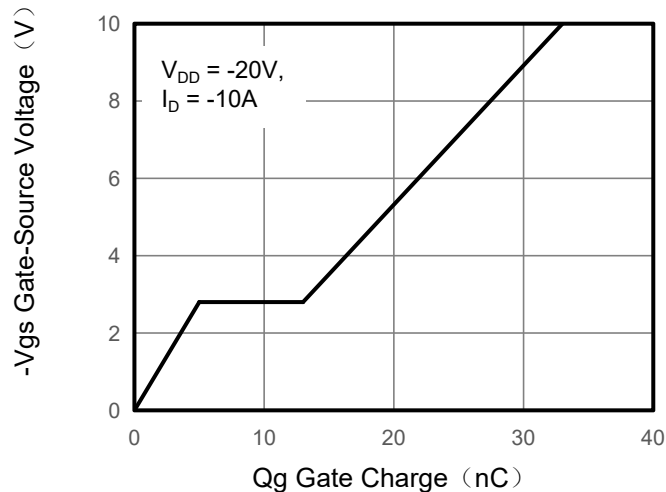


Figure 5. Capacitance

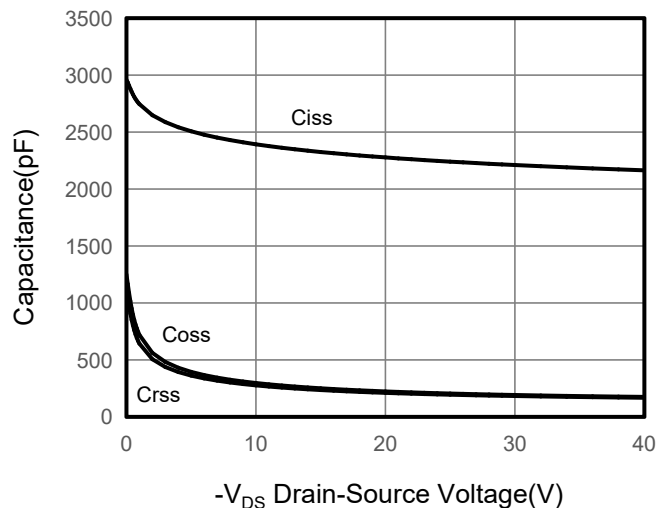
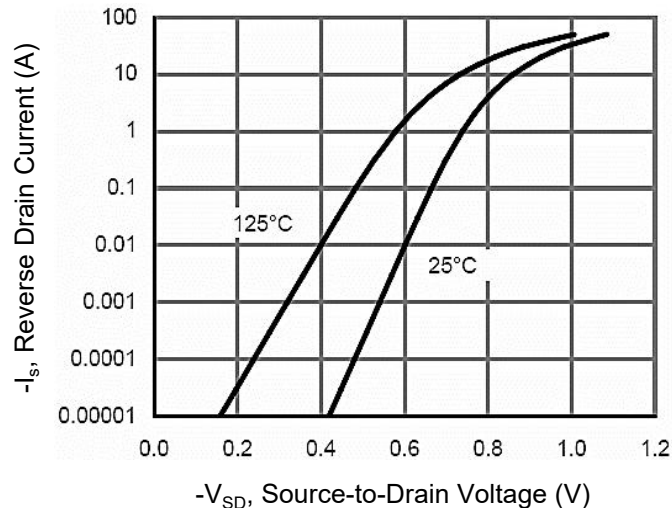


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

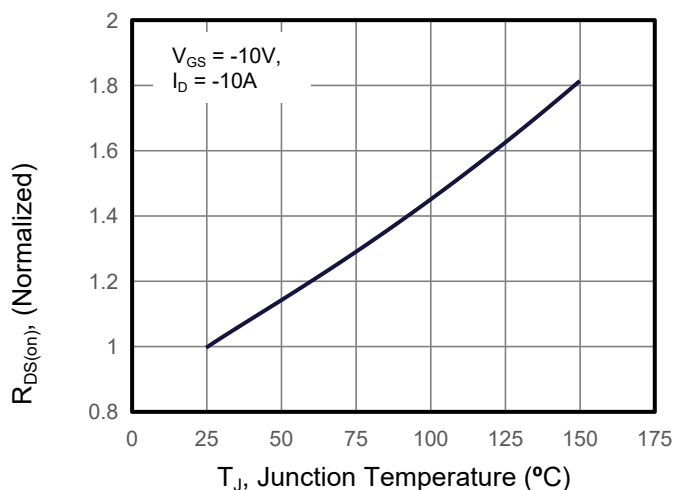


Figure 8. Safe Operation Area

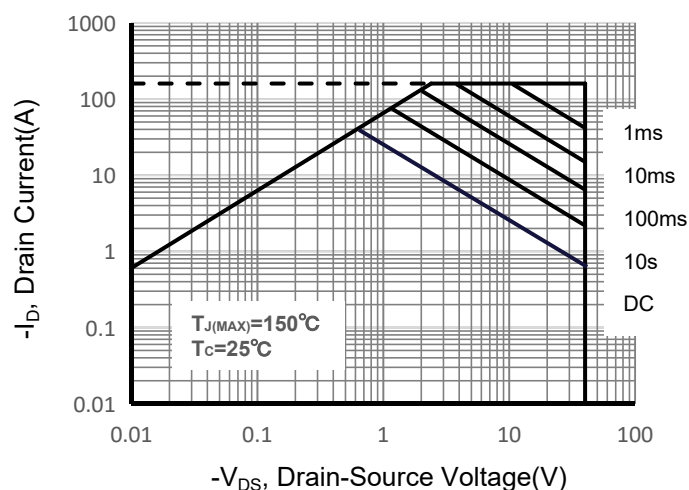


Figure 9. Maximum Continuous Drain Current vs Case Temperature

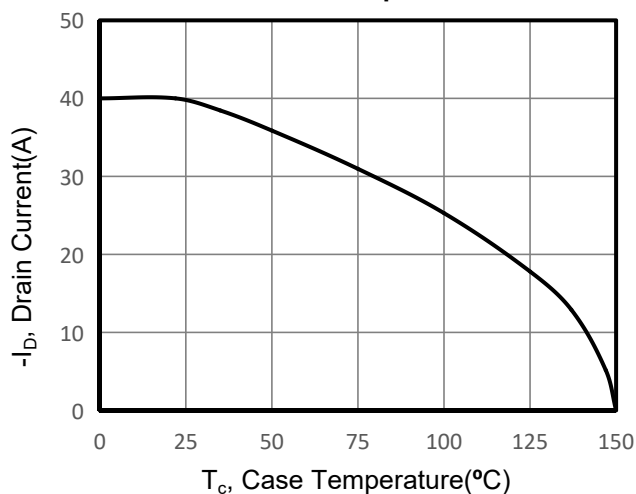
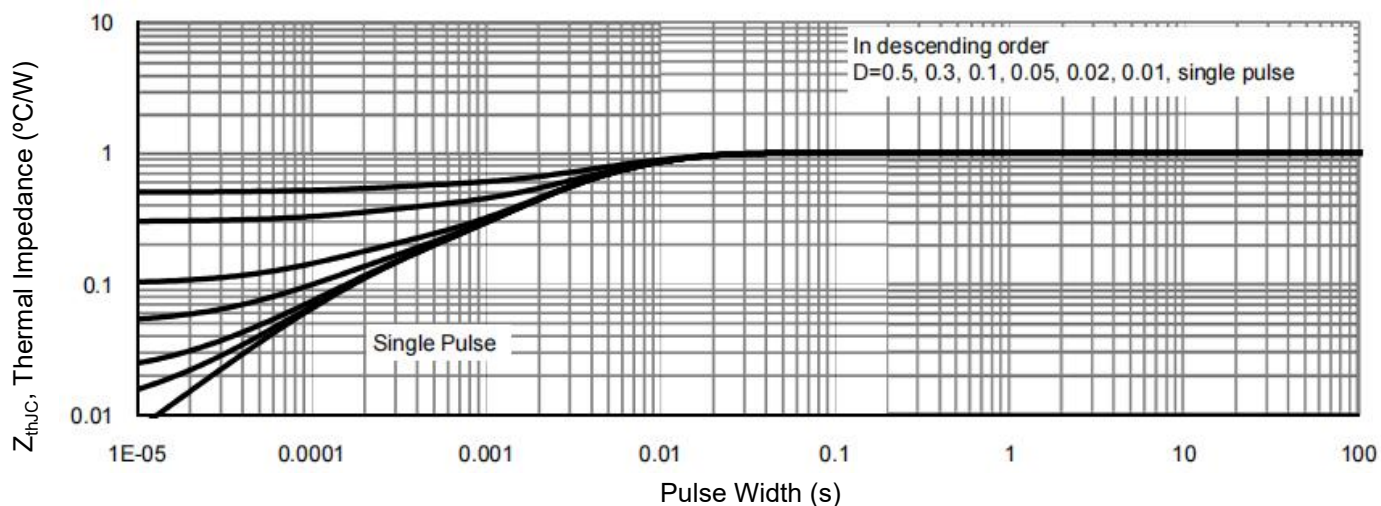
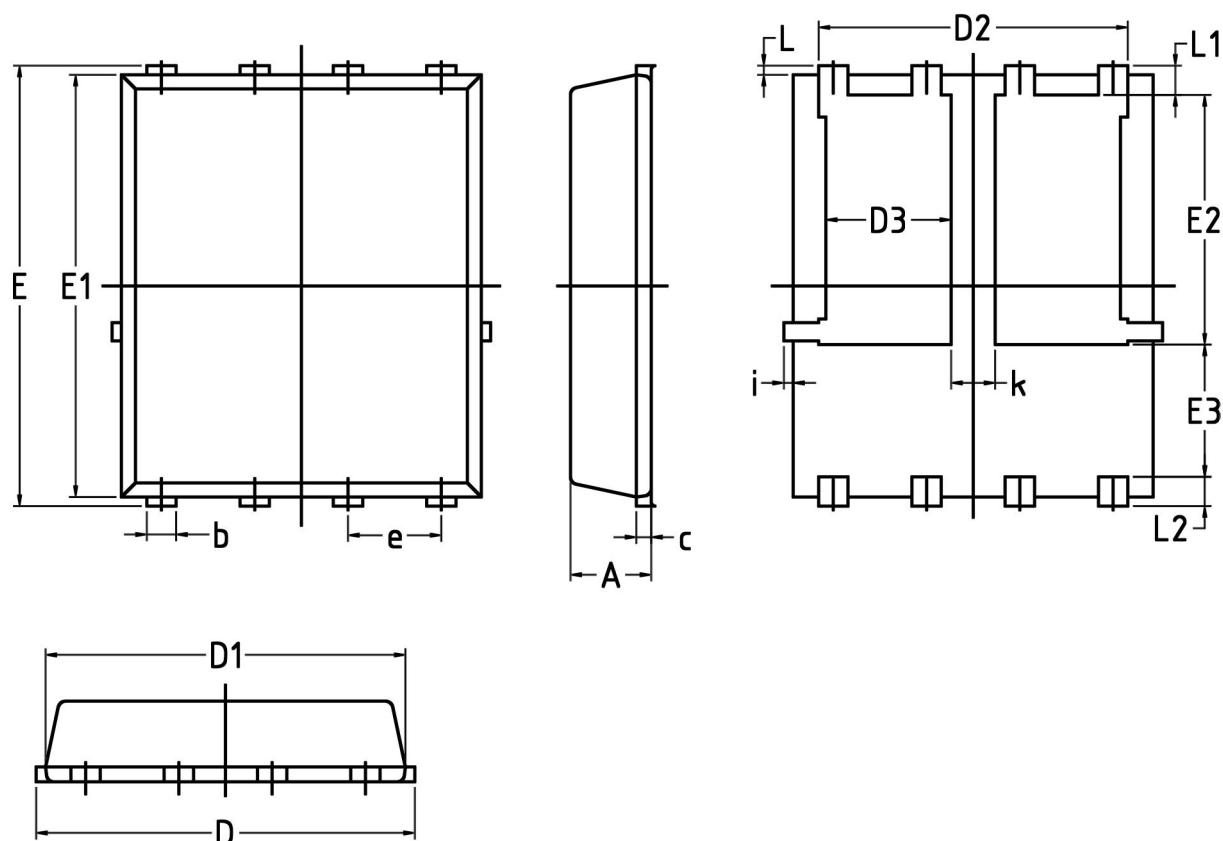


Figure 10. Normalized Maximum Transient Thermal Impedance



DFN5X6-8L Dual Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.203 BSC		0.0080 BSC	
D	4.80	5.40	0.1890	0.2126
D1	4.80	5.00	0.1890	0.1969
D2	4.11	4.31	0.1620	0.1700
D3	1.60	1.80	0.0629	0.0708
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	3.30	3.50	0.1300	0.1378
E3	1.70	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0019	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
i	/	0.18	/	0.0070
k	0.5	0.7	0.0197	0.0276