AW36801 VCSEL Laser Diode Driver for ToF Sensor

Features

- Anode common and floating driver
- Driver current up to 4.0A
- APC（Auto power control）function embedded
- Built-in Fail Safe function of LVDS input
- Over current detection of output driving current
- Diffuser issue detection
- APC process error detection
- AVCC33 Power Supply Monitor function
- Support Internal and External Temperature monitor
- Built-In 10-bit ADC for APC process and temperature measurement
- 10MHz 3-wire SPI interface
- WLCSP 2.23mmX2.23mmX0.45mm-25B, 0.4mm Pitch Package

Applications

- Smart Phone ToF application
- VR/AR devices
- AI Robots

General Description

The AW36801 is a highly-integrated VCSEL laser diode driver, used for ToF (Time of Flight) depth-detection sensor. In AW36801, up to 4A current driver, APC (Auto Power Control) process, 200MHz LVDS receiver and internal temperature sensor are integrated.

The APC process is implemented in AW36801, to optimize the output power and output current tr/tf performance with different external VCSEL laser diode. Configured through SPI interface, the APC process runs automatically and monitor the internal status during the process.

The AW36801 has a built-in 10-bit ADC, used to convert the PD voltage for APC process, also used to monitor the internal or external temperature.

Application Circuit

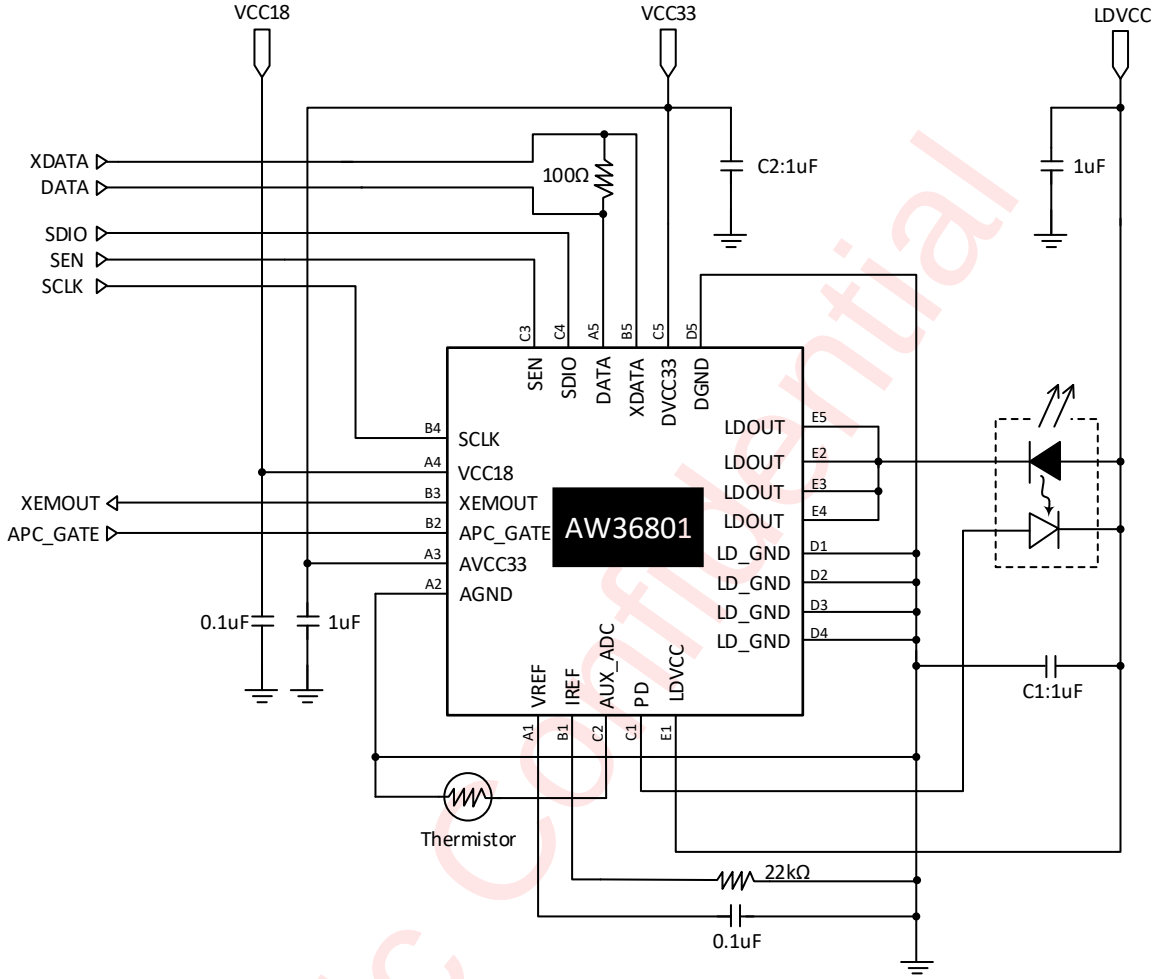


Figure 1 Typical Application Circuit of AW36801

Pin Configuration and Top Mark

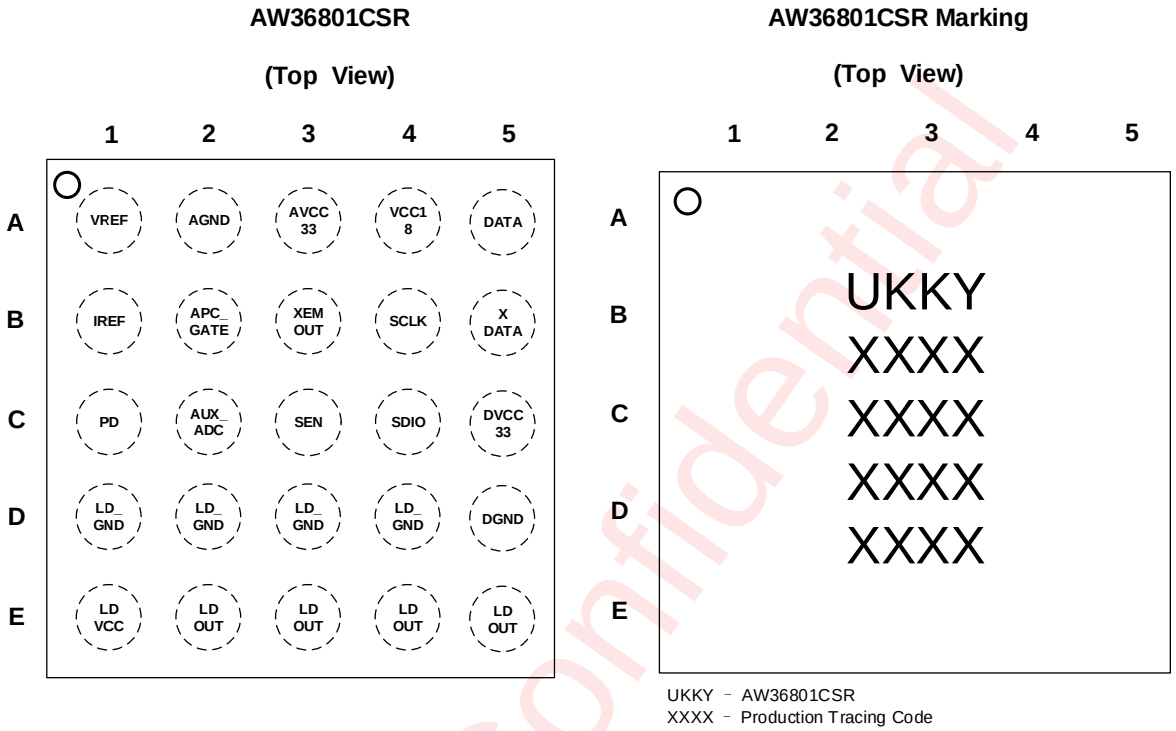


Figure 2 Pin Configuration and Top Mark

Pin Definition

PIN		Description
Number	Name	
A1	VREF	ADC reference voltage
A2	AGND	Analog ground
A3	AVCC33	Analog power supply 3.3V
A4	VCC18	Logic power supply 1.8V
A5	DATA	Timing pulse input for laser diode driver
B1	IREF	Reference current setting PIN
B2	APC_GATE	Input enable signal for laser emission
B3	XEMOUT	Emergency detection result output PIN
B4	SCLK	SPI serial clock
B5	XDATA	Timing pulse input for laser diode driver
C1	PD	PD input PIN
C2	AUX_ADC	External thermistor connection to internal ADC

C3	SEN	SPI serial enable signal
C4	SDIO	SPI serial data
C5	DVCC33	Digital power supply 3.3V
D1	LD_GND	Power ground of laser driver
D2	LD_GND	
D3	LD_GND	
D4	LD_GND	
D5	DGND	Digital power ground
E1	LDVCC	Power supply for laser diode 3.3V
E2	LDOUT	Laser diode current output PIN
E3	LDOUT	
E4	LDOUT	
E5	LDOUT	

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW36801CSR	-20°C～85°C	WLCSP 2.23mmX2.23mm X0.45mm-25B	UKKY	MSL1	ROHS+HF	4500 units/ Tape and Reel

Typical Application Circuits

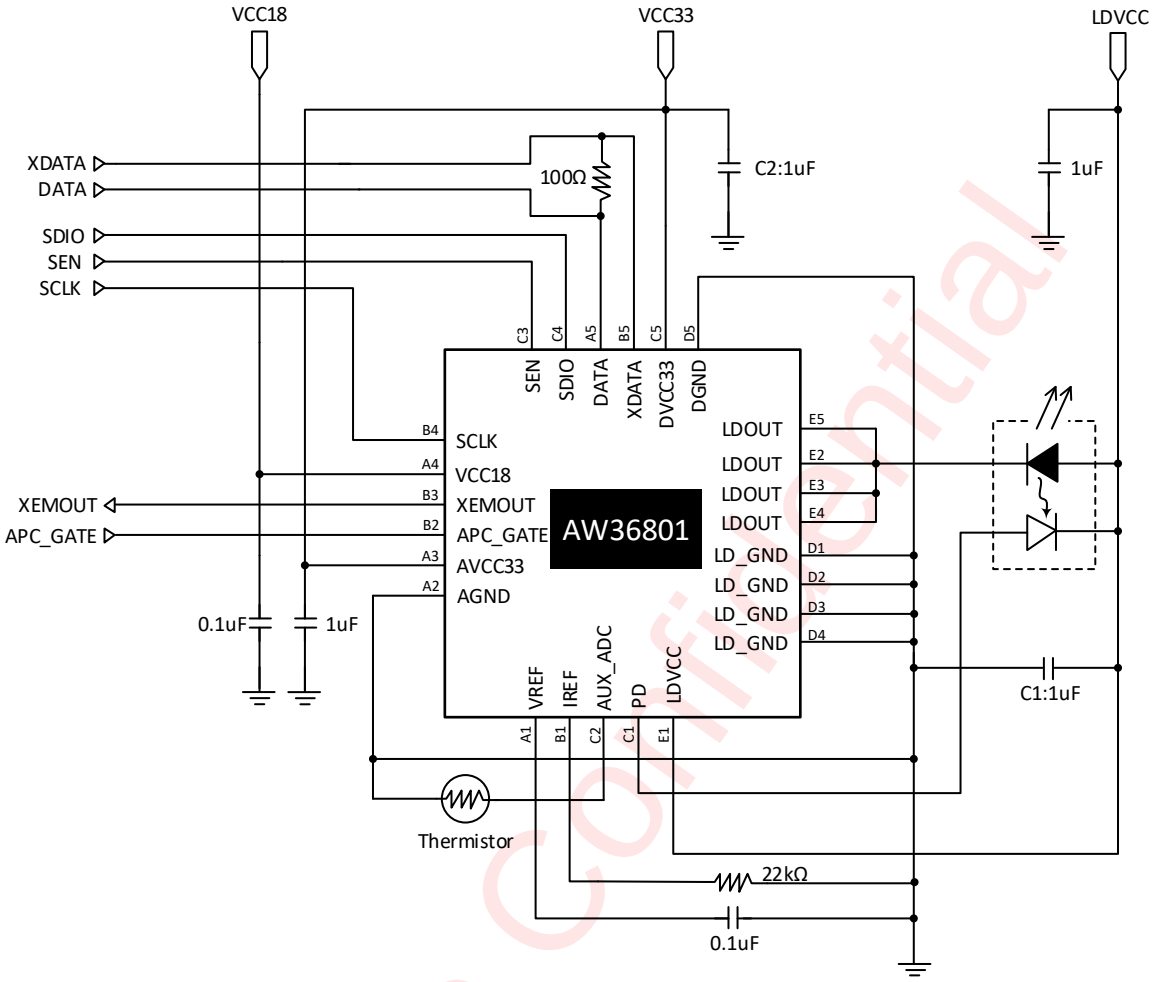


Figure 3 AW36801 Application Circuit

Notice for typical application circuits:

1：Please place power supply Caps to the chip as close as possible.

2：For the Cap C1&C2, is the important capacitance to constitute output return path.

※ 1. Recommend Low ESL capacitance;

※ 2. Please place the cap C1 in the shortest between LDVCC and LD_GND;

※ 3. Please place the cap C2 in the shortest between DVCC33 and DGND;

3：The LDOUT routing should be as short as possible, and connected widely.

4: Please design the board parasitism inductance of LDVCC and PD between LDOUT as small as possible.

Absolute Maximum Ratings(NOTE1)

PARAMETERS	MIN	MAX	UNIT
AVCC33, DVCC33, VCC18, LDVCC	GND-0.5	5.5	V
APC_GATE, DATA, XDATA, SCLK, SEN, SDIO, PD, AUX_ADC	GND-0.5	5.5	
SDIO, XEMOUT, LDOUT	GND-0.5	5.5	
Allowed power dissipation		1	W
Storage temperature	-65	150	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

ESD Ratings And Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 2)	±2	kV
CDM(NOTE 3)	±1.5	kV
Latch-Up(NOTE 4)	+IT: 200 -IT: -200	mA

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883K/Method 3015.9

NOTE3: Test method: ESDA/JEDEC JS-002-2018

NOTE4: Test method: JESD78E

Recommended Operating Conditions

PARAMETERS	MIN	NORM	MAX	UNIT
Supply voltage AVCC33/DVCC33	3.0	3.3	3.6	V
Supply voltage VCC18	1.65	1.8	1.95	V
Supply voltage LDVCC	3.0	3.3	5.5	V
LVDS frequency			200	MHz
Operating junction temperature T_J	-20		85	°C

Thermal Information

PARAMETERS	VALUE	UNIT
Junction-to-ambient thermal resistance θ_{JA}	64	°C /W

Electrical Characteristics

TA=25℃, AVCC33=DVCC33=LDVCC=3.3V, VCC18=1.8V for typical values (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption						
Icc33	VCC33 supply current @ Power save mode	DEEP_SLEEP=1	1	2	10	μA
	VCC33 supply current @ Standby mode	PS_MODE=0, APC_GATE=L	0.6	0.9	2.6	mA
	VCC33 supply current @ Laser emission	ADEN=1, APC_GATE=H, LDOUT Current 2A setting. Not include LDOUT current	18	26	29	mA
Icc_ldvcc	LDVCC supply current				2	μA
Icc18	VCC18 supply current				1.5	μA
LD Driver characteristics						
I_{swf}	Isw current full scale	VCC33=3.3V, LDOUT=1V, ISW_DAC=1111 1111	3.6	4.0	4.4	A
I_{sf}	Bias current full scale	VCC33=3.3V, LDOUT=1V, IBIAS_DAC=1111 1111	0.9	1.0	1.1	A
T_r	Rise time	Bottom=0.3A, Top=2A 10%-90%, LDOUT pin load condition 1.5V+0.2Ω//1nF		1.0		ns
T_f	Fall time			1.0		ns
T_{pdly}	Propagation delay	LVDS to LDOUT 50%		6		ns
T_{pdlyt}	Propagation delay temp. coefficient	LVDS to LDOUT 50%		2		ps/℃
APC						

V_{pdr}	PD pin input voltage range	As ADC input D-range	0.2		2.3	V
T_{apch}	APC_H emission time		3	4	5	μs
T_{apcl}	APC_L emission time		3	4	5	μs
T_{agl}	APC_GATE=L time		5			μs
T_{apc}	APC period				130	μs
Temperature sensor ADC						
T_{err}	Temperature error	0℃~105℃ after offset adjustment	-3		+3	℃
T_{adcres}	Resolution			10		bit
T_{conv}	Conversion time			80		μs
V_{ref}	Vref voltage of ADC		2.45	2.5	2.55	V
Emergency detection						
I_{thoc}	Over-current threshold	LDOUT=1V, OC_SEL=3'b001	2.9	3.2	3.5	A
VCC_{thoff}	LD off threshold of power supply VCC33	VCC33: 3.3V → 0V	2.65	2.8	2.95	V
VCC_{thon}	LD on threshold of power supply VCC33	VCC33: 0V → 3.3V	2.45	2.6	2.8	V
V_{por33}	VCC33 register reset voltage	VCC33: 3.3V → 0V		2	2.5	V
V_{por18}	VCC18 register reset voltage	VCC18: 1.8V → 0V		0.9	1.3	V
T_{lvds}	LVDS operating pulse width				0.5	μs
T_{lvds_em}	LVDS abnormal pulse width		2.5			μs
CMOS Logic						
V_{IL}	Input voltage logic low	SCLK, SEN, SDIO, APC_GATE	0		0.4	V
V_{IH}	Input voltage logic high		VCC18-0.5		VCC18	
I_{IH}	Input current logic high	SCLK, SEN, SDIO, APC_GATE (V_{IH}=1.8V)	5	9	14	μA
I_{IL}	Input current logic low	SCLK, SEN, SDIO, APC_GATE (V_{IH}=0V)	-1		1	μA
V_{OL}	Output voltage logic low	SDIO, I_{OL}=2mA	0		0.4	V

V_{OH}	Output voltage logic high	SDIO, EMOUT, I_{OH}=-2mA	VCC-0.4		VCC18	V
LVDS Input						
F_{MAX}	Operating frequency		0		200	MHz
V_{DR}	Input voltage range		0.5	0.8	1.9	V
V_{DTH}	LVDS differential input amplitude		0.1	0.15	1.0	V

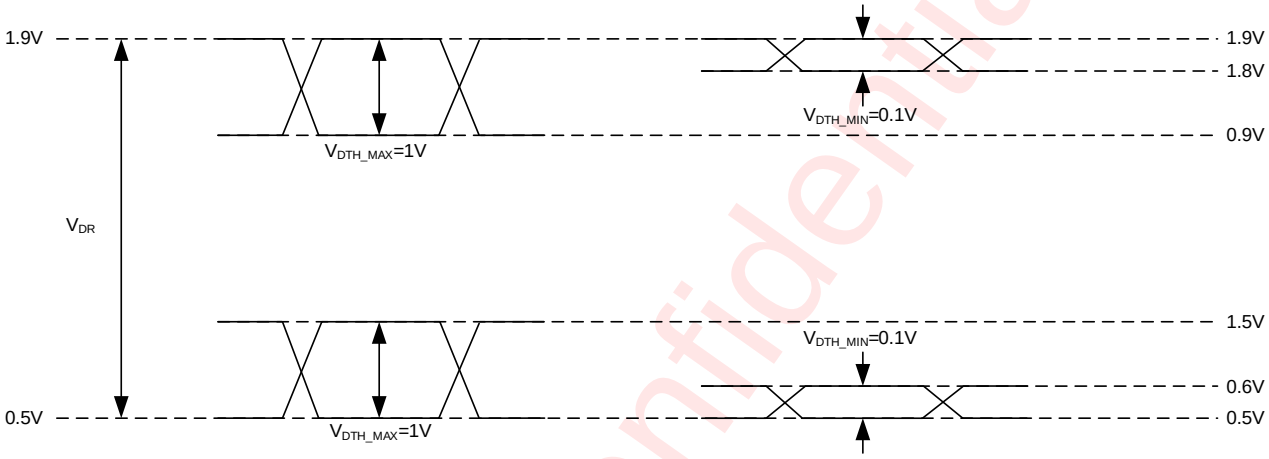


Figure 4 LVDS differential input

NOTE5: The DATA pin connect the positive level of the differential signal, and the XDATA pin connect the negative level of the differential signal.

SPI Interface Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
F_{sclk}	Operating frequency			10	MHz
T_{WH}	SCLK 'H' pulse width	26			ns
T_{WL}	SCLK 'L' pulse width	26			ns
T_{sse}	SEN setup time	30			ns
T_{hse}	SEN hold time	100			ns
T_{wlse}	SEN 'L' time	52			ns
T_{ssdi}	SDI setup time	30			ns
T_{hsdi}	SDI hold time	30			ns
T_{dsdo}	SDO output delay time			30	ns

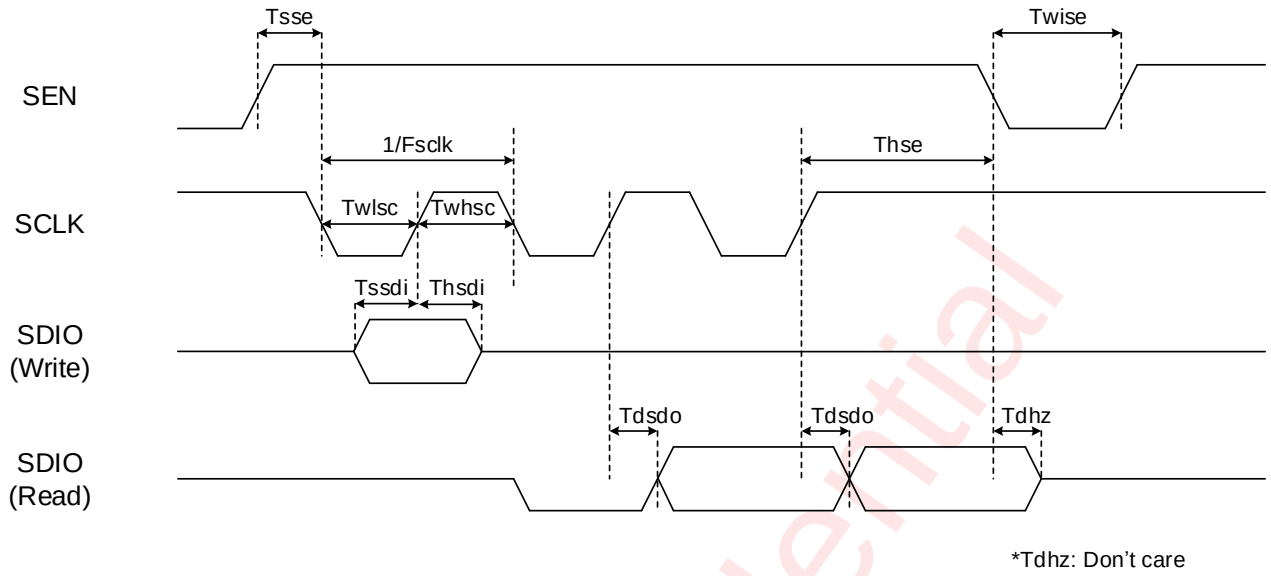


Figure 5 SPI timing relationships in the data transmission process

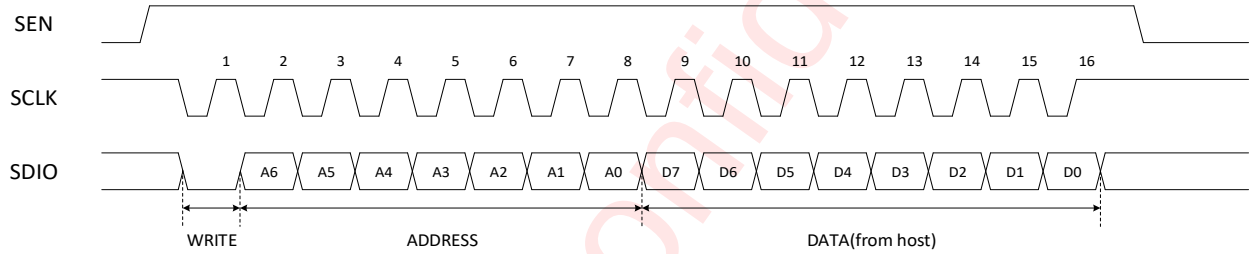
Serial I/F

Serial address bit definition

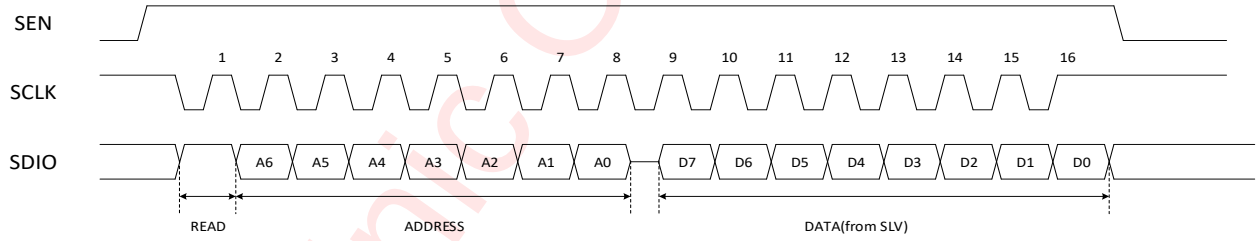
Bit	Bit Definition
A7	Read/Write select bit 0:Serial interface write mode 1:Serial interface read mode
A6:A0	Register address select bit-

Transmission and reception are performed in 16-bit units consisting of 8 address bits and 8 data bits. Both address and data are MSB first. The address switches to read or write mode by A[7].Read/Write supports continuous Read, continuous Write together.

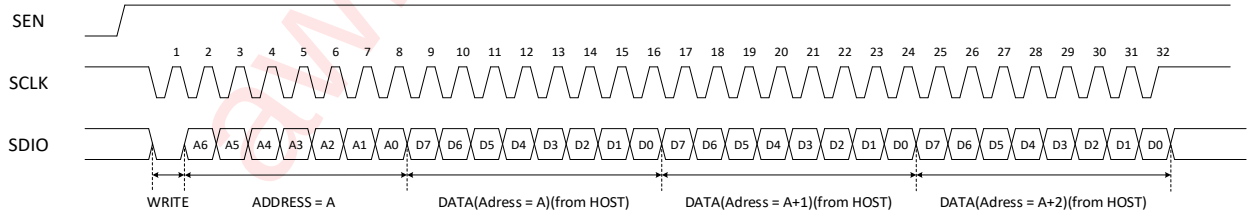
✧ Normal write



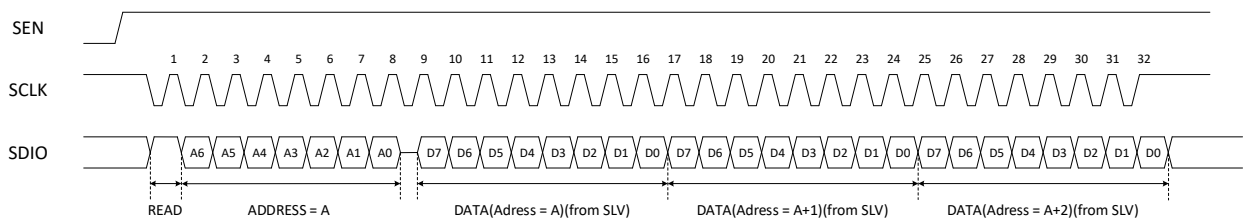
✧ Normal read



✧ Continuous write



✧ Continuous read



Functional Block Diagram

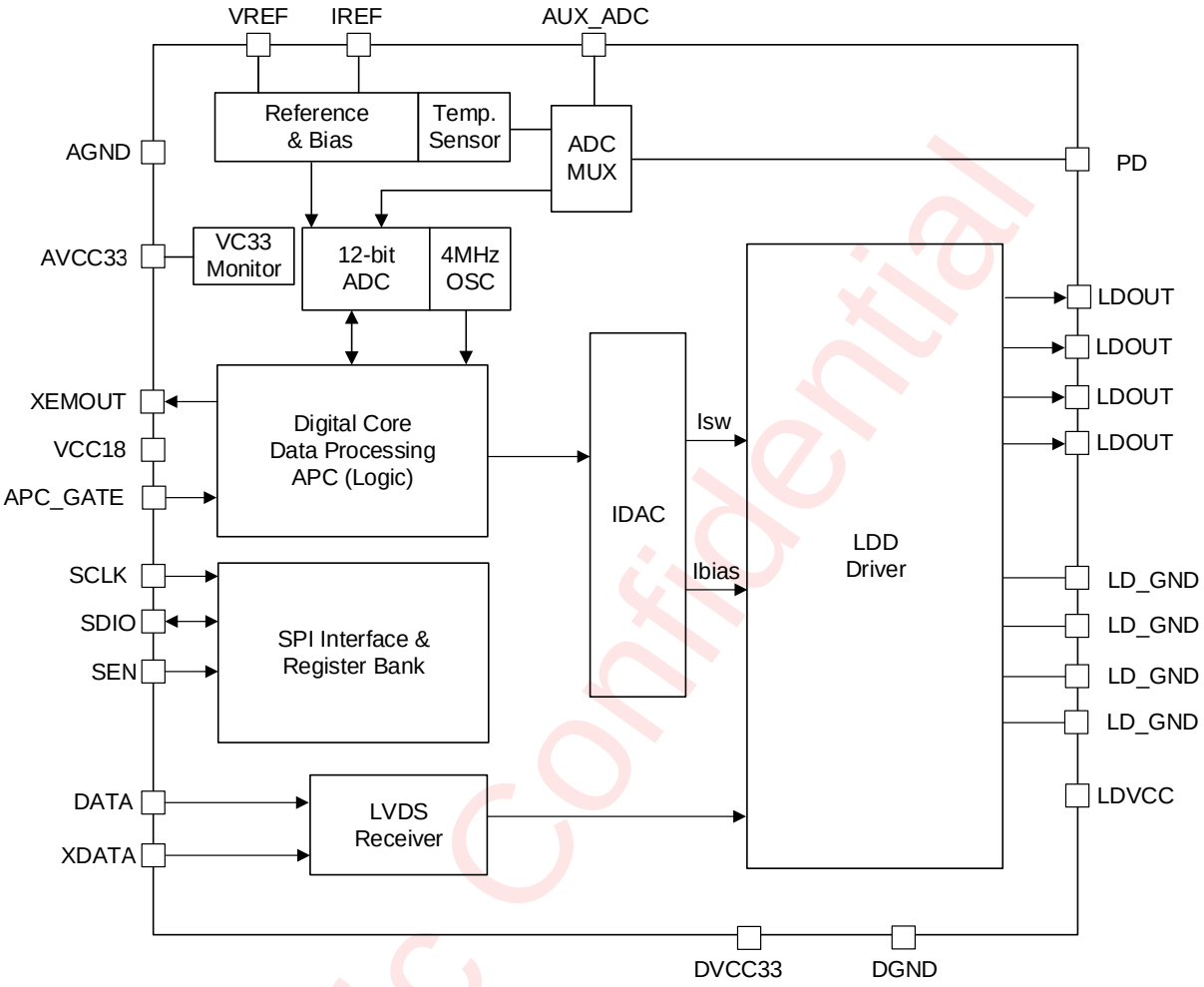


Figure 6 The AW36801 Function Block

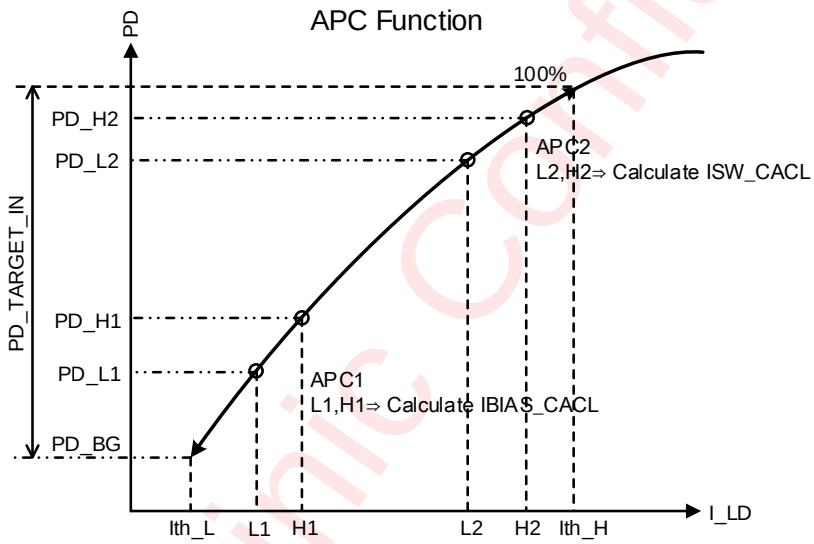
Detailed Functional Description

APC (Auto power control)

APC procedure is the essential function of AW36801, to calibrate the Laser driver to optimized output power and tr/tf performance. During about 130us after APC_GATE = High, AW36801 makes laser emit 4 level of light, L1/H1/L2/H2. Based on the photo diode (PD) current (voltage) , ADC inside of laser stores each level of light power and makes linear curve fitting to calculate IBIAS and ISW. Photo diode is required to make APC function. The calculated IBIAS and ISW values are applied to depth measurement period and IBIAS and ISW are updated when APC_GATE = High. This function contributes to laser temperature dependency performance, laser emitting timing and output power by time-related deterioration.

* Set APC_GATE on the following conditions to make APC process work correctly:

- Please set the APC process more than 130us for the time to DATA luminescence start from APC_GATE = High (start of the depth measurement) .
- Please secure the APC_GATE = Low section more than 5us.
- Please set registers which make the difference between H1 and L1 more than 30 digit.



APC function calculation method

In above figure,L1 = IBIAS_APCL1,H1 = IBIAS_APCH1,

L2 = IBIAS_CALC+ISW_APCL2, H2 = IBIAS_CALC+ISW_APCH2,

Using linear curve fitting method, can get:

$$Ith\_L = \frac{[IBIAS\_APCL1\times(PD\_H1-PD\_BG)]-[IBIAS\_APCH1\times(PD\_L1-PD\_BG)]}{PD\_H1-PD\_L1}$$

$$Ith\_H = \frac{[(IBIAS\_CALC+ISW\_APCL2)\times(PD\_H2-(PD\_TARGET\_IN+PD\_BG))]-[(IBIAS\_CALC+ISW\_APCH2)\times(PD\_L2-(PD\_TARGET\_IN+PD\_BG))]}{PD\_H2-PD\_L2}$$

Then，

IBIAS_CALC = Ith_L – IBIAS_BACK,

ISW_CALC = Ith_H – IBIAS_CALC,

Before APC, following initialization steps are required.

1.) Adjustment of PD resistance and RCFG_PD register

In I-L properties of the laser, 100% power equivalency sets driving current to be provided and confirms the return voltage to PD terminal by acquiring an ADC level at the time of the laser light emission in Read back. The PD terminal voltage must be less than or equal to ADC input range. Therefore, following steps are required to adjust the PD terminal resistance so that this return voltage reading is wished for (following steps ① to ④).

In addition, if PDSEL=1, please set the PD voltage by RCFG_PD, when PD does not have return light(following procedure ⑤ to ⑥); else if PDSEL=0, ignore the procedure ⑤ to ⑥.

① Set laser current to fixed current mode
APC_MODE[1:0] = 2b'11

② Based on laser I-L characteristics to set the fixed drive current
In IBIAS_FIX[7:0]: please set Ith (threshold current) of laser specifications.
In ISW_FIX[7:0]: please set a current value necessary to get 100% power than I-L properties of the laser.

③ Make APC_GATE = Low waiting more than 130us after making APC_GATE=High : Laser light emission and ADC movement.

④ By register Read back, Read laser light emission and each ADC level at the time of lights out (APC2_CHECK_DATA[9:0], PD_BG[9:0]) .
Adjust the PD conversion resistance to make these difference (APC2_CHECK_DATA - PD_BG) to become less than 737dec, but more than 654dec.
If PDSEL=0 (Use Internal resistance): Adjust Internal resistance with RCFG_PD[3:0] .
If PDSEL=1 (Use External resistance): Adjust External resistance.
(Repeat ③ to ④ by adjusting resistance until meet a condition).

⑤ Adjustment of the RCFG_PD set point (In case of PDSEL = 1)
Make APC_GATE = Lo waiting more than 130us after making APC_GATE = High: Laser light emission and ADC movement.

⑥ By register read back, AD level (PD_BG[9:0]) at the time of lights out, adjust by RCFG_PD[3:1] register to become less than 164dec, but more than 82dec.
(Repeat ⑤ to ⑥ by adjusting resistance until meet a condition).

2.) Initial power adjustment

Reflect PD terminal resistance value and the RCFG_PD (register value, that was determined in 1) and carry out ① to ④.

By register read back, read light emission and each ADC value of lights out (APC2_CHECK_DATA[9:0], PD_BG[9:0]) and calculate this difference (APC2_CHECK_DATA-PD_BG) .

And please memorize this difference value (APC2_CHECK_DATA-PD_BG) to an external memory as PD_TARGET_IN[9:0].

APC calibration and light emission for depth measurement

After APC_GATE is pull up to high signal, AW36801 enters into APC calibration period. By measuring ADC value of PD at several laser output conditions, BIAS current and SW current are calculated. The value stored in peripheral memory is written into PD_TARGET_IN[9:0] during initial sequence. SW current is determined by adjusting PD voltage to PD_TARGET_IN[9:0] during APC2 period. The following steps shows work flow from

APC to light emission for depth measurement.

By measuring ADC value at no emission (back ground) , ambient and offset of circuit are cancelled.

① Measure ADC value of PD voltage at LDOFF (no emission)

② Measure ADC value of PD voltage at L1 level (IBIAS_APCL1 [7:0])

③ Measure ADC value of PD voltage at H1 level (IBIAS_APCH1 [7:0])

※ L1 < H1 is required

④ From ①②③ results, calculated Ith and subtract IBIAS_BACK[6:0] using linear curve fitting method. Finally, BIAS current is determined.

⑤ Measure ADC value of PD voltage at L2 level (IBIAS_APCL2 [7:0] + ISW_APCL2 [7:0])

⑥ Measure ADC value of PD voltage at H2 level (IBIAS_APCH2 [7:0] + ISW_APCH2 [7:0])

※ L2 < H2 is required

⑦ From ⑤⑥ results, SW current is determined by adjusting photo diode voltage at IBIAS + ISW to PD_TARGET_IN[9:0] + PD_BG[9:0].

⑧ With calculated IBIAS current condition, check if the ADC value of PD voltage is correctly set.

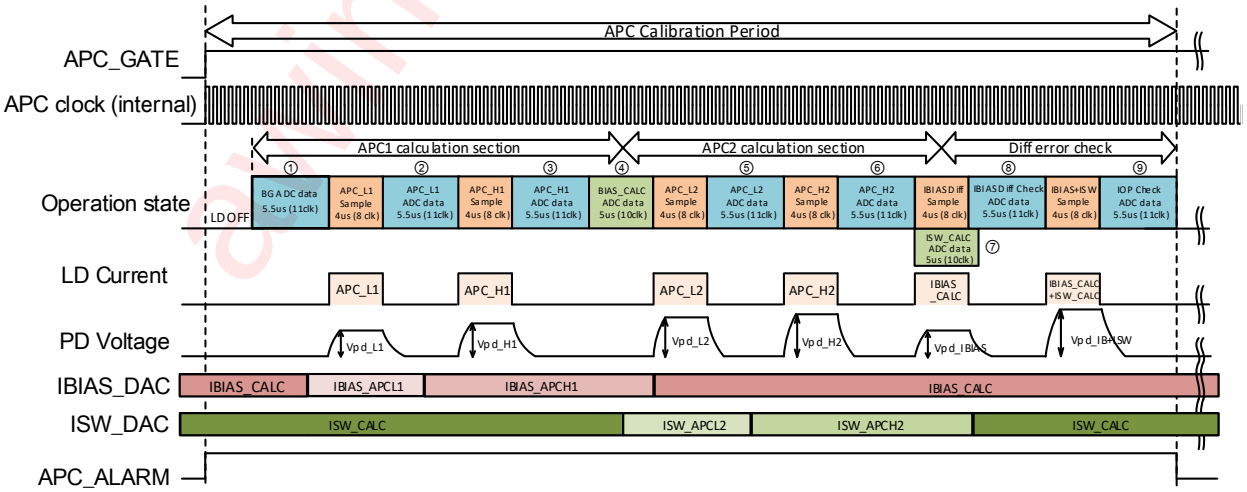
⑨ With calculated IBIAS + ISW current condition, check if the ADC value of PD voltage is correctly set.

If there is not any issue on results of ⑧ and ⑨, AW36801 shifts from APC calibration period to normal depth measurement state. If it detects error, register APC_ERR_MODE set off of LDOUT or activate LDOUT with certain level of current which is set by IBAIS_FIX[7:0] and ISW_FIX[7:0].

If PD_H1 [9:0] – PD_L1 [9:0] is 0 or negative value at APC1 calibration period or PD_H2 [9:0] – PD_L2 [9:0] is 0 or negative value at APC2 calibration period, it's possible to set LDOFF, error output at XEMOUT, and error flag stored into specific register address.

AW36801 cannot receive SPI input during ① to ⑨. APC calibration period is about 130us, and the mission pulse width at APC is 4us.

APC1 (IBIAS calculation) process and APC2 (ISW calculation) process can be set separately on or off by setting APC_MODE[1:0] register. If APC calibration is set to off, IBIAS_FIX[7:0] and ISW_FIX[7:0] register values are applied to set the laser drive currents.



APC calibration and light emission for depth measurement Timing Chart

Temperature Sensor ADC

ADC for temperature is used for either temperature sensor inside of AW36801 or external NTC input through AUX_ADC pad. ADSEL register can be set either case. It is required to take initial calibration to cancel offset of temperature sensor ADC inside of AW36801. (External thermistor cannot perform the initial calibration.)

1.) Initial calibration

In order to cancel the offset of the Internal circuit and temperature sensor and stores the acquired ADC data (at 25℃) to an external memory. The steps are below.

① Set ADEN = 2'b11 internal CLK activated

② At room temperature(25℃), set ADC_START = 2'b10 : internal AD activated. ADC result is stored into TEMP_DATA[9:0] register. After completing AD, automatically ADC_START set to 2'b00.

③ Read back TEMP_DATA[9:0] (ADC data at 25℃) register and store into peripheral memory in TEMP_INITIAL_IN[9:0].

Initial calibration is completed in the above.

2.) Temperature sensor function work flow (Performed only ②~④ in the case of external thermistor)

① At initial setting, stored value into peripheral memory is set into TEMP_INITIAL_IN[9:0] through SPI.

② At ADEN = 2'b11 : internal CLK activated.

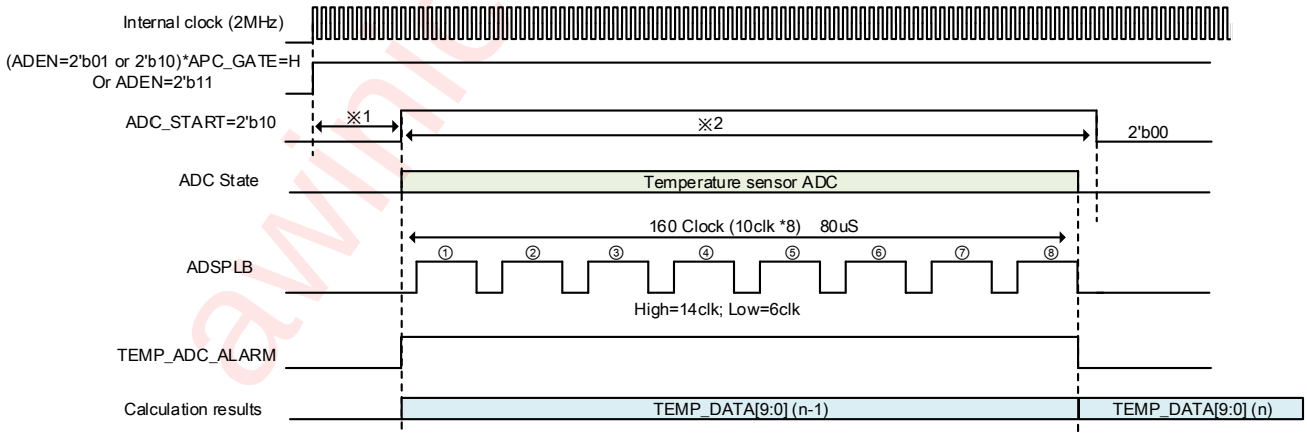
③ At ADC_START = 2'b10 : internal AD activated.

ADC result is stored into TEMP_DATA[9:0] register. After completing AD, automatically ADC_START set to 2'b00.

④ Read back TEMP_DATA[9:0] register.

⑤ Calculate the value of temperature by

(TEMP_DATA[9:0] dec- TEMP_INITIAL_IN[9:0] dec)/4.12[dec/℃]+25℃



※1: In case of ADEN=2'b01 or 2'b10, please set ADC_START=2'b10 after more than 130uS.

※2: Don't switch the APC_GATE during AD conversion time (100uS).

※3: In case of APC_EN=1'b1, please set PS_MODE=1'b1, ADEN=2'b11 and APC_GATE=L/Open.

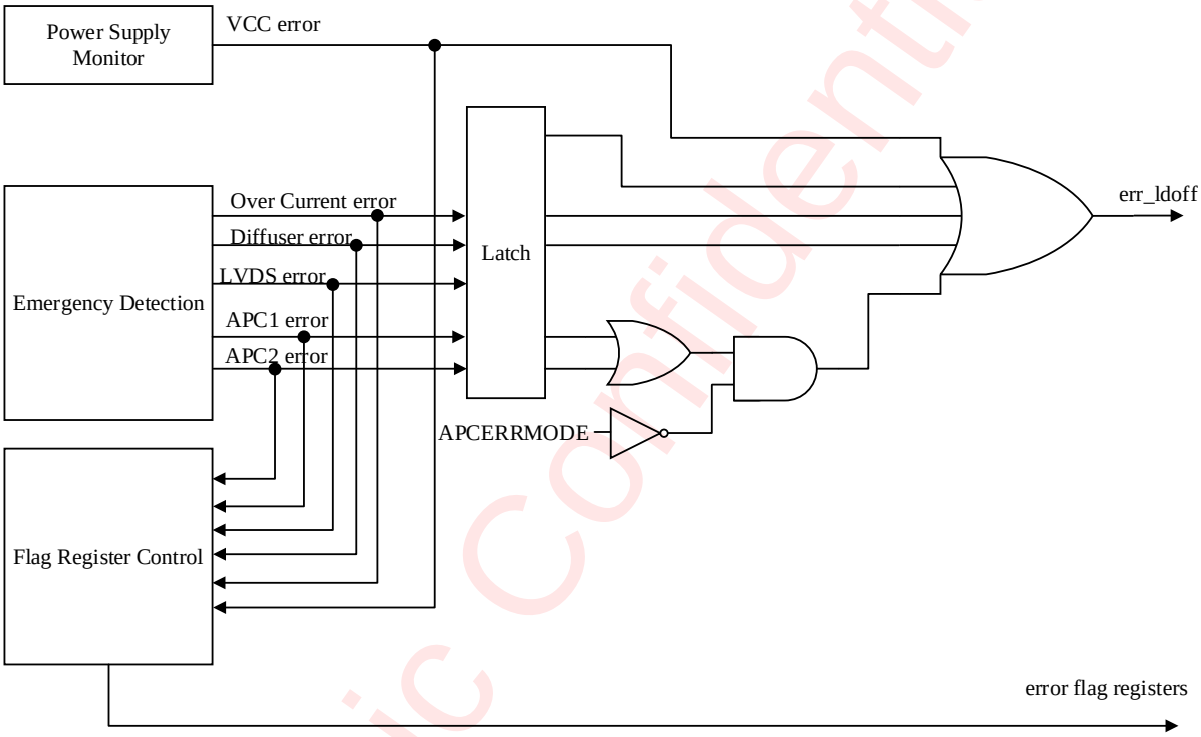
Emergency Detection Function

Emergency detection function is for power supply monitor, over current, diffuser removal detection, APC1 error, and APC2 error.

When AW36801 detects abnormal phenomena by taking OR or all of functions, then AW36801 execute processing as shown in below.

- Turn OFF LDOUT (no signal output to laser)
- Output error flag to XEMOUT pad (Low output at error detected case)
- Error flag is stored into register (`1` is for error case, can be reset by dummy write to the register)

Each detection function can be set on or off by register setting except power supply monitor function. Error flag stored into register is kept after error is even cancelled. To reset error flag, dummy write of register or global reset are required.



Emergency Detection Function

stored register of Emergency Error flag

Bit	7	6	5	4	3	2	1	0
Name	APC2_EM	APC1_EM	VCC_EM	DIF_EM	OC_EM	-	LVDS_EM	-
0	Normal					-	Normal	-
1	Error					-	Error	-

1.) Power Supply Monitor

Power Supply Monitor function monitors AVCC33 voltage in operating. When the voltage is under 2.6V, it becomes error. Once it recovers to over 2.8V, error signals of LDOFF and XEMOUT are reset. However, error flag stored into register is kept.

2.) Over Current

Over current function monitors IBIAS_CALC [7:2] and ISW_CALC[7:0] current which are calculated by APC process. OC_SEL [2:0] set over current threshold level and when IBIAS_CALC [7:2] + ISW_CALC [7:0]

is larger than equivalent of threshold level of OC_SEL[2:0], it becomes error.

OC_SEL[2：0]	Over Current Threshold level
000	3.7A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=233dec)
001	3.1A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=200dec)
010	2.6A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=167dec)
011	2.1A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=133dec)
100	1.7A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=107dec)
101	1.3A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=80dec)
110	0.8A(IBIAS_CALC[7:2]+ISW_CALC[7:0]=53dec)
111	Disable Over Current detection

3.) Diffuser Issue Detection

Diffuser Issue Detection function monitors ADC value of photo diode voltage which is calculated by APC calibration (IBIAS +ISW) . When the ADC value is less than PD_BG[9:0] (Background) + 128dec, AW36801 detects error. This detection is activated during APC calibration period.

DIF_ERR_SEL[1：0]	Diffuser removal detection
00	Less than PD_BG[9:0] + 128dec
01	Less than PD_BG[9:0] + 64dec
10	Less than PD_BG[9:0] + 32dec
11	Function off

4.) APC1 error

APC1 error function monitors AD value of photo diode with IBIAS calculated at APC1 period. This detection APC calibration period.

APC1_ERR_SEL	Detect errors in APC1
0	Error is flag if IBIAS<0，or PD voltage is larger than PD_BG[9:0]+64dec
1	Function off

5.) APC2 error

APC2 error function monitors AD value of photo diode with IBIAS+ISW calculated at APC1 and APC2 period. AD value is compared to PD_TARGET_IN [9:0]. This detection is activated during APC calibration period.

APC2_ERR_SEL[1:0]	Detect errors in APC1
00	Error: Larger than PD_TARGET_IN + PD_BG ±64dec (6.25% of PD full scale)
01	Error: Larger than PD_TARGET_IN + PD_BG ±128dec (12.5% of PD full scale)
10	Error: Larger than PD_TARGET_IN +PD_BG ±256dec (25% of PD full scale)
11	Function off

6.) LVDS pulse width detection

It monitors LVDS input signal, if the H pulse continuously (≥2.5μs) is input, detection result is identified as error. This function operates in integration period.

When DISLVDS_PED set "1", this function doesn't operate.

DISLVDS_PED	Detect errors in APC1
0	Error when width of high pulse for LVDS signal is larger than 2.5μs
1	Function off

7.) APC_ERR_MODE

APC_ERR_MODE controls output of LDOUT pad and output of XEMOUT when APC1 error or APC2 error. Register APC_ERR_MODE controls LDOUT and XEMOUT.

APC_ERR_MODE	Output control at APC1, or APC2 error
0	Turn off LDD, output XEMOUT='0'
1	Fix IBAS and ISW to IBIAS_FIX and ISW_FIX; XEMOUT='1', store error flag into register

8.) Output processing at the time of the abnormal detection function and error outbreak

VCC error:

Item	Contents	Selection of the detection function	LDOUT output	XEMOUT output	VCC_EM
VCC ERROR	Monitor the VCC voltage	Always active	HiZ (no current flow)	Low	1

APC1 error:

				Output processing when error occurs					
				APC_ERR_MODE = 0			APC_ERR_MODE = 1		
Item	Sub item	Contents	Selection of the detection function	LDOUT output	XEMOUT output	APC1 _EM	LDOUT output	XEMOUT output	APC1 _EM
APC1	APC1 Calibration error ※④	PD_H1-PD_L1≤0: Error	Always active	HiZ (no current flow)	Low	1	Set LD current at IBIAS_FIX , ISW_FIX	High	1

		Negative Ith	APC1_ERR_SEL=0, detection function on	HiZ (no current flow)	low	1	Set LD current at IBIAS_FIX, ISW_FIX	High	1
			APC1_ERR_SEL=1, detection function off						
	APC1 Check ※⑧	Ith<0; or APC1_CHECK_DATA≥PD_BG+64dec	APC1_ERR_SEL=0, detection function on	HiZ (no current flow)	Low	1	Set LD current at IBIAS_FIX, ISW_FIX	High	1
			APC1_ERR_SEL=1, detection function off						

APC2 error:

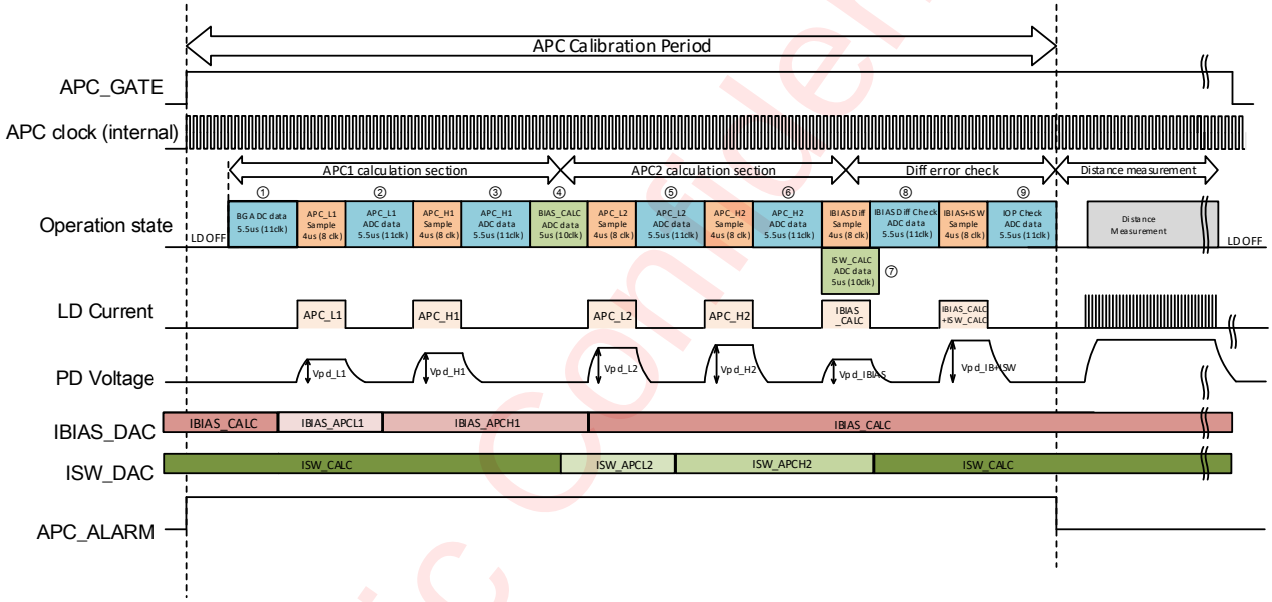
				Output processing when error occurs					
				APC_ERR_MODE = 0			APC_ERR_MODE = 1		
Item	Sub item	Contents	Selection of the detection function	LDOUT output	XEMOUT output	APC2_EM	LDOUT output	XEMOUT output	APC2_EM
APC2	APC2 Calibration error ※⑦	PD_H2-PD_L2 ≤0: Error	Always active	HiZ (no current flow)	Low	1	Set LD current at IBIAS_FIX, ISW_FIX	High	1
		Negative ISW_CALC	APC2_ERR_SEL≠2'b11, detection function on	HiZ (no current flow)	low	1	Set LD current at IBIAS_FIX, ISW_FIX	High	1
			APC2_ERR_SEL=2'b11, detection function on						
	APC2 Check ※⑨	ISW_CALC<0; or APC2_CHECK_DATA is larger than that in APC2_ERR_SEL	APC2_ERR_SEL≠2'b11, detection function on	HiZ (no current flow)	Low	1	Set LD current at IBIAS_FIX, ISW_FIX	High	1
			APC2_ERR_SEL=2'b11, detection function on						

OC error:

			Output processing when error occurs					
			OC_CLAMP = 0			OC_CLAMP = 1		
Item	Contents	Selection of the detection function	LDOUT output	XEMOUT output	OC_EM	LDOUT output	XEMOUT output	OC_EM
OC ERROR ※⑨	Monitor that if the current IBIAS_CALA+ISW_CALC is larger than 3.7A/3.2A/2.7A/2.2A/1.7A/1.3A/0.8A	OC_SEL≠2'b11, detection function on	HiZ (no current flow)	Low	1	Clamp the current at OC level as defined in OC_SEL[2:0]	High	1
		OC_SEL = 2'b11, detection function off						

Diffuser error:

Item	Contents	Selection of the detection function	LDOUT output	XEMOUT output	DIF_EM
Diffuser ERROR ※⑨	Check APC2_CHECK_DATA ≤PD_BG + 128dec / 64dec / 32dec	DIF_ERR_SEL≠ 2'b11, detection function on	HiZ (no current flow)	Low	1
		DIF_ERR_SEL = 2'b11, detection function off			



APC process and DATA Emission

Laser output assist function

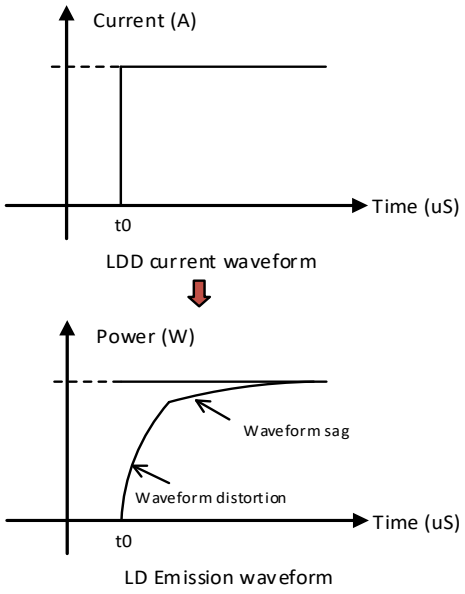
Due to PCB board design and Laser Diode (LD) load, LD emission waveform has sag and distortion. DRV_SAG function is capable to compensate sag, DRV_AS_W and DRV_AS functions compensate distortion. (adjustment flow)

① evaluate LD emission waveform with DRV_SAG, DRV_AS_W, DRV_AS default values.

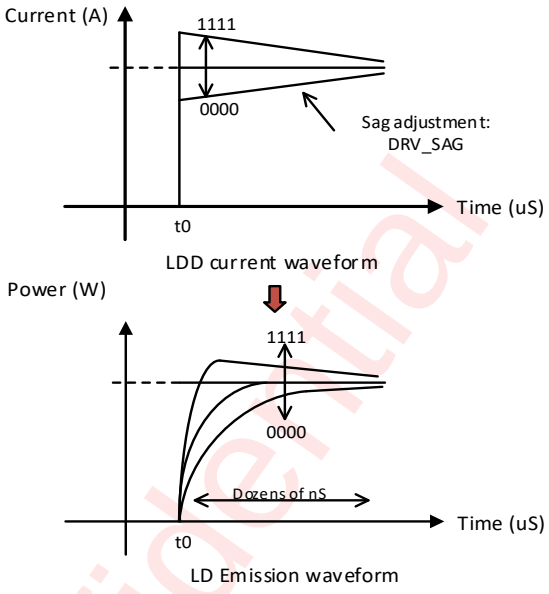
② flattening of sag with DRV_SAG compensation function

③ adjust DRV_AS_W, DRV_AS for distortion

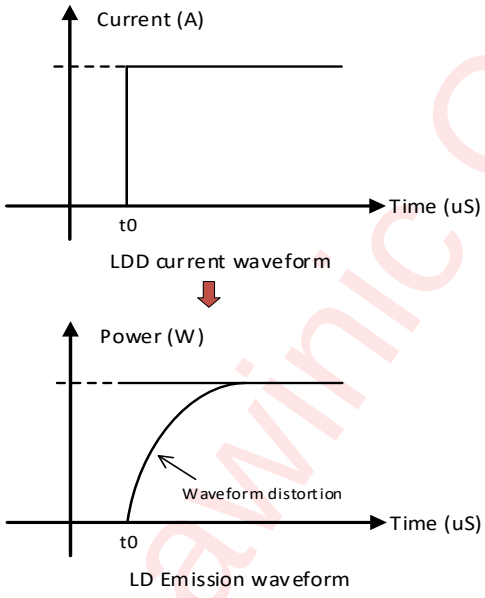
① Recommended setting



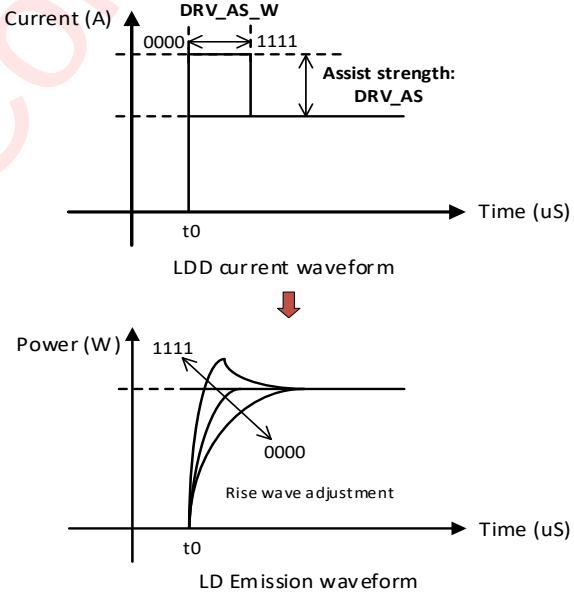
② DRV_SAG adjustment



③ After DRV_SAG adjustment



④ DRV_AS_W,DRV_AS adjustment



Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	**MODE**	R/W	RSTDIS	-		APCEN	APC_MODE		PSMODE	SLEEP	0x00
0x01	**APCL1**	R/W	IBIAS_APCL1								0x00
0x02	**APCH1**	R/W	IBIAS_APCH1								0x00
0x05	**APCL2**	R/W	ISW_APCL2								0x00
0x06	**APCH2**	R/W	ISW_APCH2								0x00
0x07	**IBSFIX**	R/W	IBIAS_FIX								0x00
0x08	**ISWFIX**	R/W	ISW_FIX								0x00
0x09	**IBSBK**	R/W	-	IBIAS_BACK							0x00
0x0A	**TMPPD_H**	R/W	-				TEMP_INITIAL_IN[9:8]		PD_TARGET_IN[9:8]		0x00
0x0B	**PDTGT_L**	R/W	PD_TARGET_IN[7:0]								0x00
0x0C	**TMPIN_L**	R/W	TEMP_INITIAL_IN[7:0]								0x00
0x0D	**OFFSET**	R/W	PDSEL	IAUX_OFFSET			RCFG_PD				0x00
0x0E	**ERRSEL**	R/W	OC_ CLAMP	APC2_ERR_SEL		APC1_ ERR_SEL	APC_ERR _MODE	OC_SEL			0x00
0x0F	**TRAS**	R/W			DIF_ERR_SEL		DRV_AS				0x0C
0x10	**ASIW**	R/W	DRV_SAG				DRV_AS_W				0x46
0x12	**LVDSCTR**	R/W	-					DRVLVDS	-	DISLVDS_ PED	0x00
0x13	**ADCMODE**	R/W	-		ADC_START		-	ADSEL	ADEN		0x01
0x14	**ADALARM**	R	TEMP_ADC _ALARM	APC_AL ARM	-				TEMP_DATA[9:8]		0x00
0x15	**TMPDATA_L**	R	TEMP_DATA[7:0]								0x00
0x18	**IBSCALC**	R	IBIAS_CALC								0x00
0x19	**ISWCALC**	R	ISW_CALC								0x00
0x1A	**PDBGLH1_H**	R	PD_L2[9:8]		PD_H1[9:8]		PD_L1[9:8]		PD_BG[9:8]		0x00
0x1B	**PDCHK_H**	R	-		APC2_CHECK_DATA[9:8]		APC1_CHECK_DATA[9:8]		PD_H2[9:8]		0x00
0x1C	**PDBG_L**	R	PD_BG[7:0]								0x00
0x1D	**PDL1_L**	R	PD_L1[7:0]								0x00
0x1E	**PDH1_L**	R	PD_H1[7:0]								0x00
0x1F	**PDL2_L**	R	PD_L2[7:0]								0x00
0x20	**PDH2_L**	R	PD_H2[7:0]								0x00
0x21	**APC1CHK_L**	R	APC1_CHECK_DATA[7:0]								0x00
0x22	**APC2CHK_L**	R	APC2_CHECK_DATA[7:0]								0x00
0x23	**SA_EM**	R	APC2_EM	APC1_E M	VCC_EM	DIF_EM	OC_EM	-	LVDS_EM	-	0x00
0x24	**VER**	R	-					VERSION			0x00
0x25	**GLRST**	W	GL_RST								0x00

Register Description

MODE：Mode Register(Address 00H)

Bit	Symbol	R/W	Description	Default
7	RSTDIS	R/W	Global reset (GLRST) enable control by serial interface. 0 : Enable (default) 1 : Disable	0x00
6	-	R/W	Reserved	
5	-	R/W	Reserved	
4	APCEN	R/W	Enable of ACC (Auto Current Control)MODE 0: APC MODE 1: IBIAS,ISW drives a laser by a fixed electric current depending on IBIAS_FIX[7:0] and ISW_FIX[7:0].	
3:2	APC_MODE	R/W	Selection of APC (Auto Power Control) MODE (enable in APC_EN=0) 00: APC1(IBIAS calculation)=ON,APC2(ISW calculation)=ON Laser-driven current with IBIAS,ISW calculated in APC 01: APC1(IBIAS calculation)=ON,APC2(ISW calculation)=OFF Laser-driven current with IBIAS calculated in APC,ISW depending on ISW_FIX[7:0] (a fixed current)set point 10: APC1(IBIAS calculation)=OFF,APC2(ISW calculation)=ON Laser-driven current with ISW calculated in APC,IBIAS depending on IBIAS_FIX[7:0] (a fixed current)set point 11: APC1(IBIAS calculation)=OFF,APC2(ISW calculation)=OFF Laser-driven current with IBIAS,ISW depending on IBIAS_FIX[7:0], ISW_FIX[7:0] set point	
1	PSMODE	R/W	Interlocking movement control with APC_GATE of Power Save of the Driver, IDAC, LVDS circuit 0: Interlocking movement control with APC_GATE (default) APC_GATE=Low : Standby APC_GARE=High: Active 1: Don't Interlocking movement control with APC_GATE Always Active(Please use APC_GATE as Low or Open)	
0	SLEEP	R/W	The control of power save in deep sleep of all tip circuits 0: Active (default) 1: Deep Sleep Power Save	

APCL1：APCL1 Current Value Register(Address 01H)

Bit	Symbol	R/W	Description	Default

7:0	IBIAS_APCL1	R/W	Ibias current setting of APC_L1 0000 0000: 0A (default) …… 1111 1111: 1.00A (3.92mA/step)	0x00

APCH1：APCH1 Current Value Register(Address 02H)

Bit	Symbol	R/W	Description	Default
7:0	IBIAS_APCH1	R/W	Ibias current setting of APC_H1 0000 0000: 0A (default) …… 1111 1111: 1.00A (3.92mA/step)	0x00

APCL2：APCL2 Current Value Register(Address 05H)

Bit	Symbol	R/W	Description	Default
7:0	ISW_APCL2	R/W	Isw current setting of APC_L2 0000 0000: 0A (default) …… 1111 1111: 4.0A (15.7mA/step)	0x00

APCH2：APCH2 Current Value Register(Address 06H)

Bit	Symbol	R/W	Description	Default
7:0	ISW_APCH2	R/W	Isw current setting of APC_H2 0000 0000: 0A (default) …… 1111 1111: 4.0A (15.7mA/step)	0x00

IBSFIX：Ibias Fixed Current Value Register(Address 07H)

Bit	Symbol	R/W	Description	Default
7:0	IBIAS_FIX	R/W	Fixed current setting of Ibias 0000 0000: 0A (default) …… 1111 1111: 1.00A (3.92mA/step)	0x00

ISWFIX：Isw Fixed Current Value Register(Address 08H)

Bit	Symbol	R/W	Description	Default
7:0	ISW_FIX	R/W	Fixed current setting of Isw 0000 0000: 0A (default) …… 1111 1111: 4.0A (15.7mA/step)	0x00

IBSBK：Ibias Offset Current Value Register(Address 09H)

Bit	Symbol	R/W	Description	Default
7	-	R/W	Reserved	0x00
6:0	IBIAS_BACK	R/W	Offset current setting from Ibias calculation result to minus 000 0000: 0A (default) …… 111 1111: 0.5A (3.92mA/step)	

TMPPD_H：AD Level Input Register(Address 0AH)

Bit	Symbol	R/W	Description	Default
7:4	-	R/W	Reserved	0x00
3:2	TEMP_INITIAL_IN[9:8]	R/W	AD level input of the revisionless 25degrees Celsius temperature sensor. Higher 2Bit (input from external memory)	
1:0	PD_TARGET_IN[9:8]	R/W	AD level input of the PD target. Higher 2Bit (input from external memory)	

PDTGT_L：PD Target In Register(Address 0BH)

Bit	Symbol	R/W	Description	Default
7:0	PD_TARGET_IN[7:0]	R/W	AD level input of the PD target. Lower 8Bit (input from external memory)	0x00

TMPIN_L：AD Level Input Register(Address 0CH)

Bit	Symbol	R/W	Description	Default
7:0	TEMP_INITIAL_IN[7:0]	R/W	AD level input of the revisionless 25degrees Celsius temperature sensor. Lower 8Bit (input from external memory)	0x00

OFFSET：Offset Current Value Register(Address 0DH)

Bit	Symbol	R/W	Description	Default
7	PDSEL	R/W	Select internal or external PD resistance 0: Internal (default) 1: External	0x00
6:4	IAUX_OFFSET	R/W	AUX_ADC terminal offset current setting 000: OFF 001: 20uA 010: 40uA 011: 80uA 100: 160uA 101: 320uA 110: 640uA 111: 1280uA	
3:0	RCFG_PD	R/W	PD terminal offset current setting (Higher 3Bit) (when PDSEL=1) 000: OFF 001: 20uA 010: 40uA 011: 80uA 100: 160uA 101: 320uA 110: 640uA 111: 1280uA Conversion resistance and Offset current setting of PD photoelectric(when PDESL=0) 0000:OPEN 0001:OPEN 0010:12.8k(20uA) 0011:8.96k(20uA) 0100:6.4k(40uA) 0101:4.48k(40uA) 0110:3.2k(80uA) 0111:2.24k(80uA) 1000:1.6k(160uA) 1001:1.12k(160uA) 1010:800(320uA) 1011:560(320uA) 1100:400(640uA)	

			1101:280(640uA) 1110:200(1280uA) 1111:140(1280uA)	

ERRSEL：Error Detect Select Register(Address 0EH)

Bit	Symbol	R/W	Description	Default
7	OC_CLAMP	R/W	LDOUT,XEMOUT output control at the time of the Over Current detection 0: LDOFF and output an error to XEMOUT and register OC_EM when detect over current 1: Do not LDOFF and do not output an error to XEMOUT either, but register OC_EM when detect over current Clamp an output current by over threshold current Output an error flag in register OC_EM	0x00
6:5	APC2_ERR_SEL	R/W	Selection of the APC2 error threshold Compare PDTGTIN[9:0] with the ADC result of the PD voltage that drove a laser in IBAIS + ISW which decided in APC1,2 00: Error with errors more than ±64dec (6.25% of PD AD full scales) 01: Error with errors more than ±128dec (12.5% of PD AD full scales) 10: Error with errors more than ±256dec (25% of PD AD full scales) 11: Error detection function OFF	
4	APC1_ERR_SEL	R/W	Selection of APC1 error and judgment standard 0: Calculated Ith is smaller than 0; or when PD ADC result at the time of APC1 are more than PD_BG[9:0] + 64dec with IBIAS laser driver current 1: Error detection function OFF	
3	APC_ERR_MODE	R/W	Selection of the process method when detected the APC1,APC2 error 0: Off at LDOUT and low at XEMOUT terminal 1: LDOUT with IBIAS_FIX[7:0] and ISW_FIX[7:0] current condition high at XEMOUT and error flag in register	
2:0	OC_SEL	R/W	Selection of the over current threshold 000: 3.7A (default) 001: 3.1A 010: 2.6A 011: 2.1A 100: 1.7A 101: 1.3A	

			110: 0.8A 111: Error detection function OFF	

TRAS (Address 0FH)

Bit	Symbol	R/W	Description	Default
7:6	-	R/W	Reserved	0x0C
5:4	DIF_ERR_SEL	R/W	Selection of the diffuser threshold Compare PD_BG[9:0] with the PD ADC result when emit light in (IBIAS + ISW) decided in APC1,APC2 00: Error in less than PD_BG[9:0] + 128dec (default) 01: Error in less than PD_BG[9:0] + 64dec 10: Error in less than PD_BG[9:0] + 32dec 11: Error detection function OFF	
3:0	DRV_AS	R/W	Selection of the Tr wave assist quantity 0000: Assist weak …… 1100 (default) …… 1111: Assist strong	

ASIW (Address 10H)

Bit	Symbol	R/W	Description	Default
7:4	DRV_SAG	R/W	Division ratio setting of the wave sag adjustment level 0000: Sag adjustment weak …… 0100 (default) …… 1111: Sag adjustment strong	0x46
3:0	DRV_AS_W	R/W	Revision width setting of the wave assist current 0000: 0.36 ns …… 0110 (default) …… 1111: 2.16ns	

LVDSCTR: LVDS Control Register (Address 12H)

Bit	Symbol	R/W	Description	Default
7:3	-	R/W	Reserved	0x00
2	DRVLVDS	R/W	Digital control part of LVDS 0 : Disable LVDS signal (default)	

			1 : Enable LVDS signal	
1	-	R/W	Reserved	
0	DISLVDS_PED	R/W	Control of the LVDS PED enable 0: Enable (default) 1: Disable	

ADCMODE: ADC Mode Register (Address 13H)

Bit	Symbol	R/W	Description	Default
7:6	-	R/W	Reserved	0x01
5:4	ADC_START	R/W	Control of the ADC start signal for temperature detection 00:ADC start in High of the APC_GATE signal for APC 01: Don't use 10: ADC start for internal temperature sensor or AUX_ADC(invalid during movement of the PD ADC) ※automatically goes back up to 00 after ADC 11: ADC start in High of the APC_GATE signal for APC	
3	-	R/W	Reserved	
2	ADSEL	R/W	Input selection of ADC connection for temperature detection 0: Internal temperature sensor 1: AUX_ADC terminal signal voltage (outside thermistor use)	
1:0	ADEN	R/W	OSC circuit control for ADC clock 00: All time disable 01: OSC enable only at the APC_GATE high condition 10: OSC enable only at the APC_GATE high condition 11: All time enable	

ADALARM: AD Alarm Register (Address 14H)

Bit	Symbol	R/W	Description	Default
7	TEMP_ADC_ALARM	R	The alarm signal to indicate the AD conversion average of TEMP process 0: AD conversion completion 1: During AD conversion, and data is invalid	0x00
6	APC_ALARM	R	The alarm signal to indicate the AD conversion average of APC process 0: AD conversion completion 1: During AD conversion, and shield Temperature monitor AD and AD for initial Power adjustment at the time of 1	
5:2	-	R	Reserved	

1:0	TEMP_DATA[9:8]	R	AD DATA for temperature monitors, Higher 2Bit	

TMPDATA_L: AD Data of Temperature Register (Address 15H)

Bit	Symbol	R/W	Description	Default
7:0	TEMP_DATA[7:0]	R	AD DATA for temperature monitors, Lower 8bit	0x00

IBSCALC: Ibias Calculated Value Register (Address 18H)

Bit	Symbol	R/W	Description	Default
7:0	IBIAS_CALC	R	Ibias value which was calculated in APC1	0x00

ISWCALC: Isw Calculated Value Register (Address 19H)

Bit	Symbol	R/W	Description	Default
7:0	ISW_CALC	R	Isw value which was calculated in APC2	0x00

PDBGLH1_H: High 2bit of PD_ADC Result Register (Address 1AH)

Bit	Symbol	R/W	Description	Default
7:6	PD_L2[9:8]	R	PD_ADC output value in APC_L2, Higher 2Bit	0x00
5:4	PD_H1[9:8]	R	PD_ADC output value in APC_H1, Higher 2Bit	
3:2	PD_L1[9:8]	R	PD_ADC output value in APC_L1, Higher 2bit	
1:0	PD_BG[9:8]	R	PD_ADC output value in the APC_BG, Higher 2bit	

PDCHK_H: High 2bit of PD_ADC Result Register (Address 1BH)

Bit	Symbol	R/W	Description	Default
7:6	-	R	Reserved	0x00
5:4	APC2_CHECK_DATA[9:8]	R	PD_ADC output value at the time of the APC2 error check Higher 2Bit	
3:2	APC1_CHECK_DATA[9:8]	R	PD_ADC output value at the time of the APC1 error check Higher 2bit	
1:0	PD_H2[9:8]	R	PD_ADC output value in APC_H2, Higher 2bit	

PDBG_L: PD_BG Result of lower 8bit Register (Address 1CH)

Bit	Symbol	R/W	Description	Default
7:0	PD_BG	R	PD_ADC output value in the APC_BG, Lower 8bit	0x00

PDL1_L: PD_ADC Result Register (Address 1DH)

Bit	Symbol	R/W	Description	Default
7:0	PD_L1	R	PD_ADC output value in APC_L1, Lower 8bit	0x00

PDH1_L: PD_ADC Result Register (Address 1EH)

Bit	Symbol	R/W	Description	Default
7:0	PD_H1	R	PD_ADC output value in APC_H1, Lower 8bit	0x00

PDL2_L: PD_ADC Result Register (Address 1FH)

Bit	Symbol	R/W	Description	Default
7:0	PD_L2	R	PD_ADC output value in APC_L2, Lower 8bit	0x00

PDH2_L: PD_ADC Result Register (Address 20H)

Bit	Symbol	R/W	Description	Default
7:0	PD_H2	R	PD_ADC output value in APC_H2, Lower 8bit	0x00

APC1CHK_L: PD_ADC Result Register (Address 21H)

Bit	Symbol	R/W	Description	Default
7:0	APC1_CHECK_DATA	R	PD_ADC output value at the time of the APC1 error check Lower 8bit	0x00

APC2CHK_L: PD_ADC Result Register (Address 22H)

Bit	Symbol	R/W	Description	Default
7:0	APC2_CHECK_DATA	R	PD_ADC output value at the time of the APC2 error check Lower 8bit	0x00

SA_EM: Error Flag Register (Address 23H)

Bit	Symbol	R/W	Description	Default
7	APC2_EM	R	APC2 error flag 0: Normal 1: APC2 error (Except reset dummy write to this address can clear this error result)	0x00
6	APC1_EM	R	APC1 error monitor	

			0: Normal 1: APC1 error (Except reset dummy write to this address can clear this error result)	
5	VCC_EM	R	Power supply monitoring error flag 0: Normal 1: Power supply error (Except reset dummy write to this address can clear this error result)	
4	DIF_EM	R	Diffuser issue detection 0: Normal 1: Diffusion error (Except reset dummy write to this address can clear this error result)	
3	OC_EM	R	Over current error flag 0: Normal 1: Over current (Except reset dummy write to this address can clear this error result)	
2	-	R	Reserved	
1	LVDS_EM	R	LVDS error flag 0: Normal 1: LVDS error (Except reset dummy write to this address can clear this error result)	
0	-	R	Reserved	

VER: Mixed Function Register (Address 24H)

Bit	Symbol	R/W	Description	Default
7:3	-	R	Reserved	0x00
2:0	VERSION	R	CHIP VERSION	

GLRST: Global Reset Register(Address 25H)

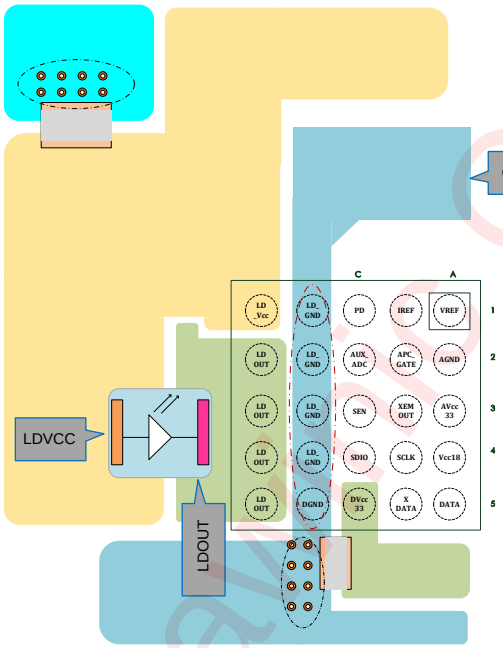
Bit	Symbol	R/W	Description	Default
7:0	GL_RST	W	At the time of RSTDIS = 0, writing 8'h01 to reset the data of the registers; At the time of RSTDIS = 1, not reset	0x00

PCB Layout Consideration

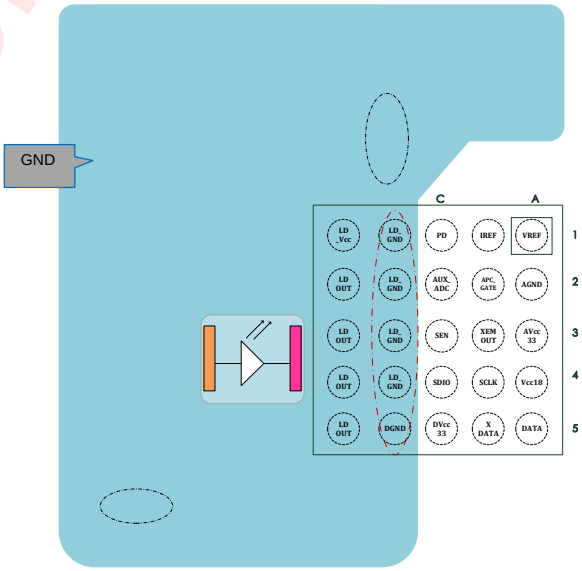
AW36801 is a highly-integrated VCSEL laser diode driver, PCB layout should be considered carefully. Here are some guidelines:

1. The capacitors of all power pins are placed close to the corresponding pins of the chip. The capacitance of VREF pins and the resistance of IREF pins should be placed as close to their respective pins as possible.
2. The VCSEL needs to be placed close to the LDOUT of the chip to reduce the route length from LDVCC to LDOUT and the route length is as wide as possible.
3. The current path from LDVCC-VCSEL-LDOUT-LDGND-LDVCC should be as small as possible. Using thin interlayer plates is batter.
4. The Via connected to GND should be placed as far as possible at the edges of the two nodes to reduce impedance.
5. LVDS input pins need to be equidistant wiring and impedance matching. Place 100Ω resistor as close as possible to the DATA and XDATA pin.
6. Try to keep the integrity of the ground plane of layer 2, and do not divide the GND of layer2.
7. Inductance less than 1nH.

Layer 1



Layer 2

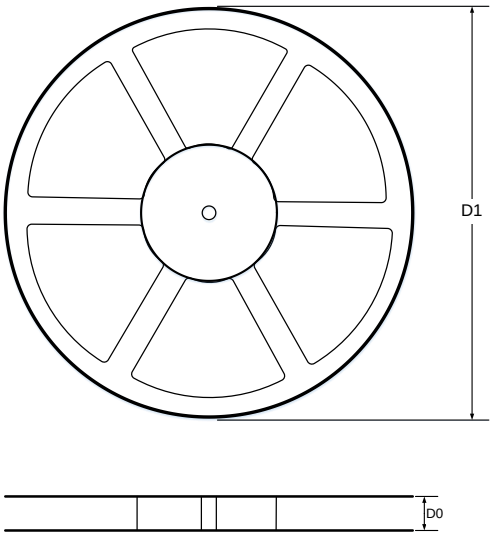


Use the Low ESL Capacitor

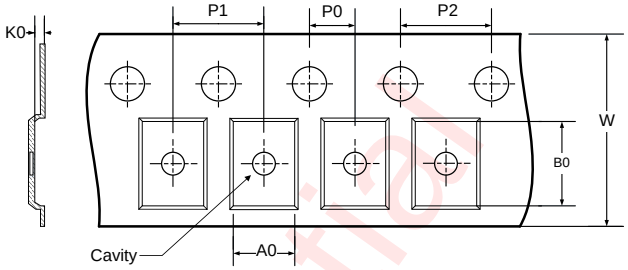
Place many via around the circle area to reduce connection impedance of GND between layer1 and layer2.

Tape And Reel Information

REEL DIMENSIONS

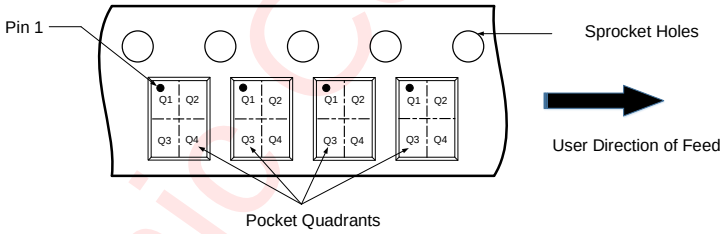


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

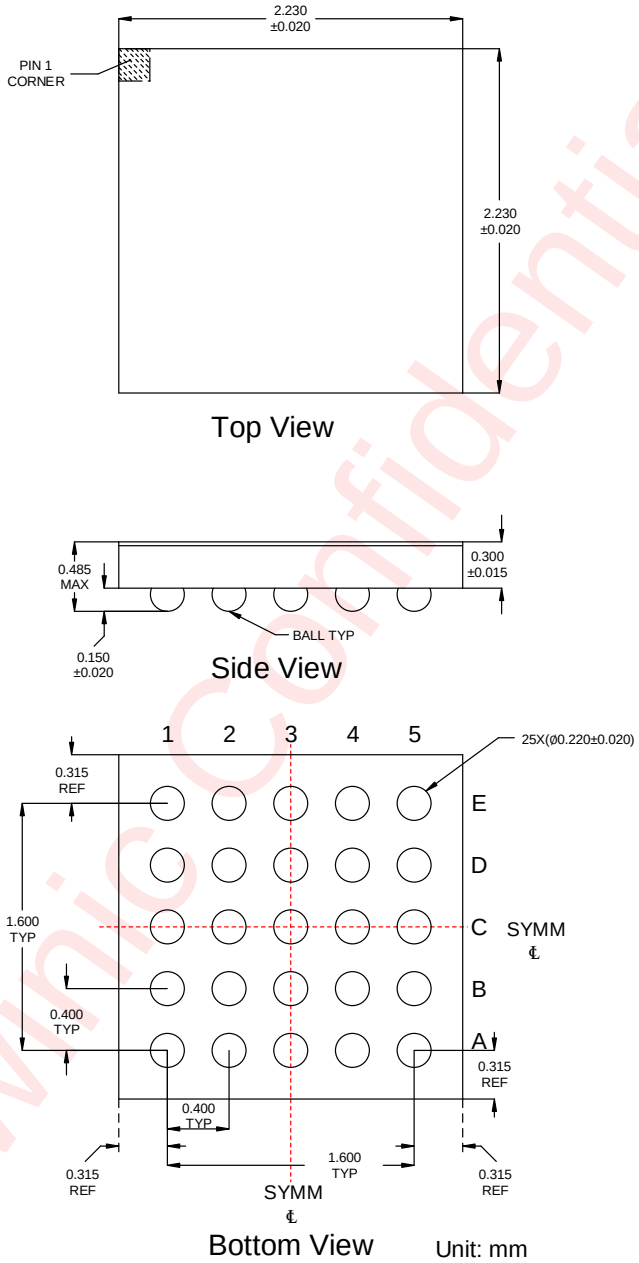
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



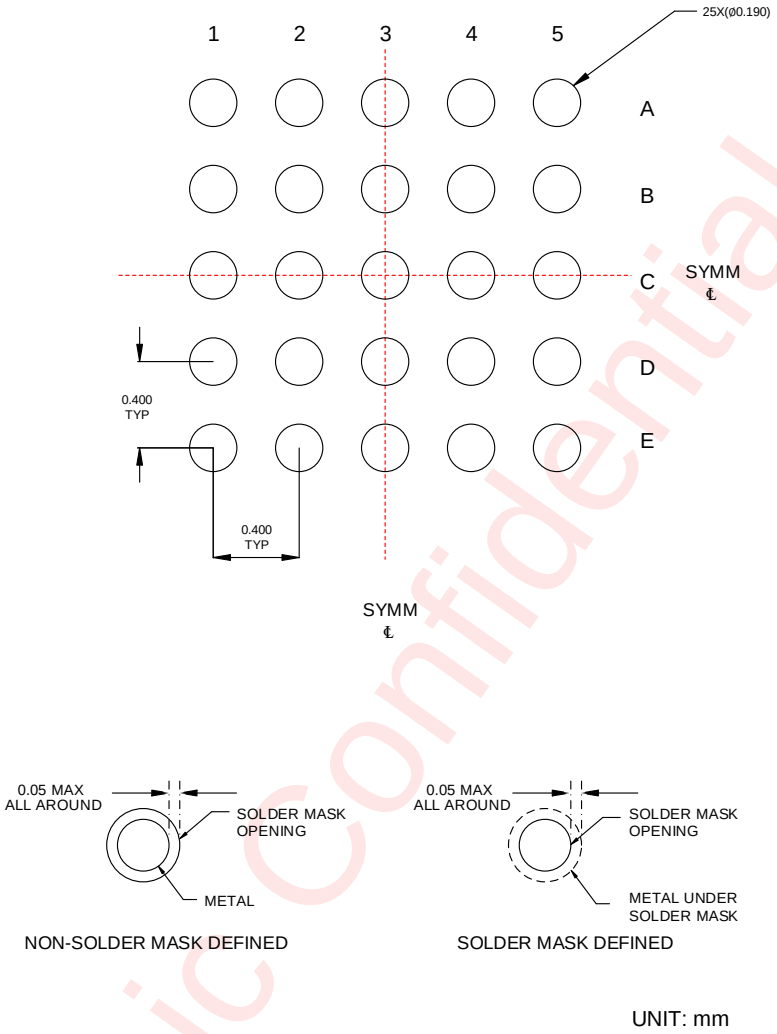
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	2.42	2.42	0.65	2.00	4.00	4.00	8.00	Q1

Package Description



Land Pattern Data



UNIT: mm

Revision History

Version	Date	Change Record
V1.0	2020.10	Preliminary Released
V1.1	2021.07	Correct the description error
V1.2	2023.08	1. Correct the test method of HBM and CDM.(P6) 2. Add the Allowed power dissipation and Thermal Information.(P6-P7) 3. Update the Recommended Operating Conditions and Electrical Characteristics.(P6-P8)
V1.3	2023.10	Add the figure of LVDS differential input.(P9)

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