SY5881Z

DC/DC Buck Controller For LED Dimming Lighting

General Description

The SY5881Z is a DC/DC Buck controller targeting at LED lighting applications with analog dimming. It adopts the proprietary control architecture to achieve an accurate regulation of LED current and Quasi-Resonant valley turn-on high efficiency operation.

The SY5881Z supports analog dimming function and it has a linear dimming curve.

It integrates open/short LED protection and eliminates the auxiliary winding with floating topology, thus minimizing the component count and board size.

Features

- Linear Dimming Curve.
- Dimming Range from 2.5% to 100.0%.
- CV Mode for Bias Supply when PWM=0%
- Valley Turn-on to Achieve Low Switching Losses
- Single Winding Inductor with Floating Topology
- 200mA Sourcing Current and 600mA Sinking Current Drive Capability
- Low Start up Current: 34μA typical
- Reliable Short LED and Open LED Protection
- Reliable Short ISEN Resistor Protection
- Compact Package: SO8

Ordering Information

SY5881 □(□□)□

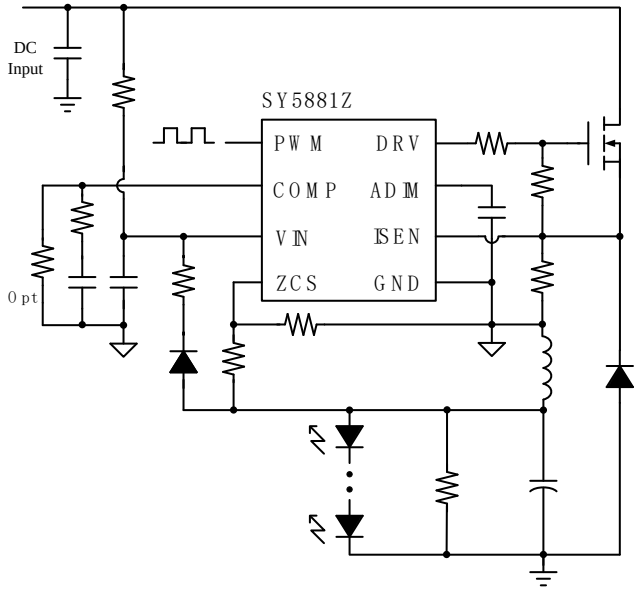
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5881ZFAC	SO8	----

Applications

- LED Lighting

Typical Applications



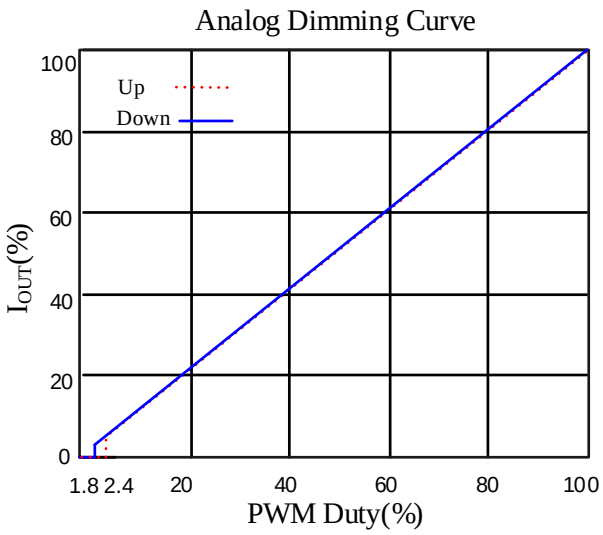
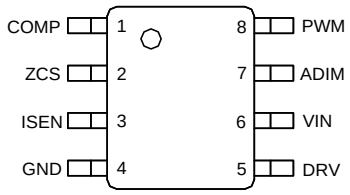


Figure.1 Schematic Diagram

Pinout (top view)



（SO8）

Top Mark: CGG*xyz* (device code: CGG, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
COMP	1	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
ZCS	2	Inductor current zero-crossing detection pin. This pin receives the output voltage by a resister divider and detects the inductor current zero crossing point. This pin also provides over voltage protection. If the voltage on this pin is above $V_{ZCS,OVP}$, the IC would enter over voltage protection mode.
ISEN	3	Current sense pin. Connect this pin to the source of the MOSFET. Connect the sense resistor across the source of the MOSFET and the GND pin. (current sense resister R_S: $R_S = \frac{V_{REF}}{I_{OUT}}$)
GND	4	Ground pin
DRV	5	Gate driver pin. Connect this pin to the gate of the MOSFET.
VIN	6	Power supply pin. This pin also provides output over voltage protection along with ZCS pin.
ADIM	7	Bypass this pin to GND with enough capacitance to hold on internal voltage reference. 2.2uF cap is recommended.
PWM	8	PWM dimming input pin, this pin detects the PWM dimming signal

Absolute Maximum Ratings (Note 1)

VIN, DRV ---------- -0.3V~25V
Supply current I_{VIN} ---------- 7mA
PWM ---------- -0.3V~23V
ZCS, ADIM ---------- -0.3V~1.8V
ISEN, COMP ---------- -0.3~ 3.6V
Power Dissipation, @ T_A = 25°C SO8 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} ---------- 88°C/W
SO8, θ_{JC} ---------- 45°C/W
Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV ---------- 8.5V~20V

Block Diagram

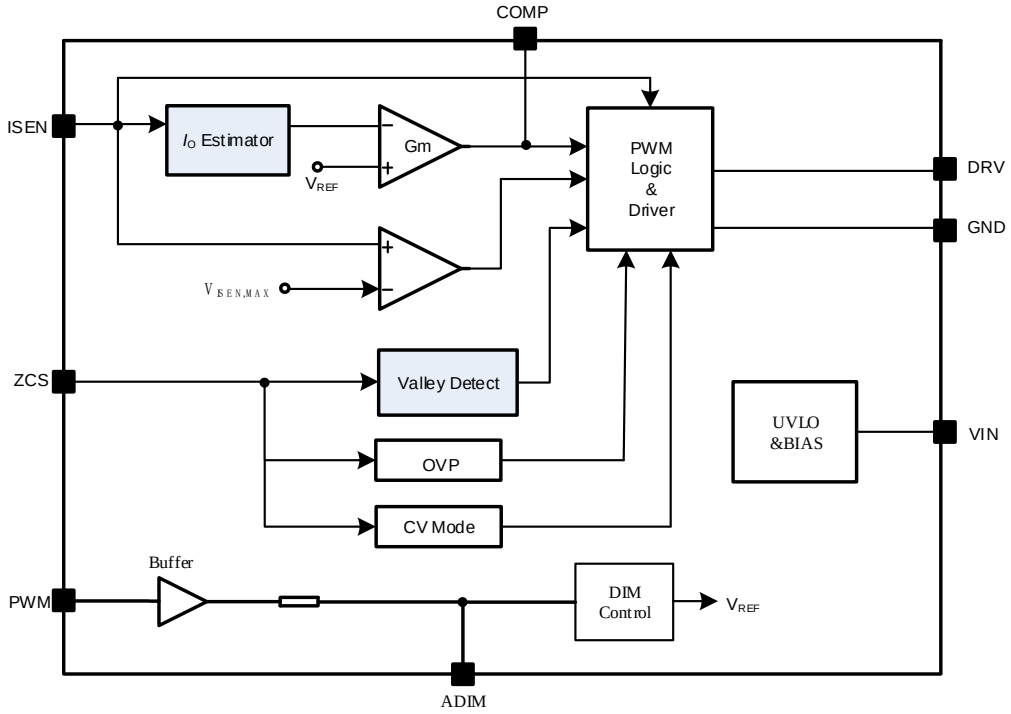


Figure.3 Block Diagram

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}		12.5	14.0	15.5	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.7	7.3	8.0	V
VIN OVP Voltage	V_{VIN_OVP}			24		V
Start up Current	I_{ST}	V_{VIN}<V_{VIN_ON}	24	34	46	μA
Discharge Current in OVP Mode	I_{VIN_OVP}	V_{VIN}=15V(Note 4)	5	7	10	mA
Error Amplifier Section						
Internal Reference Voltage	V_{REF}		245	250	255	mV
Current Sense Section						
Current Limit Reference Voltage	V_{ISEN_MAX}		0.53	0.6	0.67	V
ZCS Pin Section						
ZCS Pin OVP Voltage Threshold	V_{ZCS_OVP}		1.43	1.50	1.57	V
Gate Driver Section						
Gate Driver Voltage	V_{Gate}		9.5	12.0	14.5	V
Maximum Source Current	I_{SOURCE}		150	200	250	mA
Minimum Sink Current	I_{SINK}		500	600	800	mA
Max ON Time	T_{ON_MAX}	V_{COMP}=2.6V		20		μs
Min ON Time	T_{ON_MIN}			350		ns
Max OFF Time	T_{OFF_MAX}			52		μs
Min OFF Time	T_{OFF_MIN}			0.5		μs
Maximum Switching Frequency	F_{MAX}			200		kHz
ADIM function Section						
ADIM Enable ON	V_{ADIM_ON}		31	42	53	mV
ADIM Enable OFF	V_{ADIM_OFF}		24	35	46	mV
Thermal Section						
Thermal Fold back Temperature	T_{FB}			150		°C
Thermal Shut down Temperature	T_{SD}			160		°C
PWM Function Section						
PWM ON voltage	V_{PWM_ON}				1.2	V
PWM OFF voltage	V_{PWM_OFF}		0.5			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.
Note 4: Increase VIN pin voltage gradually higher than VVIN,OVP voltage then turn down to 15V.

Operation

The SY5881Z is a DC/DC Buck controller targeting at LED lighting applications with analog dimming function.

It eliminates the auxiliary winding with floating topology, thus minimizing the component count and board size.

The SY5881Z supports analog dimming function and it has a linear dimming curve.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley.

the startup current of SY5881Z is rather small (34 μ A typically) to reduce the standby power loss further.

SY5881Z provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), etc.

SY5881Z is available with SO8 package.

Applications Information

Start up

After DC BUS is powered on, the capacitor C_{VIN} between VIN and GND pin is charged up by BUS voltage through a start-up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of transformer could supply enough energy to maintain V_{VIN} above V_{VIN_OFF}.

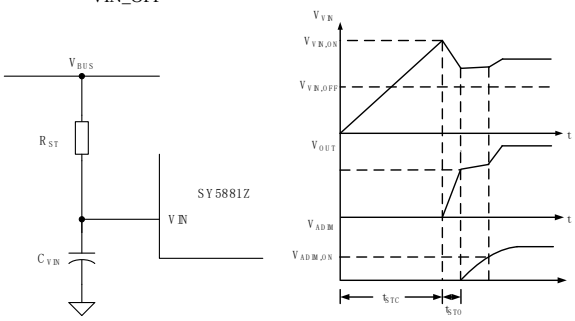


Fig.4 Start up

The whole start up procedure is divided into four sections shown in Fig.4. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage build-up section. The start-up time t_{ST} is composed of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

t_{STO} is fast start-up stage, which will help to create output voltage quickly. After t_{STO}, if V_{ADIM} is less than V_{ADIM_ON}, IC enters into CV mode. When V_{ADIM} is larger than V_{ADIM_ON}, IC works in peak current mode.

The start-up resistor R_{ST} and C_{VIN} are designed by rules as below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than 1mA.

$$\frac{V_{BUS}}{1mA} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step **(a)** and redo such design flow until the ideal start up procedure is obtained.

Internal pre-charge design for quick start up

In P3, V_{COMP} is pre-charged by internal current source until it is over the initial voltage V_{COMP_IC}. V_{COMP_IC} can be programmed by R_{COMP}. Such design is meant to reduce the start-up time shown in Fig.5.

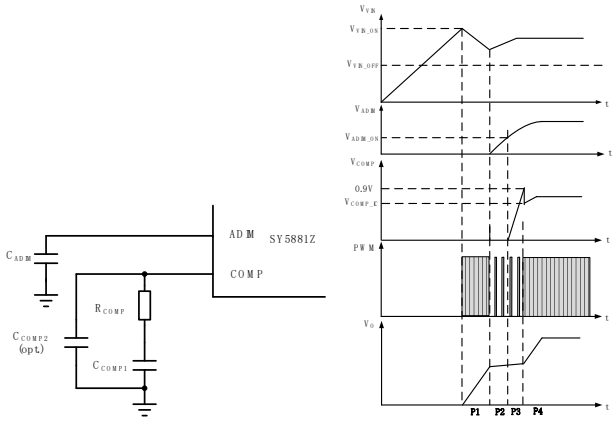


Fig.5 Pre-charge scheme in start up

The voltage pre-charged V_{COMP_IC} in start-up procedure can be programmed by R_{COMP}:

$$V_{COMP\_IC} = 0.9V - 300\mu A \times R_{COMP} \quad (3)$$

Where V_{COMP_IC} is the pre-charged voltage of COMP pin.

Generally, a small capacitance of C_{COMP} is necessary to stabilize the system loop (10nF is recommended).

The voltage pre-charged in start-up procedure can be programmed by R_{COMP}; On the other hand, larger R_{COMP} can provide larger phase margin for the control loop; A small ceramic capacitor is added to suppress high frequency interruption (10pF~100pF is recommended if necessary)

Shut down

After DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the power supply for IC is not enough, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working and V_{COMP} will be discharged to zero.

Constant-current control

The switching waveforms are shown in Fig.6.

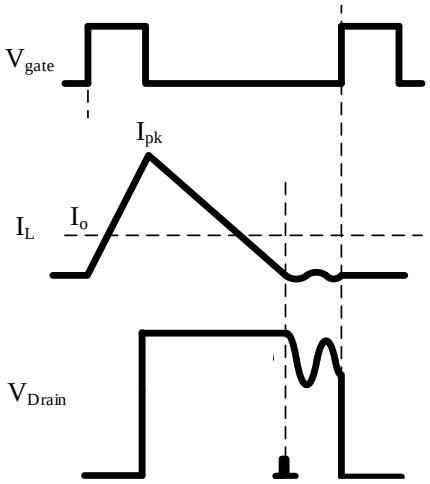


Fig.6 Switching waveforms

The average current of the inductor can be detected by ISEN pin of the IC directly, which is applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.as shown in Fig.7.

$$V_{REF}=I_{OUT}\times R_S \quad (4)$$

Finally, the output current I_{OUT} can be represented by

$$I_{OUT}=\frac{V_{REF}}{R_S} \quad (5)$$

Where V_{REF} is the internal reference voltage; R_S is the current sense resistor.

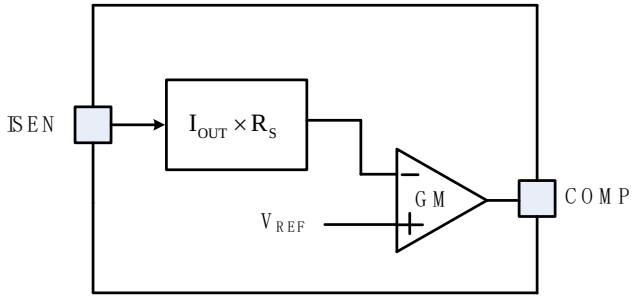


Fig.7 Output current detection diagram

V_{REF} is internal constant parameters, the R_S resistance can be expressed as follows, when the output current is known.

$$R_S=\frac{V_{REF}}{I_{OUT}} \quad (6)$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for the converter. The voltage across drain and source of the MOSFET is reflected by a resistor divider across Inductor. ZCS pin detects the voltage via this resistor divider. When the voltage across drain and source of the MOSFET is at voltage valley, the MOSFET would be turned on.

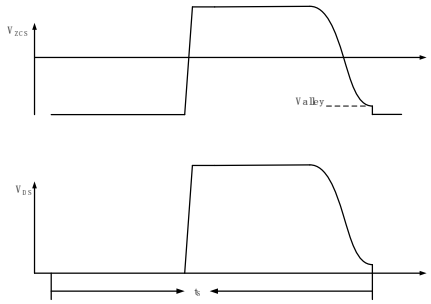


Fig.8 QR mode operation

CV Mode

When PWM near to zero, IC and MCU still need bias power, so:

(1) If Dimming signal is greater than 2.4%, IC always works at CC mode.

(2) If Dimming signal is lower than 1.8%, CV mode is triggered. IC works in CV mode to maintain V_{FB} nearby

V_{ZCS_CV}. R_{ZCS} could be adjusted to prevent LED flicker and bias supply enough.

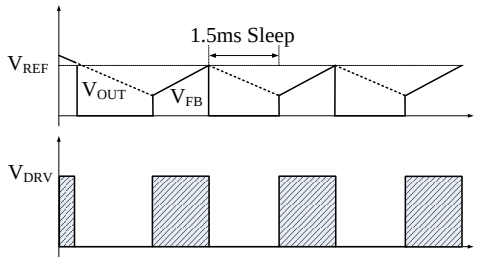


Figure.9 The working process of CV mode

In CV mode,

If V_{FB} is smaller than V_{ZCS_CV}, MOSFET turned off when ISEN voltage reach $V_{CV\_ISEN\_MAX}$ in every switching cycle, and turned on by QR.

If V_{FB} is greater than V_{ZCS_CV}, IC will sleep for 1.5ms, until V_{FB} is smaller than V_{ZCS_CV}.

The output of CV is decided by OVP.

$$V_{OUT\_CV} = \frac{V_{OUT,OVP}}{3} \quad (6)$$

Over Voltage Protection (OVP) & Open LED Protection (OLP)

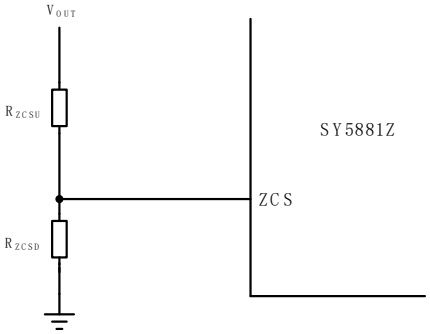


Fig.10 OVP&OLP

The output voltage is reflected by the Buck inductor, and both ZCS pin and VIN pin provide over voltage protection function.

When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{VIN} exceeds V_{VIN_OVP} or V_{ZCS} exceeds V_{ZCS_OVP}, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_OVP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the resistor divider is related with the OVP function.

$$\frac{V_{ZCS\_OVP}}{V_{OVP}} = \frac{R_{ZCSD}}{R_{ZCSU}+R_{ZCSD}} \quad (8)$$

Where V_{OVP} is the output over voltage specification; R_{ZCSU} and R_{ZCSD} compose the resistor divider. The ratio of R_{ZCSU} to R_{ZCSD} could be induced from equation (8).

Short Circuit Protection (SCP)

When the output is shorted, the output voltage is clamped to zero. Valley signal cannot be detected by ZCS. Without valley detection, MOSFET cannot be turned ON until maximum off time t_{OFF_MAX} is matched. If MOSFET is turned ON by t_{OFF_MAX} 64 times continuously, IC will be shut down and enter into hiccup mode.

If the output voltage is not low enough to disable valley detection in short condition, V_{VIN} will drop down without power supply. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by the BUS voltage through the start-up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Dimming Mode

SY5881Z supports analog dimming. The dimming signal is given as PWM square waveform and the output current is up to the duty cycle of the dimming signal.

Analog Dimming Mode

In Analog dimming mode, SY5881Z is compatible with PWM dimming signal, the output current is regulated by the voltage on ADIM pin.

If the dimming signal is PWM signal, it is given to PWM pin. When the voltage of PWM pin is higher than V_{PWM_ON}, the dimming signal is sensed as high logic level, and ADIM pin is pulled up to 1.75V by a 10kΩ resistor; when the voltage is lower than V_{PWM_OFF}, the dimming signal is sensed as low logic level, and ADIM pin is pulled down to GND by a 10kΩ resistor. The duty cycle of the dimming signal D_{DIM} is reflected by the voltage on ADIM pin V_{ADIM}.

$$V_{ADIM} = D_{DIM} \times 1.75V \quad (9)$$

When V_{ADIM} is lower than V_{ADIM_OFF} (D_{DIM} is 1.8%), the output current is zero; When V_{ADIM} is from V_{ADIM_OFF} to V_{ADIM_ON} (D_{DIM} is about from 1.8% to 2.4%), the output current is zero;

When V_{ADIM} is higher than V_{ADIM_ON}, the output current is 3.1% of rated output current. When V_{ADIM} is higher than 1.75V, the output current is 100% of rated output current;

When V_{ADIM} is in the range from 1.75V to 32mV (D_{DIM} is from 100% to 1.8%), I_{OUT} reduces with PWM linearly from 100% to 2.5% of rated output current.

The dimming curve between output current I_{OUT} and duty cycle of dimming signal is shown as below.

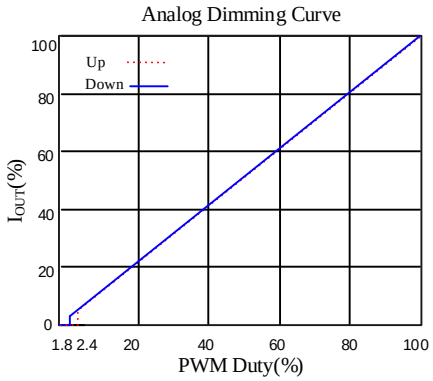


Fig.11 Dimming cure of analog dimming

1% dimming depth

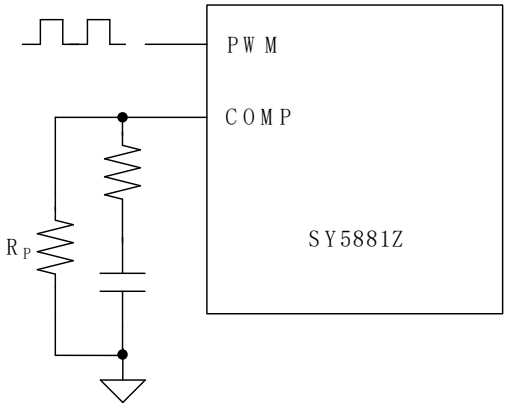


Fig.12 1% Dimming depth circuit

For further dimming depth, R_P is added to achieve it and 2M is recommended.

ADIM capacitor

A capacitor C_{ADIM} need be connected across ADIM pin and GND pin to obtain a smooth voltage waveform of the dimming signal duty cycle. C_{ADIM} is selected by

$$C_{ADIM} \geq \frac{10^{-3}}{f_{DIM}} \ F \cdot Hz \quad (10)$$

Where f_{DIM} is the frequency of PWM dimming signal.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and output power diode is maximized;

$$V_{MOS\_DS\_MAX} = V_{BUS\_MAX} \quad (11)$$

$$V_{D\_R\_MAX} = V_{BUS\_MAX} \quad (12)$$

Where V_{BUS_MAX} is the maximum input DC voltage.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

Inductor (L)

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.13.

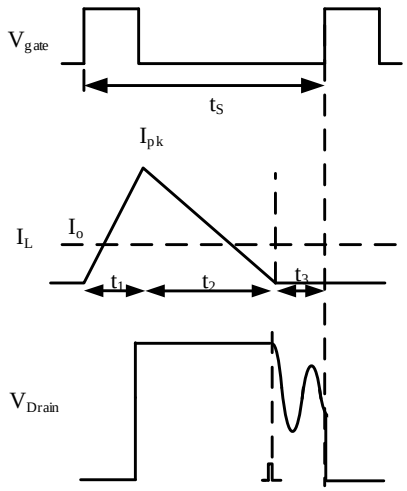


Fig.13 switching waveforms

The system operates in peak current mode. The ON time increases with the input DC voltage decreasing and the load increasing. When the operation condition is with minimum input DC voltage and full load, the ON time is maximized. Thus, the minimum switching frequency f_{S_MIN} happens at minimum input voltage and maximum load condition; Meanwhile, the maximum RMS current through MOSFET happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be calculated. The design flow is shown as below:

(a) Preset minimum frequency f_{S_MIN}

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}} \quad (13)$$

$$t_1 = \frac{t_S \times (V_{OUT} + V_{DF})}{(V_{BUS,MIN} + V_{DF})} \quad (14)$$

$$t_2 = t_S - t_1 \quad (15)$$

Where V_{DF} is the forward voltage of the diode

(c) Design inductance L

$$L = \frac{(V_{BUS,MIN} - V_{OUT}) \times t_1 \times \eta}{2 \times I_{OUT}} \quad (16)$$

Where η is the efficiency; P_{OUT} is rated full load power;

(d) Compute inductor maximum peak current $I_{L\_PK\_MAX}$.

$$I_{L\_PK\_MAX} = \frac{(V_{BUS,MIN} - V_{OUT}) \times t_1}{L} \quad (17)$$

Where $I_{L\_PK\_MAX}$ is the maximum inductor peak current;

(e) Compute the RMS current of Buck inductor

$I_{L\_RMS\_MAX}$ is inductor RMS current

$$I_{L\_RMS\_MAX} = \frac{1}{\sqrt{3}} \times I_{L,PK,MAX} \quad (18)$$

(f) Compute RMS current of the MOSFET

$$I_{MOS\_RMS\_MAX} = \sqrt{\frac{t_1}{3t_S}} \times I_{L,PK,MAX} \quad (19)$$

Inductor design (N)

These parameters below are necessary:

Necessary parameters	
Inductance	L
inductor maximum current	$I_{L\_PK\_MAX}$
inductor maximum RMS current	$I_{L\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.3~0.33T

(c) Compute the primary turns N

$$N = \frac{L_M}{\Delta B \times A_e} \times \frac{V_{ISEN,MAX}}{R_{ISEN}} \quad (20)$$

(d) Select an appropriate wire diameter

With $I_{L\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(e) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Output current ripple ΔI_O is,

$$\Delta I_O = \sqrt{\frac{I_{L,PK,MAX}^2}{3} - I_O^2} \quad (21)$$

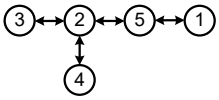
Choose proper output capacitance to satisfy current ripple.

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the input should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small.

(c) The connection of ground is recommended as:



Ground ①: ground node of current sample resistor
Ground ②: ground of GND pin
Ground ③: ground of ADIM capacitor
Ground ④: ground of signal trace except GND pin
Ground ⑤: ground of bias supply capacitor

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of ‘Source of MOSFET – current sample resistor – GND pin’ should be kept as small as possible.

(f) The resistor divider connected to ZCS pin is recommended to be put beside the IC.

(g) The control circuit is recommended to be put outside the power circuit loop.

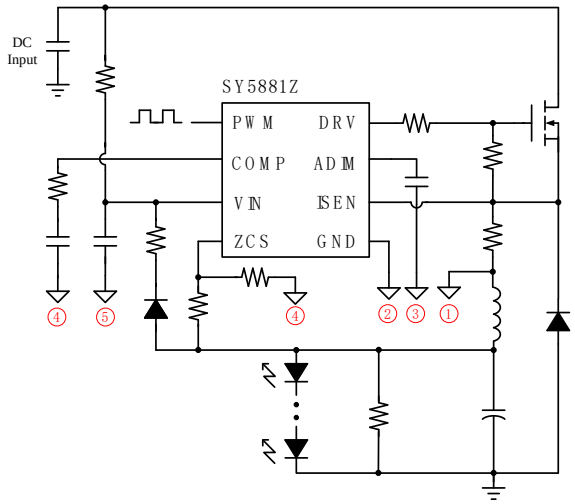


Fig.14 Ground connection recommended

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{BUS}	380~420V	V_{OUT}	150V
I_{OUT}	300mA	η	96%

#2.Inductor design (L)

Refer to Power Device Design

Conditions			
$V_{BUS,MIN}$	380V	$V_{BUS,MAX}$	420V
P_{OUT}	45W	$F_{S,MIN}$	50kHz

(a) $F_{S,MIN}$ is preset

$$F_{S,MIN} = 50KHz$$

(**b**) Compute the switching period t_S and ON time t_1.

$$t_S = \frac{1}{F_{S,MIN}} = 20.00\mu s$$

$$t_1 = \frac{t_S \times (V_{OUT} + V_{DF})}{(V_{BUS,MIN} + V_{DF})} = \frac{20.00us \times (150V + 1V)}{(380V + 1V)} = 7.92\mu s$$

$$t_2 = t_S - t_1 = 20.00\mu s - 7.92\mu s = 12.08\mu s$$

(c) Compute the inductance L

$$L = \frac{(V_{BUS,MIN} - V_{OUT}) \times t_1 \times \eta}{2 \times I_{OUT}} = \frac{(380V - 150V) \times 7.92us \times 0.96}{2 \times 0.3A} = 2914.56\mu H$$

Choose L=3000uH;

(d) Compute inductor maximum peak current $I_{L\text{-}PK\text{-}MAX}$.

$$I_{L\_PK\_MAX} = \frac{(V_{BUS,MIN} - V_{OUT}) \times t_1}{L} = \frac{(380V - 150V) \times 7.92us}{3000uH} = 0.6072A$$

Where $I_{L\_PK\_MAX}$ is the maximum inductor peak current;

(e) Compute RMS of the inductor current $I_{L\_RMS\_MAX}$

$$I_{L\_RMS\_MAX} = \frac{1}{\sqrt{3}} \times I_{L,PK,MAX} = \frac{1}{\sqrt{3}} \times 0.6072A = 0.35A$$

#3. Select power MOSFET and power diode

Refer to Power Device Design

Known conditions at this step			
$V_{BUS,MAX}$	420V	η	96%
V_{OUT}	150V		

Compute the voltage and the current stress of MOSFET:

$$I_{MOS\_RMS\_MAX} = \sqrt{\frac{t_1}{3t_S}} \times I_{L,PK,MAX} = \sqrt{\frac{7.92us}{3\times 20us}} \times 0.6072A = 0.22A$$

#4. Set VIN pin

Refer to Start up

Conditions			
V_{BUS_MIN}	380V	V_{BUS_MAX}	420V
I_{ST}	34μA (typical)	V_{IN_ON}	14.5V (typical)
		t_{ST}	500ms (designed by user)

(a) R_{ST} is preset

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} = \frac{380V}{34\mu A} = 11.17M\Omega$$

$$R_{ST} > \frac{V_{BUS,MAX}}{1mA} = \frac{420V}{1mA} = 420k\Omega$$

Set R_{ST}

$R_{ST} = 510k\Omega \times 2 = 1020k\Omega$

(b) Design C_{VIN}

$$C_{VIN} = \frac{(\frac{V_{BUS,MIN}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

$$= \frac{(\frac{380V}{1020k\Omega} - 34\mu A) \times 500ms}{14.5V}$$

$$= 11.67\mu F$$

Set C_{VIN}

$C_{VIN} = 10\mu F$

#5 Set COMP pin

Refer to **Internal pre-charge design for quick start up**

Parameters designed			
R_{COMP}	1.0kΩ	V_{COMP_IC}	900mV
C_{COMP1}	10nF	C_{COMP2}	0

#6 Set current sense resistor to achieve ideal output current

Refer to **Constant-current control**

Known conditions at this step			
V_{REF}	0.25V	I_{OUT}	0.3A

The current sense resistor is

$$R_S = \frac{V_{REF}}{I_{OUT}} = \frac{0.25}{0.3A} = 0.833\Omega$$

#7 set ZCS pin

Refer to **Over Voltage Protection (OVP) & Open Loop Protection (OLP)**

First, Set R_{ZCSD}=10KΩ.

Then compute R_{ZCSD}

Conditions			
V_{ZCS_OVP}	1.50V	V_{OVP}	180V
V_{OUT}	150V		
Parameters designed			
R_{ZCSD}	10kΩ		

$$R_{ZCSU} = \frac{(V_{OVP} - V_{ZCS\_OVP}) \times R_{ZCSD}}{V_{ZCS\_OVP}} = \frac{(180V - 1.5) \times 10K}{1.5} = 1190K$$

R_{ZCSU} is set to

R_{ZCSU}=620kΩ×2=1240kΩ

#8 set ADIM and PWM pin

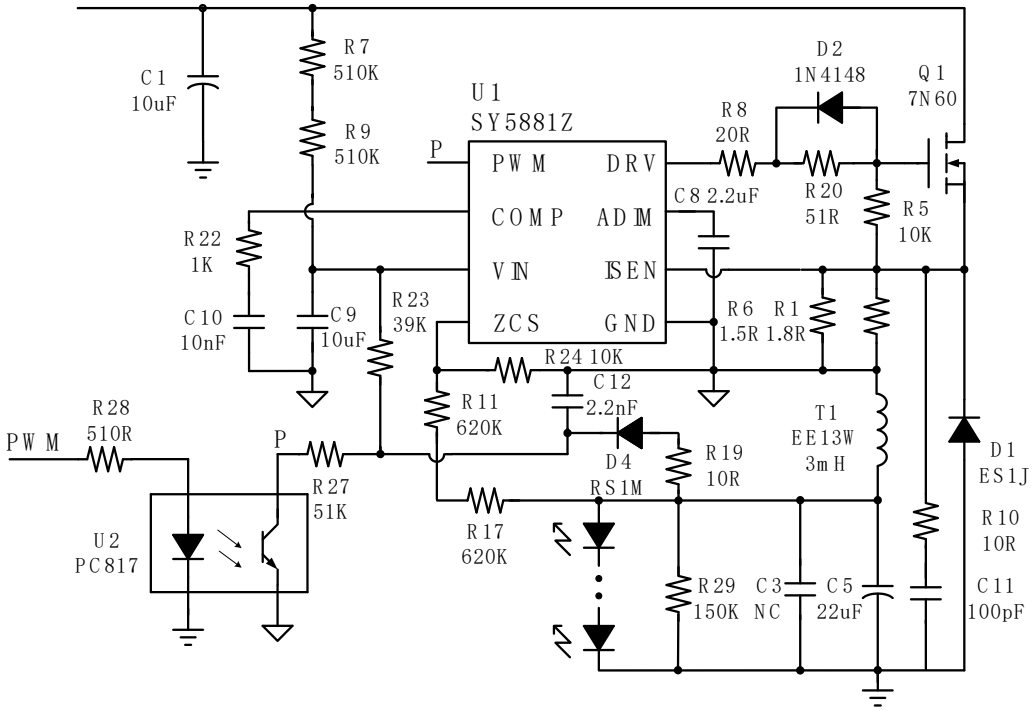
Refer to **Analog Dimming Mode Design**

$$C_{ADIM} \geq \frac{10^{-3}}{f_{PWM}} F \times Hz = \frac{10^{-3}}{1000} F = 1uF$$

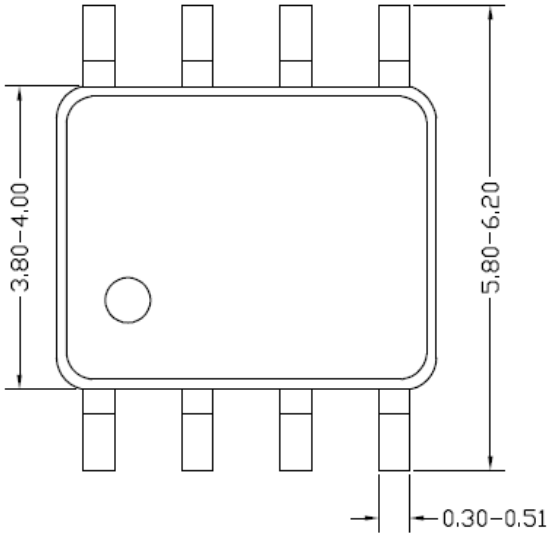
Hence C_{ADIM} is set to

C_{ADIM}=2.2uF

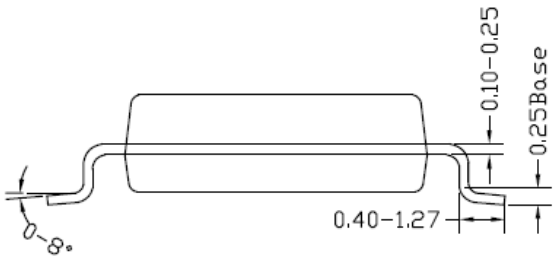
#9 final result



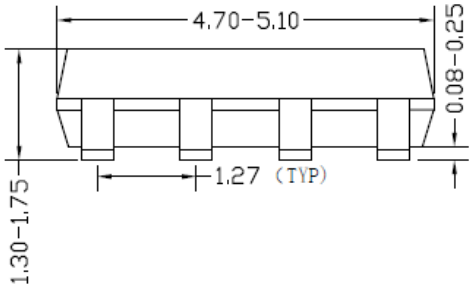
SO8 Package Outline & PCB Layout Design



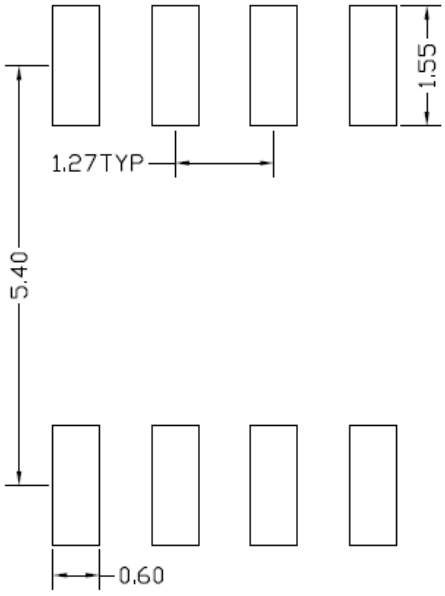
Top view



Side view



Front view

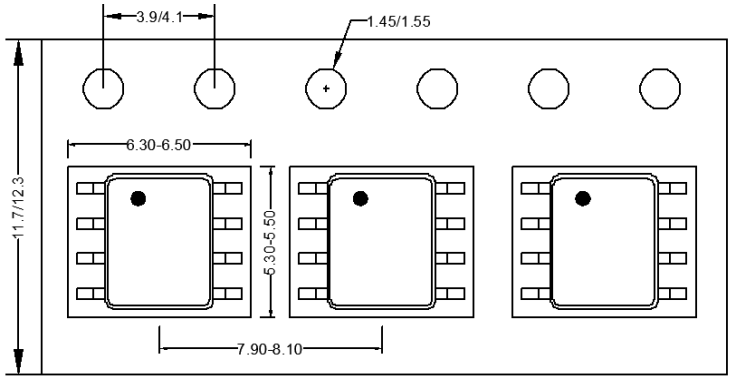


Recommended Pad Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

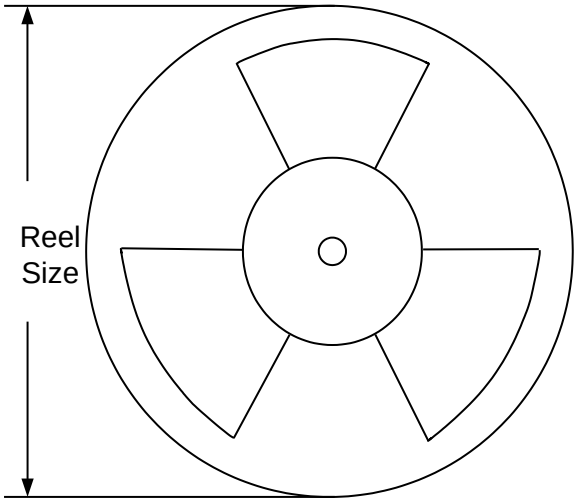
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 22,2020	Revision 0.9	Initial Risk Production Release
May 22,2021	Revision 1.0	Initial Production Release

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