钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TSV632A/TSV632

Dual and quad, rail-to-rail input/output, 60 µA, 880 kHz operational amplifiers

网址 www.sztdbdt.com

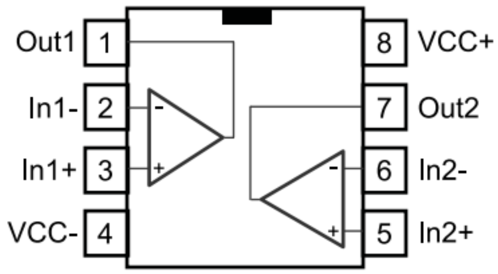
用芯智造 · 卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- ●Rail-to-rail input and output
- ●Low power consumption: 60 µA typ at 5 V
- ●Low supply voltage: 1.5 V - 5.5 V
- ●Gain bandwidth product: 880 kHz typ
- ●Unity gain stable on 100 pF capacitor
- ●Low power shutdown mode: 5 nA typ
- ●Low offset voltage: 800 µV max (A version)
- ●Low input bias current: 1 pA typ
- ●EMI hardened op amps
- ●Automotive qualification



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Applications

- ●Battery-powered applications
- ●Portable devices
- ●Signal conditioning
- ●Active filtering
- ●Medical instrumentation

Description

The TSV63x and TSV63xA series of dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.
This family features an excellent speed/power consumption ratio, offering an 880 kHz gain-bandwidth product while consuming only 60 µA at 5 V supply voltage. The devices also feature an ultralow input bias current and TSV633 and TSV635 have a shutdown mode.
These features make the TSV63x and TSV63xA family ideal for sensor interfaces, battery-supplied and portable applications, and active filtering.

2 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	V
V_{in}	Input voltage (3)		$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	V
I_{in}	Input current (4)		10	mA
$\overline{SHDN}$ SHDN	Shutdown voltage (3)		$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	V
T_{stg}	Storage temperature		-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient (5)(6)	DFN8 2x2	57	°C/W
		SOT23-8	105	
		MiniSO8	190	
		MiniSO10	113	
		SO8	125	
		QFN16 3x3	39	
		TSSOP14	100	
		TSSOP16	95	
T_j	Maximum junction temperature		150	°C
ESD	HBM: human body model (7)		4000	V
	MM: machine model (8)		300	
	CDM: charged device model (9)		1500	
	Latch-up immunity		200	mA

Notes:

(1) All voltage values, except the differential voltage are with respect to the network ground terminal.

(2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3) V_{CC} - V_{IN} must not exceed 6 V, V_{IN} must not exceed 6 V.

(4) Input current must be limited by a resistor in series with the inputs

(5) R_{th} are typical values

(6) Short-circuits can cause excessive heating and destructive dissipation

(7) Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

(8) Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating

(9) Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

3 Electrical characteristics

Table 4: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV63x			3	mV
		TSV63xA			0.8	
		TSV633AIST (MiniSO10)			1	
		$T_{min} < T_{op} < T_{max}$ - TSV63x			4.5	
		$T_{min} < T_{op} < T_{max}$ - TSV63xA			2	
		$T_{min} < T_{op} < T_{max}$ - TSV633AIST			2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		μV/°C
I_{io}	Input offset current	($V_{out} = V_{CC}/2$)		1	10 (1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current	($V_{out} = V_{CC}/2$)		1	10 (1)	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 1.8 V, V_{out} = 0.9 V	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 0.5 V to 1.3 V	85	95		
		$T_{min} < T_{op} < T_{max}$	80			
V_{OH}	High level output voltage, ($V_{OH} = V_{CC} - V_{out}$)	R_L = 10 kΩ		5	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low level output voltage	R_L = 10 kΩ		4	35	
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_o = 1.8 V	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	I_{source}	V_o = 0 V	6	10		
		$T_{min} < T_{op} < T_{max}$	4			
I_{CC}	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$	40	50	60	μA
		$T_{min} < T_{op} < T_{max}$			62	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz	700	790		kHz
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		45		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		13		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v = 1	0.2	0.27		V/μs
e_n	Equivalent input noise voltage	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		33		

Notes:

(1) Guaranteed by design

Table 5: Shutdown characteristics VCC = 1.8 V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current in shutdown mode (all channels)	$\overline{SHDN} = V_{CC-}$		2.5	50	nA
		$T_{min} < T_{op} < 85°$ C			200	nA
		$T_{min} < T_{op} < 125°$ C			1.5	µA
t_{on}	Amplifier turn-on time	R_L = 2 kΩ, V_{out} = (V_{CC-}) to (V_{CC-}) + 0.2 V		200		ns
t_{off}	Amplifier turn-off time	R_L = 2 kΩ, V_{out} = (V_{CC+}) - 0.5 V to (V_{CC+}) - 0.7 V		20		ns
V_{IH}	$\overline{SHDN}$ logic high		1.35			V
V_{IL}	$\overline{SHDN}$ logic low				0.6	V
I_{IH}	$\overline{SHDN}$ current high	$\overline{SHDN} = V_{CC+}$		10		pA
I_{IL}	$\overline{SHDN}$ current low	$\overline{SHDN} = V_{CC-}$		10		pA
I_{OLeak}	Output leakage in shutdown mode	$\overline{SHDN} = V_{CC-}$		50		pA
		$T_{min} < T_{op} < 125°$ C		1		nA

Table 3: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{ICM}	Common-mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	V
T_{oper}	Operating free-air temperature range	-40 to 125	°C

Table 6: VCC+ = 3.3 V, VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV63x			3	mV
		TSV63xA			0.8	
		TSV633AIST (MiniSO10)			1	
		$T_{min} < T_{op} < T_{max}$ - TSV63x			4.5	
		$T_{min} < T_{op} < T_{max}$ - TSV63xA			2	
		$T_{min} < T_{op} < T_{max}$ - TSV633AIST			2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		μV/°C
I_{io}	Input offset current	$V_{out} = V_{CC}/2$		1	10 [(1)]	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$		1	10 [(1)]	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V	88	98		
		$T_{min} < T_{op} < T_{max}$	83			
V_{OH}	High level output voltage, ($V_{OH} = V_{CC} - V_{out}$)	R_L = 10 kΩ		5	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low level output voltage	R_L = 10 kΩ		4	35	
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_o = 3.3 V	23	45		mA
		$T_{min} < T_{op} < T_{max}$	20			
	I_{source}	V_o = 0 V	23	38		
		$T_{min} < T_{op} < T_{max}$	20			
I_{CC}	Supply current, (per channel)	No load, V_{out} = 1.75 V	43	55	64	μA
		$T_{min} < T_{op} < T_{max}$			66	
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz	710	860		kHz
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		46		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		13		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_V = 1	0.22	0.29		V/μs

Notes:
(1) Guaranteed by design

Table 7: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{io}	Offset voltages	TSV63x			3	mV
		TSV63xA			0.8	
		TSV633AIST (MiniSO10)			1	
		$T_{min} < T_{op} < T_{max}$ - TSV63x			4.5	
		$T_{min} < T_{op} < T_{max}$ - TSV63xA			2	
		$T_{min} < T_{op} < T_{max}$ - TSV633AIST			2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	($V_{out} = V_{CC}/2$)		1	10 (1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current	($V_{out} = V_{CC}/2$)		1	10 (1)	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 1.8 to 5 V	75	102		
		$T_{min} < T_{op} < T_{max}$	73			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 4.5 V	89	98		
		$T_{min} < T_{op} < T_{max}$	84			
EMIRR	EMI rejection ratio, EMIRR = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mV_{rms}, f = 400 MHz		61		
		V_{RF} = 100 mV_{rms}, f = 900 MHz		85		
		V_{RF} = 100 mV_{rms}, f = 1800 MHz		92		
		V_{RF} = 100 mV_{rms}, f = 2400 MHz		83		
V_{OH}	High level output voltage, ($V_{OH} = V_{CC} - V_{out}$)	R_L = 10 kΩ		7	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
V_{OL}	Low level output voltage	R_L = 10 kΩ		6	35	
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	V_o = 5 V	40	69		mA
		$T_{min} < T_{op} < T_{max}$	35			
	I_{source}	V_o = 0 V	40	74		
		$T_{min} < T_{op} < T_{max}$	35			
I_{CC}	Supply current, (per channel)	No load, $V_{out} = V_{CC}/2$	50	60	69	µA
		$T_{min} < T_{op} < T_{max}$			72	
		AC performance				
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz	730	880		kHz
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF		830		
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		48		Degrees

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		13		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_v =1	0.25	0.34		V/μs
e_n	Equivalent input noise voltage	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		33		
THD+e_n	Total harmonic distortion + noise	V_{CC} = 5V, f = 1 kHz, A_v = 1, R_L = 100 kΩ, V_{icm} = V_{CC}/2, V_{out} = 2Vpp		0.002		%

Notes:
(1)Guaranteed by design

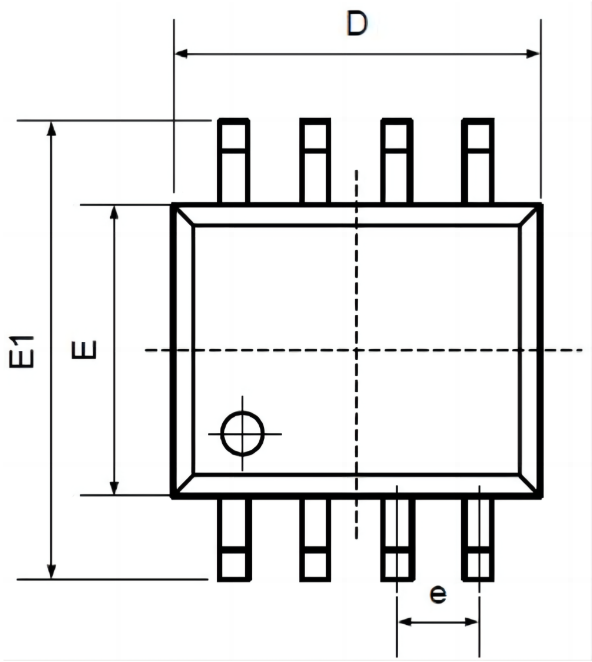
Table 8: Shutdown characteristics at VCC = 5 V

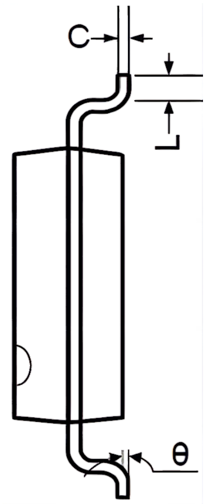
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current in shutdown mode (all channels)	$\overline{SHDN}$ = V_{CC-}		5	50	nA
		T_{min} < T_{op} < 85° C			200	
		T_{min} < T_{op} < 125° C			1.5	μA
t_{on}	Amplifier turn-on time	R_L = 2 kΩ, V_{out} = (V_{CC-}) to (V_{CC-}) + 0.2 V		200		ns
t_{off}	Amplifier turn-off time	R_L = 2 kΩ, V_{out} = (V_{CC+}) - 0.5 V to (V_{CC+}) - 0.7 V		20		
V_{IH}	$\overline{SHDN}$ logic high		2			V
V_{IL}	$\overline{SHDN}$ logic low				0.8	
I_{IH}	$\overline{SHDN}$ current high	$\overline{SHDN}$ = V_{CC+}		10		pA
I_{IL}	$\overline{SHDN}$ current low	$\overline{SHDN}$ = V_{CC-}		10		
I_{OLeak}	Output leakage in shutdown mode	$\overline{SHDN}$ = V_{CC-}		50		
		T_{min} < T_{op} < 125 °C		1		nA

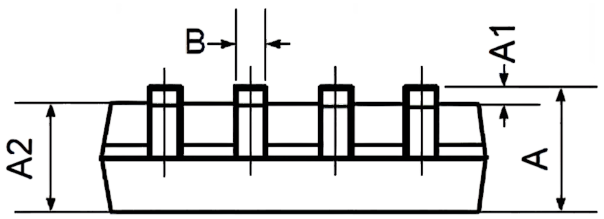
Order information

Order Number	Package	Package Quantity	Marking On The park
TSV632AIDT-TUDI	SOP8	Tape,Reel,2500	TSV632AIDT
TSV632IDT-TUDI	SOP8	Tape,Reel,2500	TSV632IDT

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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