3.1 W Digital Input mono Digital Smart K Audio Amplifier with I²C control interface

FEATURES

- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 9μV**
- **THD+N: 0.016%**
- Supports 4Ω Speaker
- Extensive Pop-Click Suppression
- I²C-bus control interface(≤1MHz)
- Three gain settings
- Volume control(from -96dB to 0dB)
- I²S /TDM interface：
  - I²S Philips,Left-Justified and Right-Justified
  - Supports 1/2/4/6/8 slots TDM
  - Input Sample Rates from 8kHz to 96kHz
  - Data Width: 16,20,24,32 Bits
  - Left/right selection and mono mixing
- PDM interface：
  - Input Sample Rates: 3M/6M/12M
  - Left/right selection
  - Low delay
- Power Supplies：
  - VBAT：2.5V-5.5V
  - DVDD: 1.65V~1.95V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- QFN 3.0mmX3.0mmX0.75mm-16L Package

APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

DESCRIPTION

AW88082QNR is an I²S/TDM/PDM input digital audio amplifier. Due to its 9μV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 3.1W output power into an 4Ω speaker at 10% THD+N.

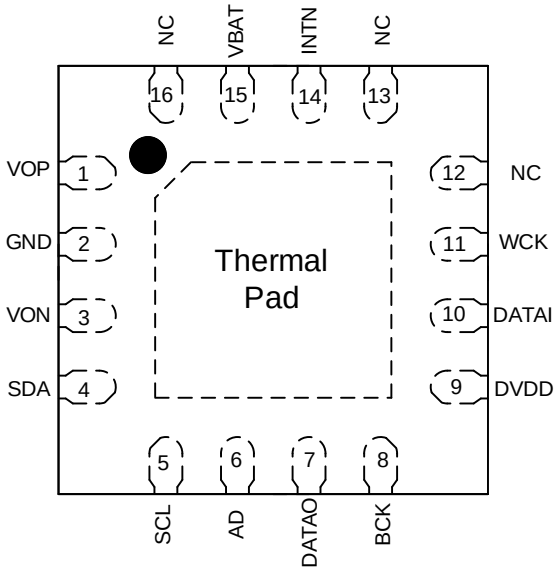
AW88082QNR features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I²C-bus interface, and the device address is configurable. Two devices can be combined to build a stereo application.

AW88082QNR offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

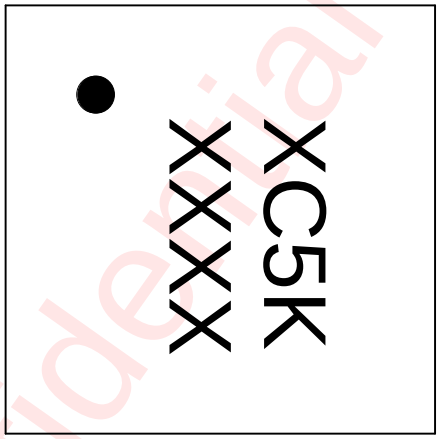
AW88082QNR is available in a QFN 3.0mmX3.0mmX0.75mm-16L package. The package is reliable and stable.

PIN CONFIGURATION AND TOP MARK

AW88082QNR
(Top View)



AW88082QNR Marking
(Top View)



XC5K - AW88082QNR
XXXX - Production Tracing Code

Figure 1 AW88082QNR pin diagram top view and device marking

PIN DESCRIPTION

Pin No	Pin Name	Description
1	VOP	Non-inverting Class-D output
2	GND	Ground
3	VON	Inverting Class-D output
4	SDA	I²C data IO
5	SCL	I²C clock input
6	AD	I²C device address selection
7	DATAO	I²S/TDM data out
8	BCK	I²S/TDM/PDM bit clock input
9	DVDD	Digital power supply
10	DATAI	I²S/TDM/PDM input data
11	WCK	I²S word select input
14	INTN	Interrupt output
15	VBAT	Battery power supply
12,13,16	NC	No connected

FUNCTIONAL BLOCK DIAGRAM

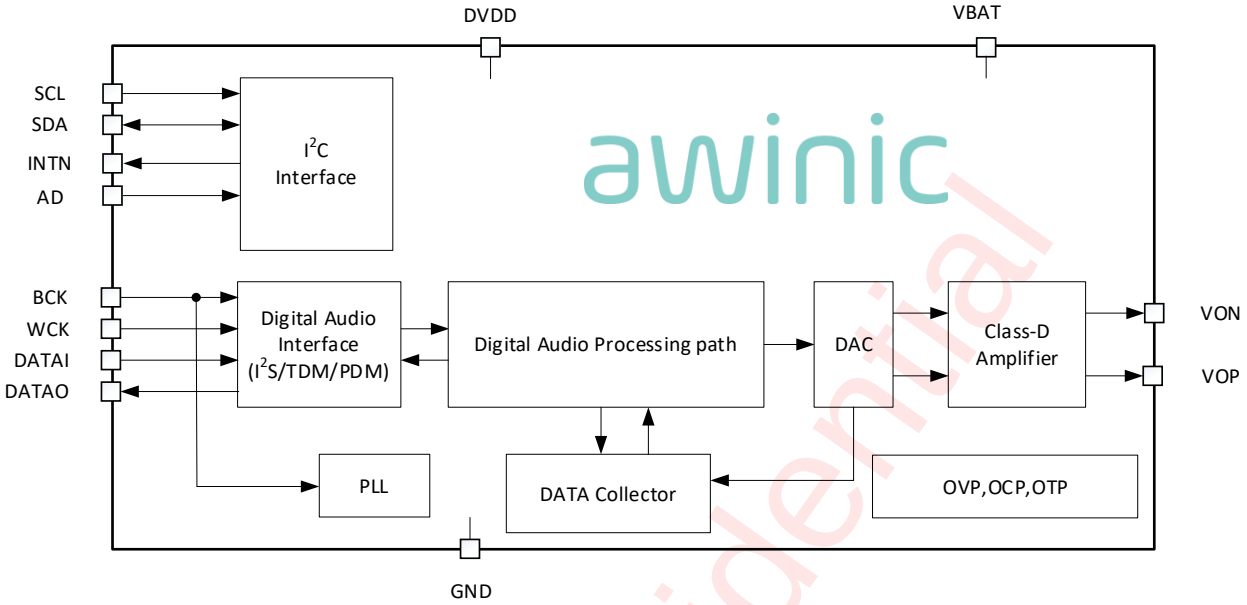


Figure 2 FUNCTIONAL BLOCK DIAGRAM

APPLICATION DIAGRAM

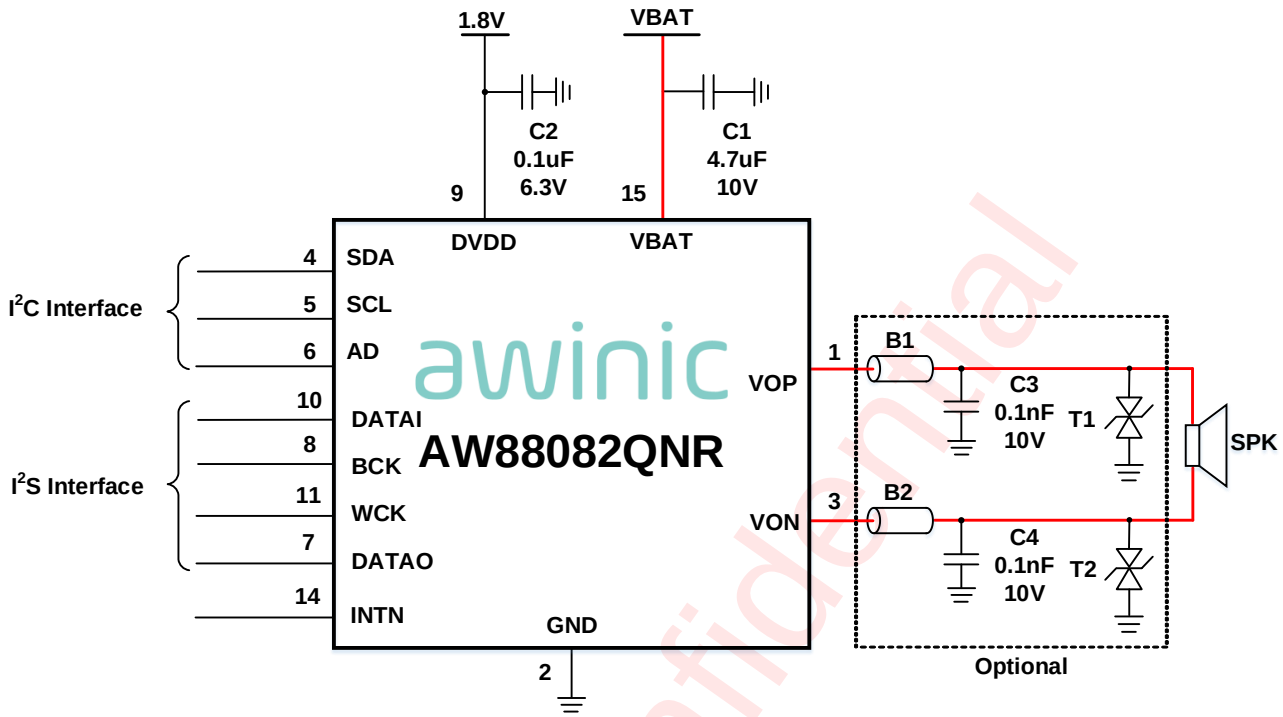


Figure 3 AW88082QNR Application Circuit

Note: Traces carry high current are marked in red in the above figure

ORDERING INFORMATION

Product Type	Temperature	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88082QNR	-40℃ ~ 85℃	QFN 3X3 – 16L	XC5K	MSL1	RoHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage V_{VBAT}	-0.3V to 6V
Digital Supply Voltage V_{DVDD}	-0.3V to 2V
VOP/VON pin voltage	-0.3 to V_{VBAT}
Minimum load resistance R_L	3.2Ω
Junction-to-ambient Thermal Resistance θ_{JA}	77.54°C/W
Junction-to-top Characterization Parameter Ψ_{JT}	12.13°C/W
Junction-to-board Thermal Resistance θ_{JB}	31.79°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 2,3)	
HBM (Human Body Model)	±2000V
CDM (Charge Device Model)	±1500V
Latch-up	
Test Condition：JESD78F	+IT：200mA -IT：-200mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023*

Note 3：*Test method of the charged device model: ESDA/JEDEC JS-002-2022*

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition: T_A=25°C, VBAT=3.6V, DVDD=1.8V , R_L=4Ω+33μH, f=1kHz(unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{VBAT}	Battery supply voltage	On pin VBAT	2.5		5.5	V
V_{DVDD}	Digital supply voltage	On pin DVDD	1.65	1.8	1.95	V
I_{VBAT}	Battery supply current	Operating mode,fs=48k		2.25		mA
		Operating mode,fs=32k		1.98		mA
		Standby mode		1.6		μA
		Power down mode, DVDD=0V		1.4	2.3	μA
I_{DVDD}	Digital supply current	Operating mode,fs=48k		2.28		mA
		Operating mode,fs=32k		1.49		mA
		Power down mode		1.5		μA
Class-D						
Po	RMS Output Power	THD+N=1%, R_L=4Ω, VBAT=3.6V, fi=100Hz		1.25		W
		THD+N=1%, R_L=4Ω, VBAT =5V, fi=100Hz		2.5		W
		THD+N=1%, R_L=8Ω, VBAT =3.6V, fi=100Hz		0.75		W
		THD+N=1%, R_L=8Ω, VBAT =5V, fi=100Hz		1.45		W
		THD+N=10%, R_L=4Ω, VBAT =3.6V, fi=100Hz		1.7		W
		THD+N=10%, R_L=4Ω, VBAT =5V, fi=100Hz		3.1		W
		THD+N=10%, R_L=8Ω, VBAT =3.6V, fi=100Hz		0.9		W
		THD+N=10%, R_L=8Ω, VBAT =5V, fi=100Hz		1.8		W
V_{OS}	Output offset voltage	I^2S signal input 0	-10	0	10	mV
F_{PWM}	PWM Switching frequency	Typical Sample Rate: 48kHz		384		kHz
η	Total efficiency	Po=1.3W		88		%
THD+N	Total harmonic distortion plus noise	Po=0.1W		0.016		%

Symbol	Description	Test Conditions		Min	Typ.	Max	Units
V_N	Output noise	A-weighting			9		μV
SNR	Signal-to-noise ratio	VBAT =5V, Po=2.3W, A-weighting			109		dB
PSRR	Power supply rejection ratio	V_{p-p_sin}=200mV	217Hz		88		dB
			1kHz		83		dB
Digital Logical Interface							
V_{IL}	Logic input low level	BCK,WCK,DATAI, SDA,SCL,AD Pin				0.3 x V_{DVDD}	V
V_{IH}	Logic input high level			0.7 x V_{DVDD}		3.6	V
V_{OL}	Logic output low level	I_{OUT}=4mA				0.45	V
V_{OH}	Logic output high level	I_{OUT}=-4mA		V_{DVDD} - 0.45		V_{DVDD}	V
Protection							
T_{SD}	Over temperature protection threshold				150		°C
T_{SDR}	Over temperature protection recovery threshold				130		°C
UVP	Under-voltage protection voltage				2.4		V
	Under-voltage protection hysteresis voltage				120		mV

[1] R_L = load resistance + load inductance.

DIGITAL AUDIO INTERFACE TIMING

I²S

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8	-	96	kHz
f_{bck}	Bit clock frequency, on pin BCK	32fs		128fs	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns
t_d	DATAO output delay time to BCK			50	ns

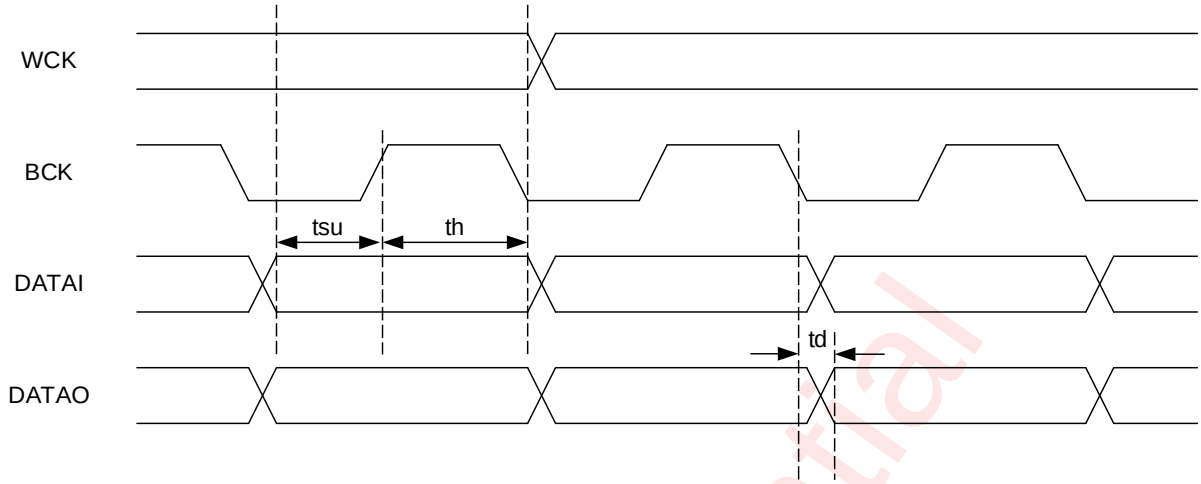


Figure 4 I²S Digital Audio Interface Timing

PDM

Parameter Name		Condition	Min	Typ.	Max	Units
f_{bck}	clock frequency, on pin BCK		3	-	12	MHz
δ_{bck}	clock duty cycle		40		60	%
t_{su}	DATAI Setup time to BCK	after clock HIGH	10	-	-	ns
		after clock LOW	10	-	-	ns
t_h	DATAI hold time to BCK	after clock HIGH	10	-	-	ns
		after clock LOW	10	-	-	ns

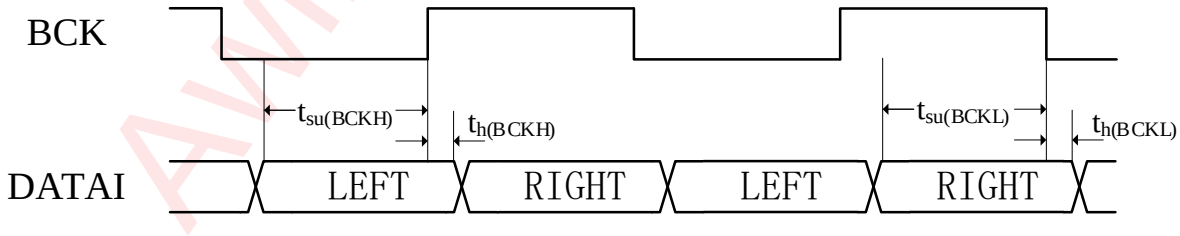
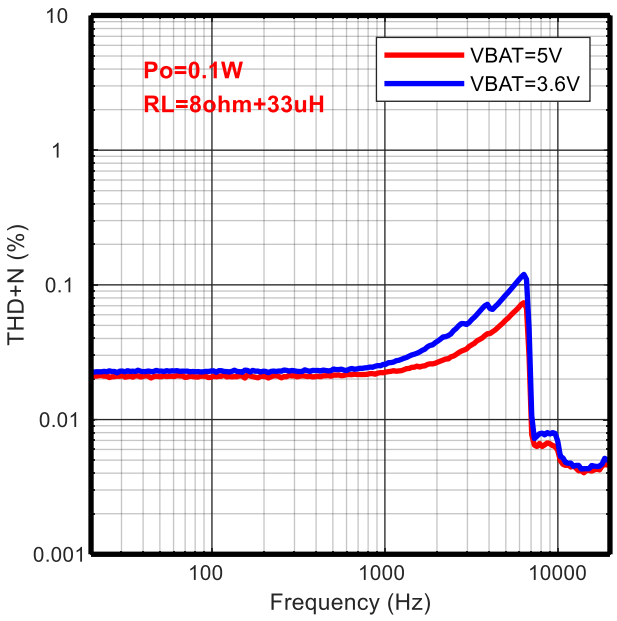


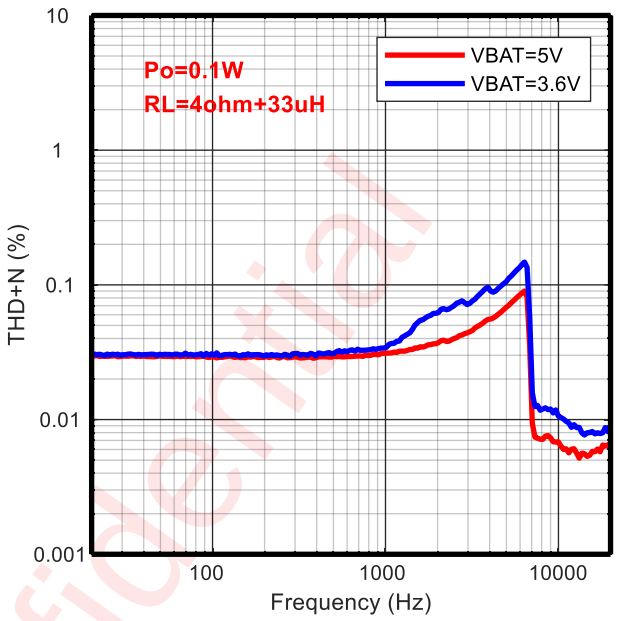
Figure 5 PDM Digital Audio Interface Timing

TYPICAL CHARACTERISTIC CURVES

THD+N VS. FREQUENCY



THD+N VS. FREQUENCY



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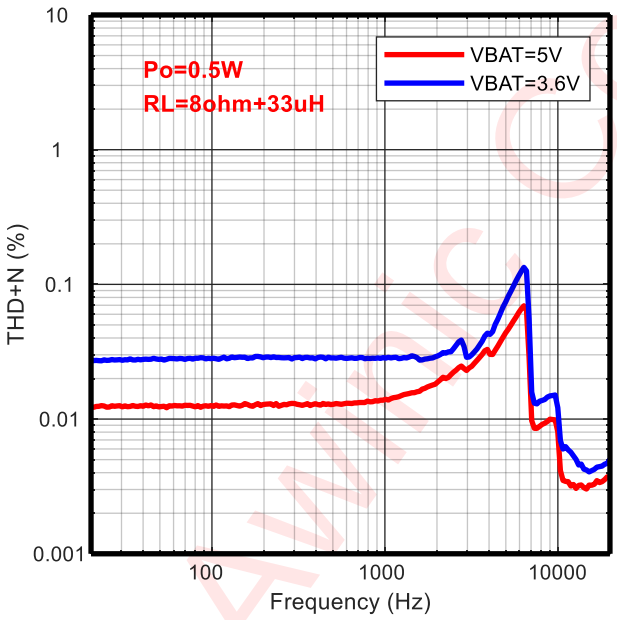
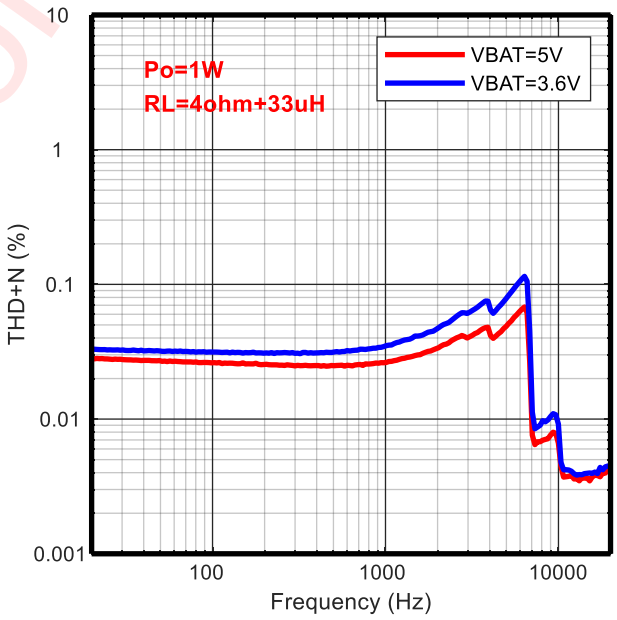
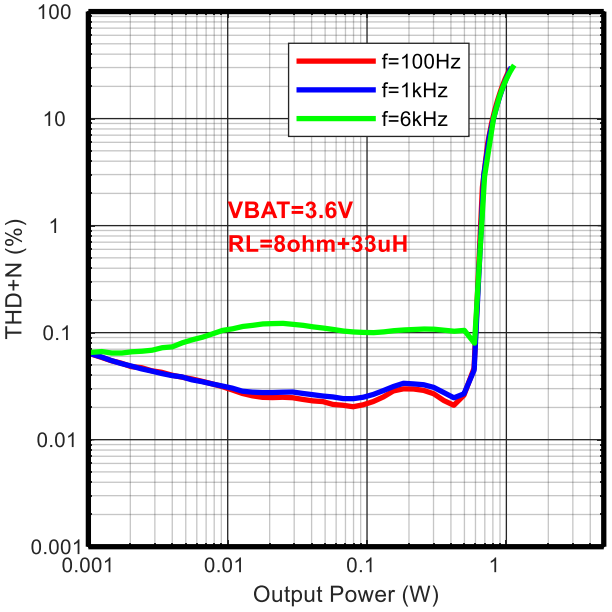


THD+N VS. FREQUENCY



THD+N VS. OUTPUT POWER



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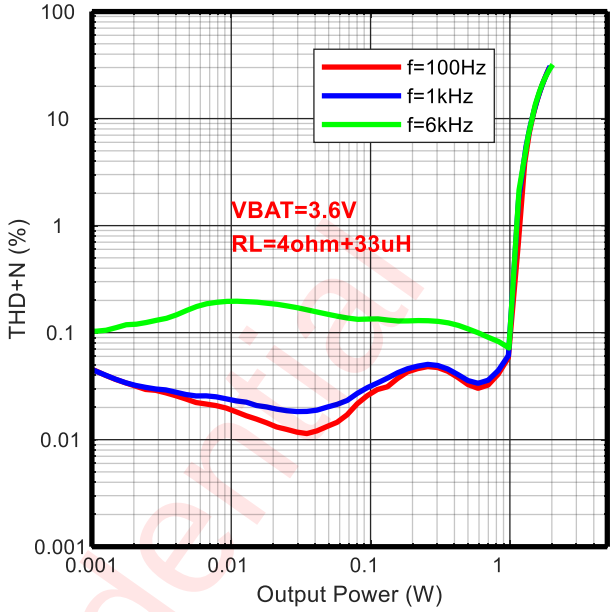
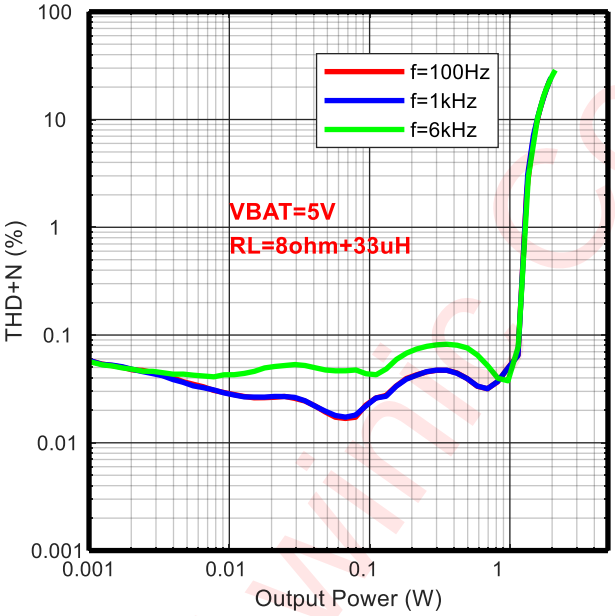
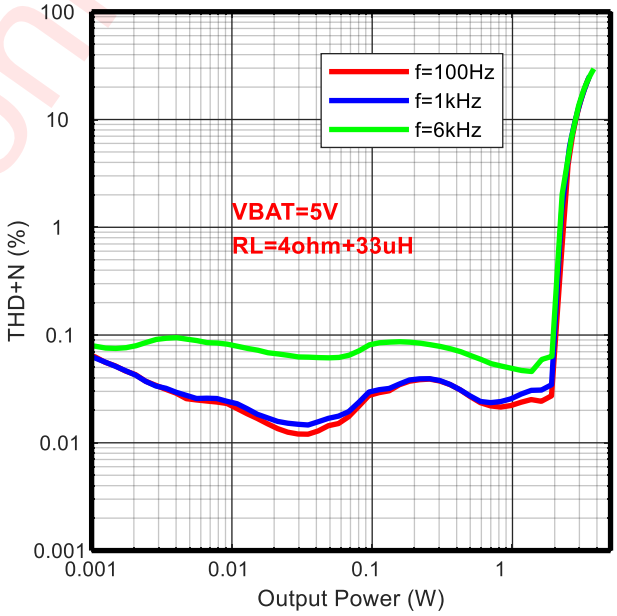


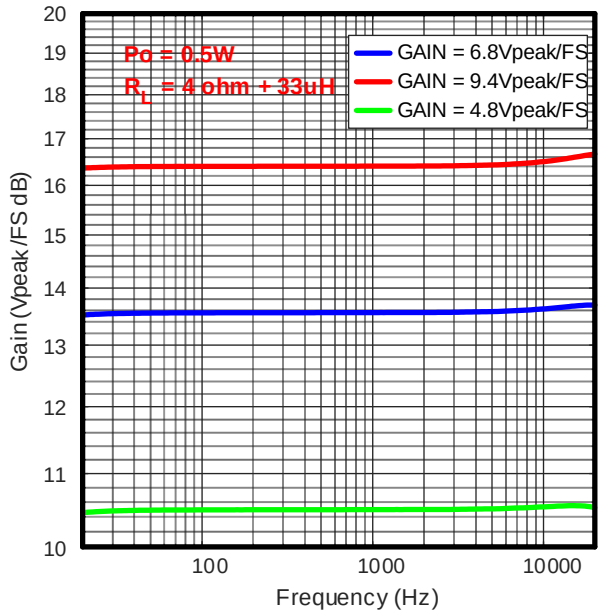
THD+N VS. OUTPUT POWER



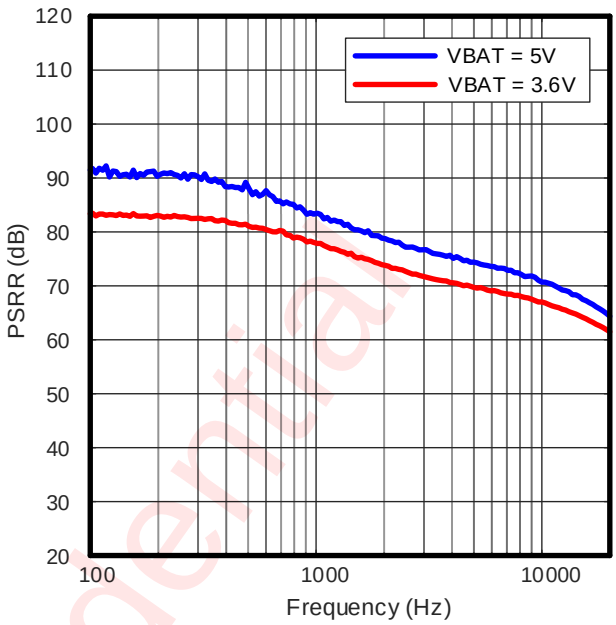
THD+N VS. OUTPUT POWER



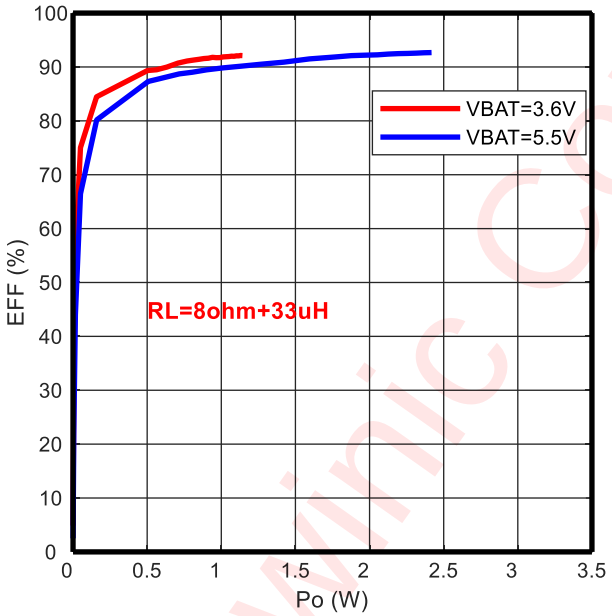
GAIN VS. FREQUENCY



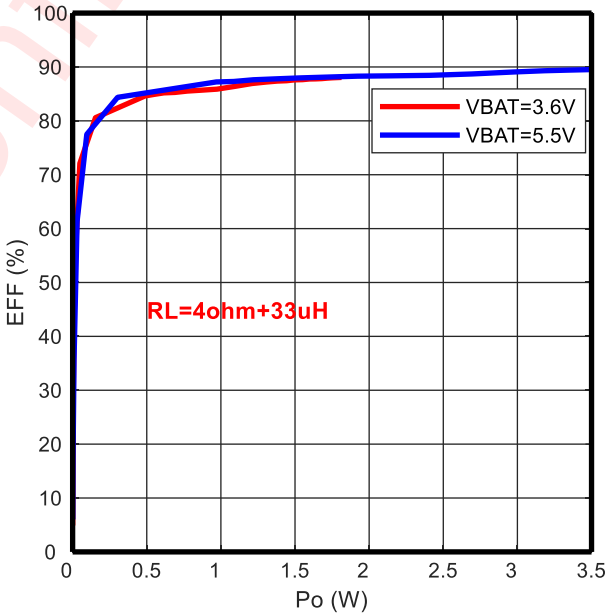
PSRR VS. FREQUENCY



EFFICIENCY VS. OUTPUT POWER



EFFICIENCY VS. OUTPUT POWER



DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VBAT and DVDD supply voltage. When the VBAT supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The internal reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{VBAT} < 2.1V V_{DVDD} < 1.1V	Power supply is not ready, chipset is power down.
Stand-By	V_{VBAT} > 2.5V V_{DVDD} > 1.65V	Power supply is ready, most parts of the device are power down for low power consumption except I^2C interface
Configuring	PWDN = 0	Device is biased while boost and Class-D output is floating. System configuration carried out in this mode
Operating	EN_PA = 1	Amplifier is fully operating

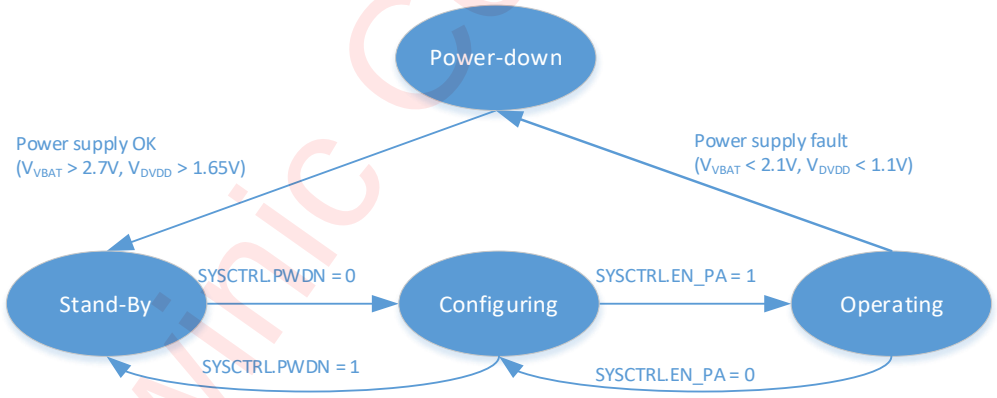


Figure 6 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{DVDD} < 1.1 V
- V_{VBAT} < 2.1 V

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

V_{DVDD} > 1.65 V and V_{VBAT} > 2.5 V

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

CONFIG MODE

The device switches to OFF mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.EN_PA= 0;

In this mode the internal bias, OSC, PLL will start to work

OPERATING MODE

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.EN_PA= 1 to make device in this mode.
This device power up sequence is illustrated in the following figure:

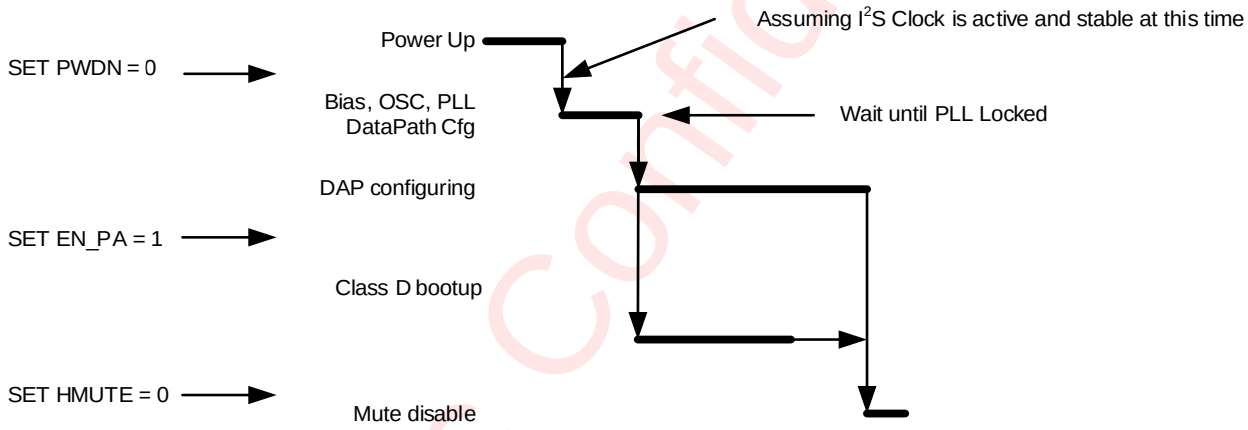


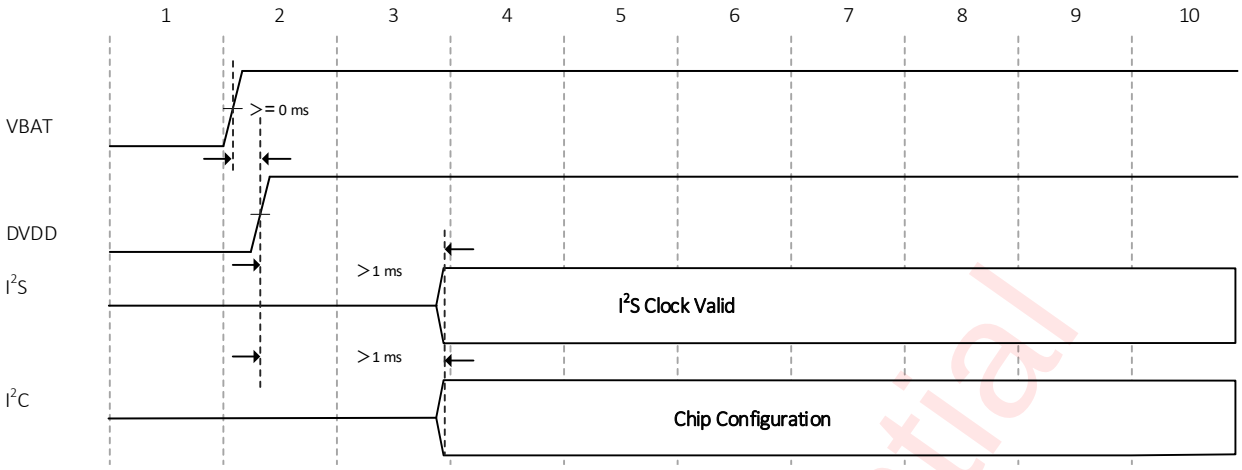
Figure 7 Power up sequence

Detail description for each step is listed in the following table.

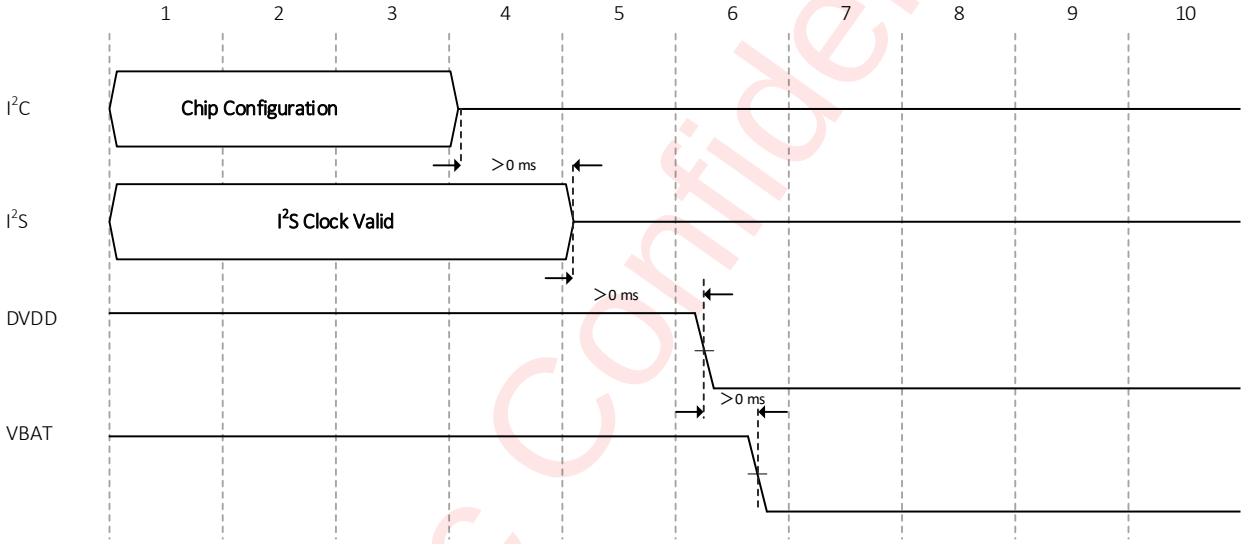
Table 2 Detail Description of Power up sequence

Index	description	Mode
1	Wait for VBAT、DVDD supply power up	Power-Down
2	I²S + Data Path Configuration	Stand-By
3.1	Enable system (SYSCTRL.PWDN = 0)	Configuring
3.2	Active Bias, OSC and PLL	
3.3	Wait for PLL to be locked	
4.1	Enable amplifier (SYSCTRL.EN_PA=1) Amplifier boot up	Operating
4.2	Wait for SYSST.SWS =1	
5	Release Hard-Mute Data Path active	

Power up sequence considering I²S, I²C timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

MODE SELECTION

AW88082QNR support I²S/PDM interface protocol. The default configuration is I²S. Customer can switch to PDM by I²C.

I²S DIGITAL AUDIO INTERFACE

The state of each digital input and output are shown in below table. After power on, the input signal pin BCK, WCK, DATAI are set to high impedance by default. If I2STXEN bit is enabled, DATAO is actively driven when outputting data otherwise it is high impedance by default.

Table 3 Detail Description of Digital I/O

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
INTN	Output	Hi-Z
AD	Input	Weak pull down
BCK	Input	Hi-Z
WCK	Input	Hi-Z
DATAI	Input	Hi-Z
DATAO	Output	Hi-Z

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATAI
- DATAO

Two-slot I²S and 1/2/4/6/8-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device sup

ports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL1.I2SBCK. The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 4-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL.

Table 4 Supported I²S interface parameters

Interface format(MSB first)	Data width	BCK frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs /64fs

Interface format(MSB first)	Data width	BCK frequency
left-justified	16b/20b/24b/32b	32fs/48fs /64fs
right-justified	16b/20b/24b/32b	32fs /48fs /64fs

The output port DATAO, can be enabled or disabled via bit I2SCTRL3.I2STXEN. The unused slots can be set to Hi-z or zero, which is controlled by I2SCTRL3.DOHZ.

STANDARD I²S MODE

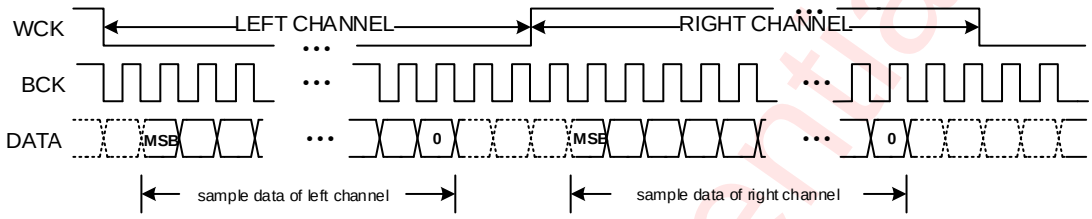


Figure 8 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

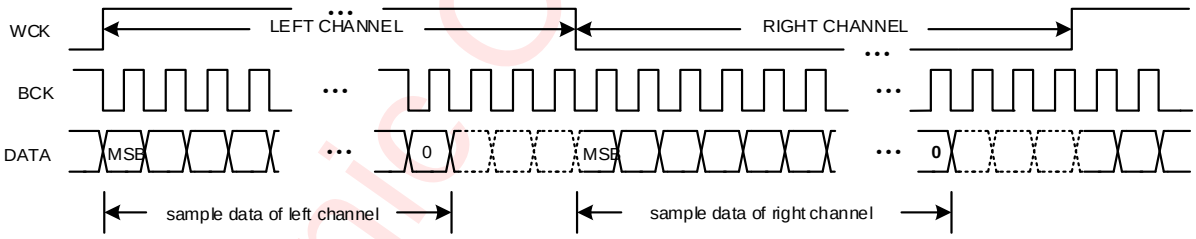


Figure 9 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

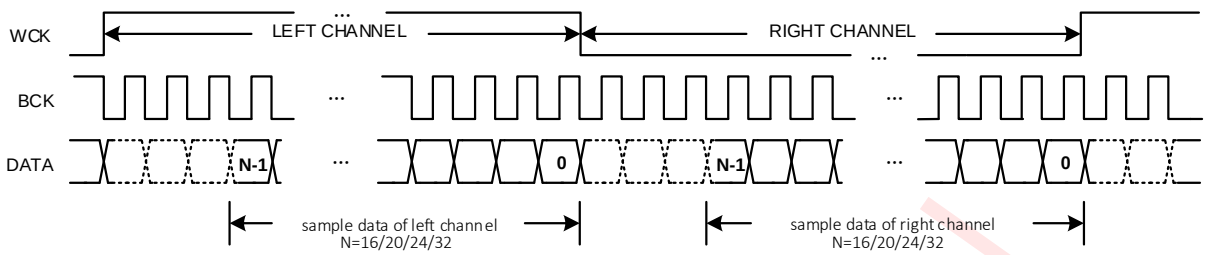


Figure 10 I²S Timing for Right-Justified Mode

- When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 4-slot is supported in TDM mode, while 2-slot is supported in I²S mode

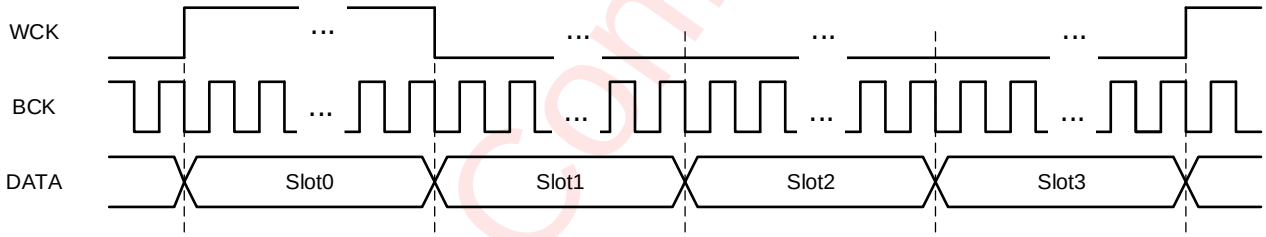


Figure 11 TDM Timing

Note: The high level pulse width of WCK signal can be one slot time or one period of BCK.

PDM DIGITAL AUDIO INTERFACE

AW88082QNR supports the digital stereo PDM stream illustrated in Figure 12. The BCK frequency support 3M/6M/12M. It is selected via configurable register PDMCTRL.INTF_MODE.

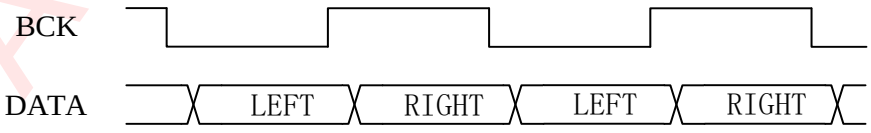


Figure 12 Digital stereo PDM Timing

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by PDMCTRL.PDM_CHSEL.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the DAP (Digital Audio Processor) is illustrated in the following figure.

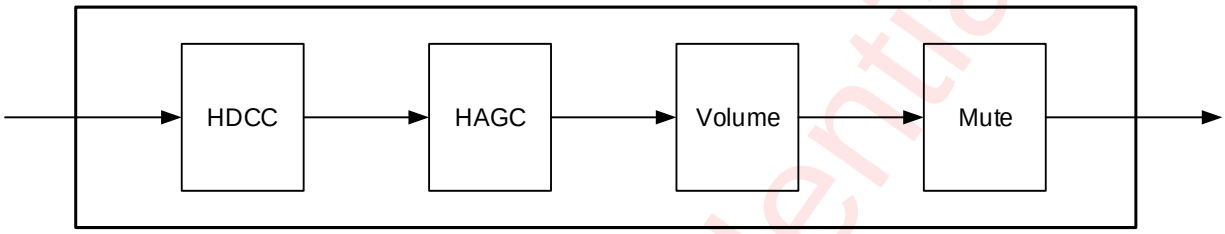


Figure 13 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker, such as in the 5V power supply, as for 4Ω speaker, the maximum undistorted power is about 3.1W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with hardware AGC can protect the speaker effectively, When the output power is not exceeding the setting threshold, the hardware AGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the hardware AGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -96.162db with 0.094db/step

MUTE

This module performs mute control for the audio stream

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

The circuit of device has integrated the over voltage protection control loop. When the voltage of VBAT is above the threshold, the device will stop working, until the voltage of VBAT going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to VBAT/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

Table 5 Address Selection

AD	Address(7-bit)
Connect to GND	0x34
Connect to DVDD	0x35
Connect to SCL	0x36
Connect to SDA	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

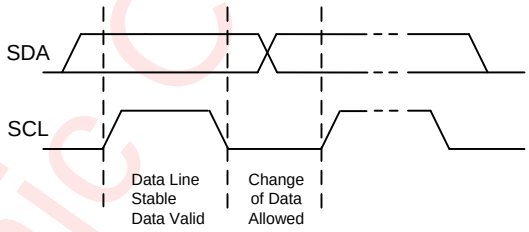


Figure 14 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

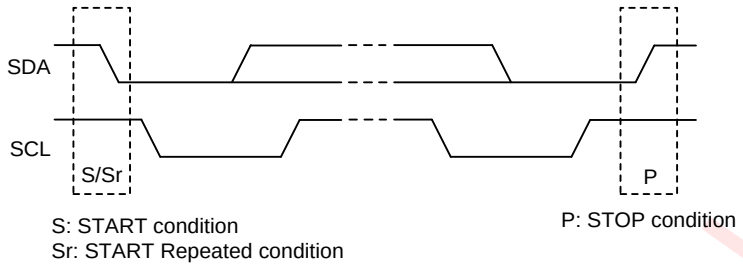


Figure 15 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

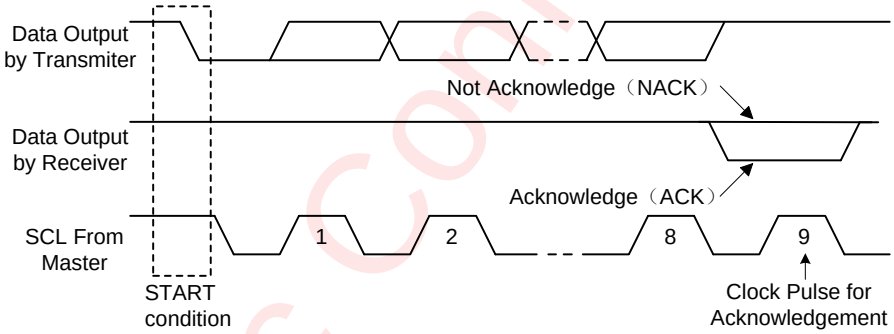


Figure 16 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends high data byte of 16-bit data to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends low data byte of 16-bit data to be written to the addressed register

i) Slave sends acknowledge signal

j) If master will send further 16-bit data bytes, the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)

k) Master generates STOP condition to indicate write cycle end

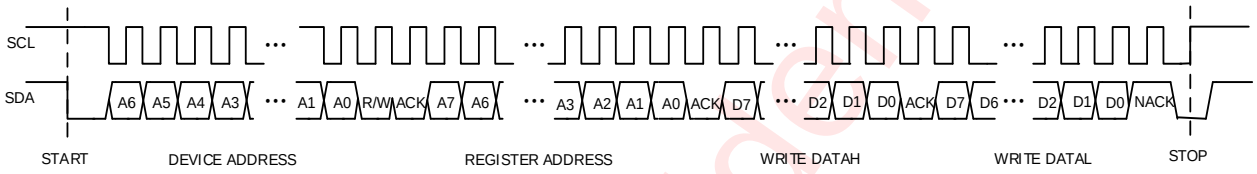


Figure 17 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

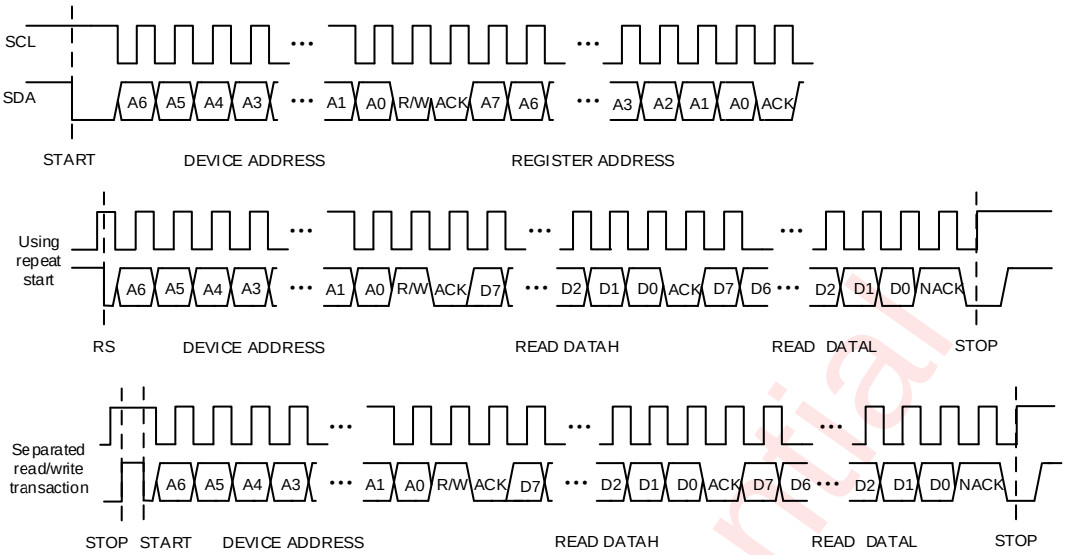


Figure 18 I²C Read Byte Cycle

REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	RO	IDCODE																0x2116
0x01	SYSST	RO		UVLS	UVL_DVDDS					SWS	CLIPS	PATTERN_MODES	NOCLKS	CLKS	OCDS	BOPS	OTHS	PLLS	0x0000
0x02	SYSINT	RC		UVLI	UVL_DVDDI					SWI	CLIPI	PATTERN_MODEI	NOCLKI	CLKI	OCDI	BOPI	OTHI	PLLI	0x0000
0x03	SYSINTM	RW		UVLM	UVL_DVDDM					SWM	CLIPM	PATTERN_MODEM	NOCLKM	CLKM	OCDM	BOPM	OTHM	PLLM	0x61FF
0x04	SYSCTRL	RW		ULS_HMUTE	SET_GAIN		RMSE	HAGCE	HDCCE	HMUTE		I2SEN	WSINV	BCKINV	IPLL	EN_PLL	EN_PA	PWDN	0x2246
0x05	SYSCTRL2	RW	BOP_VOL_EN	BOP_EN		ULS_MODE	INTMODE	INTN	VOL										0x8000
0x06	I2SCTRL1	RW		CFSEL			CHSEL		I2SMD		I2SFS		I2SBCK		I2SSR				0x04E8
0x07	I2SCTRL2	RW		SLOT_NUM			I2S_TX_SLOTVLD				I2S_RXR_SLOTVLD				I2S_RXL_SLOTVLD				0x0010
0x08	I2SCTRL3	RW									FSYNC_TYPE	I2STXEN		I2SRXEN		I2SDOSEL	DOHZ	I2SCHS	0x0056
0x09	DACCFG1	RW	RVTH								AVTH								0x4B6A
0x0A	DACCFG2	RW	ATTH																0x000F
0x0B	DACCFG3	RW	RTTH																0x01E0
0x0C	DACCFG4	RW									HOLDTH								0x1C1E
0x19	PDMCTRL	RW	INTF_MODE		PDM_CHSEL	CIC_ORDER													0x0000

DETAILED REGISTER DESCRIPTION

ID: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	IDCODE	RO	Chip ID will be returned after read. All configuration registers will be reset to default value after 0x55aa is written	0x2116

SYSST: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RO	Not used	0
14	UVLS	RO	VBAT under UVLO threshold voltage indicator 0: Normal 1: UVLO	0
13	UVL_DVDDS	RO	DVDD under UVLO threshold voltage indicator 0: Normal 1: UVLO	0
12:9	Reserved	RO	Not used	0
8	SWS	RO	Ampifier switching status. 0: Not switching 1: Switching	0
7	CLIPS	RO	Ampifier clipping status. 0: Not clipping 1: Clipping	0
6	PATTERN_MODES	RO	setting mode/operating mode signal	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0
4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCDS	RO	Over current status in amplifier 0: Noraml 1: OC	0
2	BOPS	RO	whether bop status is triggered or not 0: not triggered 1: triggered	0
1	OTHS	RO	Die Temperature is higher than 160degrees 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RC	Not used	0
14	UVLI	RC	Interrupt indicator for Power On and VBAT UVLS	0
13	UVL_DVDDI	RC	Interrupt indicator for Power On and UVL_DVDDS	0
12:9	Reserved	RC	Not used	0
8	SWI	RC	Interrupt indicator for SWS.	0
7	CLIPI	RC	Interrupt indicator for CLIPS.	0
6	PATTERN_MODEI	RC	setting mode/operating mode signal	0

5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCDI	RC	Interrupt indicator for OCDS	0
2	BOPI	RC	Interrupt indicator for BOPS	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14	UVLM	RW	Interrupt mask for UVLI.	1
13	UVL_DVDDM	RW	Interrupt mask for UVL_DVDDI.	1
12:9	Reserved	RW	Not used	0
8	SWM	RW	Interrupt indicator for SWI.	1
7	CLIPM	RW	Interrupt indicator for CLIPI.	1
6	PATTERN_MODEM	RW	setting mode/operating mode signal	1
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCDM	RW	Interrupt mask for OCDI.	1
2	BOPM	RW	Interrupt mask for BOPS.	1
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

SYSCTRL: (Address 04h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14	ULS_HMUTE	RW	Only when HMUTE&ULS_HMUTE=1, ultrasound can be muted 0:disable 1:enable	0
13:12	SET_GAIN	RW	RCV Mode gain setting 00: AV=4.2 01:AV=4.8 10:AV=6.8 11:AV=9.4	2
11	RMSE	RW	Hardware HAGC mode selection 0: Peak AGC 1: RMS AGC	0
10	HAGCE	RW	Disable/Enable Hardware AGC 0: disable 1: enable	0
9	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: disable 1: enable	1
8	HMUTE	RW	Disable/Enable Hardware mute module 0: disable 1: enable	0
7	Reserved	RW	Not used	0
6	I2SEN	RW	Disable/Enable whole I^2S interface module 0: disable 1: enable	1

5	WSINV	RW	I²S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I²S bit clock invert control 0: Not invert 1: Inverted	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: No used	0
2	EN_PLL	RW	PLL enalbe control	1
1	EN_PA	RW	ClassD enable control	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	0

SYSCTRL2: (Address 05h)

Bit	Symbol	R/W	Description	Default
15	BOP_VOL_EN	RW	Enable/Disable Volume control module in brownout protection mode 0: Disable 1: Enable	1
14	BOP_EN	RW	whether enable bop or not 0: disable 1: enable	0
13	Reserved	RW	Not used	0
12	ULS_MODE	RW	Ultrasonic mode control 0: Legacy 1: TDM	0
11	INTMODE	RW	Interrupt pad INTN output mode selection 0: Open-drain 1: Push&Pull	0
10	INTN	RW	Interrupt pad INTN pin-source selection 0: SYSINT 1: SYSST	0
9:0	VOL	RW	Volume control, from 0 to -96dB, in unit of -6.02/64dB	0

I2SCTRL1: (Address 06h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14:12	CFSEL	RW	I²S legacy path output data selection 000: HAGC 001:INTP 010: REG_OUT Others: Reserved	0
11:10	CHSEL	RW	Left/right channel selection for I²S input 00: Reserved 01: Left 10: Right 11: Mono	1
9:8	I2SMD	RW	I²S interface mode selection 00: Philip Standard 01: MSB justified 10: LSB justified 11: Reserved	0

7:6	I2SFS	RW	I²S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	3
5:4	I2SBCK	RW	I²S BCK mode 00: 32*fs 01: 48*fs 10: 64*fs 11: Reserved	2
3:0	I2SSR	RW	I²S interface sample rate configuration 0000: 8 KHz 0001: 11 KHz 0010: 12 KHz 0011: 16 KHz 0100: 22 KHz 0101: 24 KHz 0110: 32 KHz 0111: 44 KHz 1000: 48 KHz 1001: 96 KHz Others: Reserved	8

I2SCTRL2: (Address 07h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14:12	SLOT_NUM	RW	I²S TDM mode control (support max to 16 slots). 000: I²S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: TDM16s	0
11:8	I2S_TX_SLOTVLD	RW	TX slot selection, data will be sent to one of the 16 slots. 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 …… 1111: Slot 15	0
7:4	I2S_RXR_SLOTVLD	RW	RX right channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 …… 1111: Slot 15	1

3:0	I2S_RXL_SLOTVLD	RW	RX left channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 …… 1111: Slot 15	0

I2SCTRL3: (Address 08h)

Bit	Symbol	R/W	Description	Default
15:8	Reserved	RW	Not used	0
7	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-bck	0
6	I2STXEN	RW	Disable/Enable I²S transmitter module 0: disable 1: enable	1
5	Reserved	RW	Not used	0
4	I2SRXEN	RW	Disable/Enable I²S receiver module 0: disable 1: enable	1
3	Reserved	RW	Not used	0
2	I2SDOSEL	RW	I²S unused channels output data selection 0: Zeros 1: TXData	1
1	DOHZ	RW	Unused channel Data control, When it is set to 0, all Channels are available with same data. Otherwise Unused channel is set to be HiZ. 0: All 1: HiZ	1
0	I2SCHS	RW	I²S Tx Channel selection 0: Left 1: Right	0

DACCFG1: (Address 09h)

Bit	Symbol	R/W	Description	Default
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale	0x4B
7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC) : P0= ((i/256*Gain)**2)/RLoad/2 RMSE = 1 (RMS AGC) : P0=(i/256)*(Gain**2)/RLoad i is the register value, default 0x40 Gain is the Amplifier Gain configured by SYSCTRL.SPK_GAIN, default 6.8 RLoad is 8ohm/4ohm for different application, default 4 ohm	0x6A

DACCFG2: (Address 0Ah)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8us	0x000F

DACCFG3: (Address 0Bh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x01E0

DACCFG4: (Address 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:8	Reserved	RW	Not used	0
7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	0x1E

PDMCTRL: (Address 19h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:14	INTF_MODE	RW	Control the interface 00:I²S 01:PDM 3M 10:PDM 6M 11:PDM 12M	0
13	PDM_CHSEL	RW	PDM Left/Right channel select 0:left 1:right	0
12	CIC_ORDER	RW	The order of CIC filter 0:4 stages 1:3 stages	0
11:0	Reserved	RW	Not used	0

APPLICATION INFORMATION

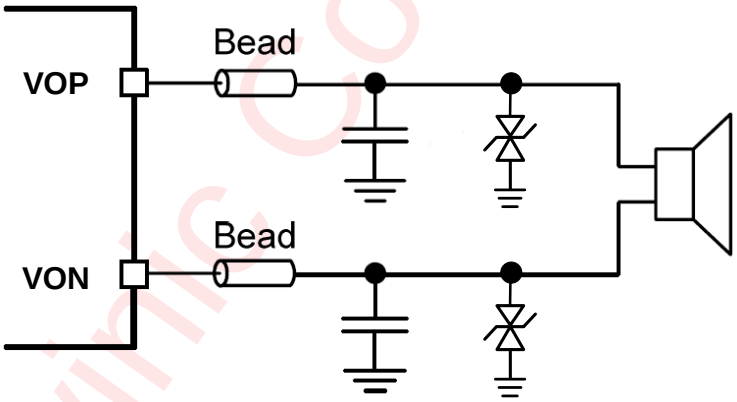
EXTERNAL COMPONENTS

SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 4.7μF low equivalent-series-resistance (ESR) ceramic capacitor is recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 4.7μF ceramic capacitor, place a 10μF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

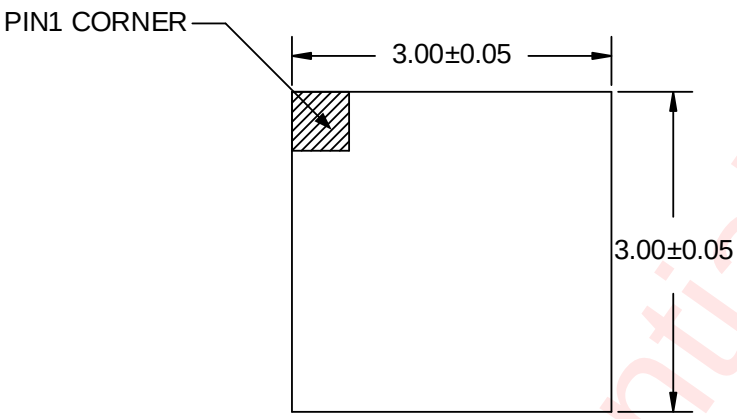
If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 10V. The output(VOP/VON) can reserve ESD devices, used to improve ESD protection capabilities.



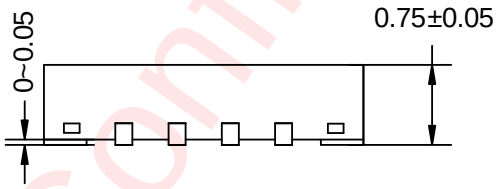
LAYOUT CONSIDERATION

In order to obtain excellent performance of the PA, the below PCB layout guidelines should be followed:
All the filter capacitors should be placed close to the corresponding pins of the PA, including VBAT, DVDD.
The beads and capacitor should be placed close to the VOP and VON pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 1.2mm.
The via numbers determine the current capability.

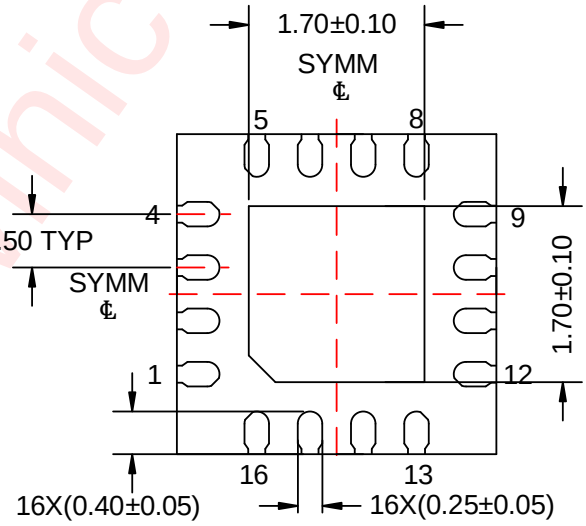
PACKAGE DESCRIPTION



Top View



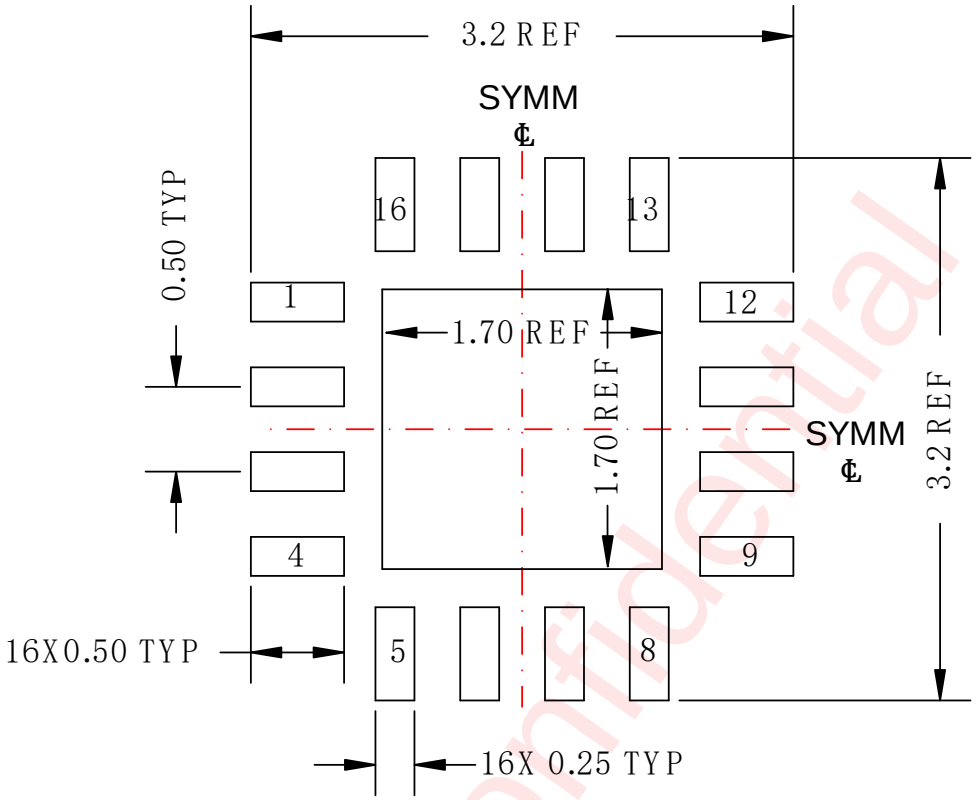
Side View

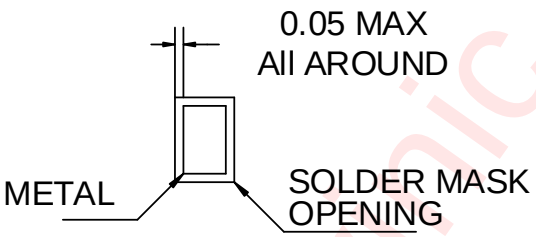


Bottom View

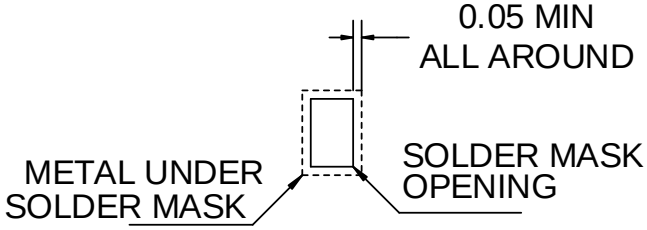
Unit：mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED

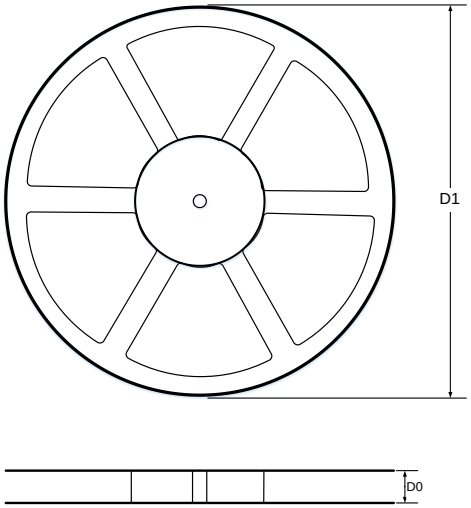


SOLDER MASK DEFINED

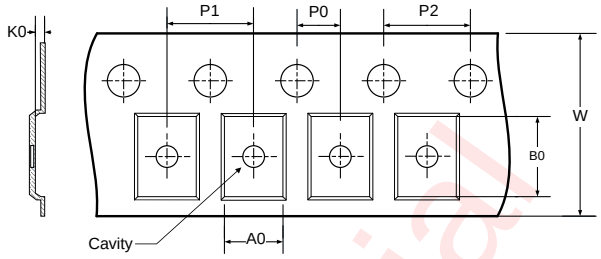
Unit: mm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

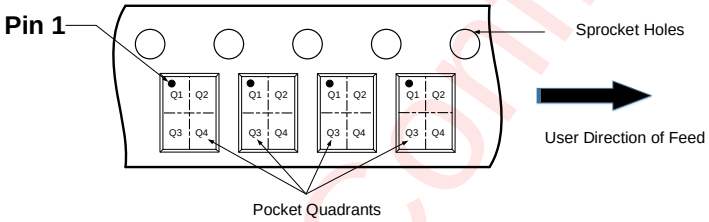


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

All dimensions are nominal

REVISION HISTORY

Version	Date	Change Record
V1.0	Feb. 2024	Officially Released
V1.1	Aug. 2025	Update data input interface description and Minimum load resistance R_L Correct register list

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