3.2 W I²S/TDM Input, High Efficiency, Digital Smart K Audio Amplifier

Features

- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 10μV**
- **Low shutdown current: 0.15uA**
- **Fast turn-on times：1ms**
- **THD+N: 0.02%**
- Supports 4Ω Speaker
- Extensive Pop-Click Suppression
- Support spread spectrum
- I²S interface：
  - I²S, Left-Justified and Right--Justified
  - Supports 1/2/4/6/8 slots
  - Input Sample Rates from 8kHz to 96kHz
  - Data Width: 16, 20, 24, 32 Bits
- Power Supplies：
  - VDD：2.5V-5.5V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection
- WLCSP 1.403mmX1.183mm-12B package

Applications

- Mobile phones
- Wearable Device
- Portable Audio Devices

Description

The AW88083A is an I2S input digital audio amplifier. Due to its 10μV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 3.2W output power into an 4Ω speaker at 10% THD+N.

The AW88083A features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface.

The AW88083A support spread spectrum and edge-rate limiting to enhance EMI performance while reduces output filter size and cost.

The AW88083A offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection to protect the device.

AW88083A is available in a WLCSP 1.403mmX1.183mm-12B package.

PIN CONFIGURATION AND TOP MARK

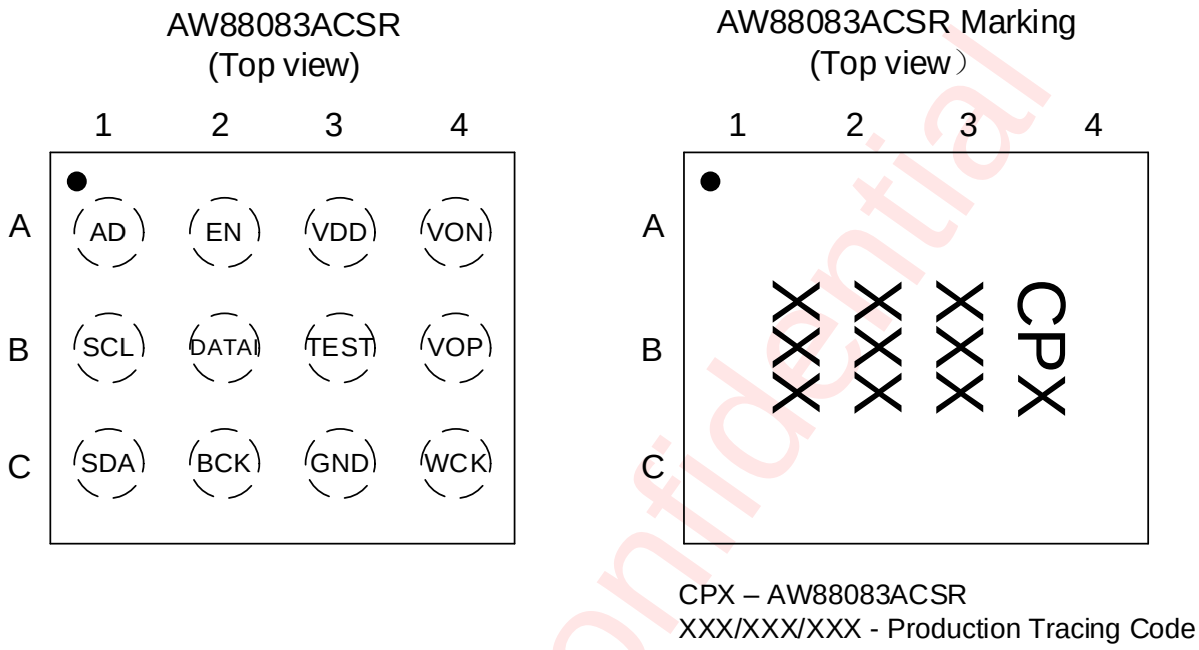


Figure 1 AW88083ACSR pin diagram top view and device marking

PIN DESCRIPTION

Pin No	Pin Name	Description
A1	AD	I2C device address selection
A2	EN	Enable pin (active High)
A3	VDD	Battery power supply
A4	VON	inverting Class-D output
B1	SCL	I2C clock input
B2	DATAI	I2S/TDM data input
B3	TEST	Test signal, connected to ground
B4	VOP	Non-inverting Class-D output
C1	SDA	I2C data IO
C2	BCK	I2S/TDM bit clock input
C3	GND	GND
C4	WCK	I2S word select input / TDM frame sync signal

FUNCTIONAL BLOCK DIAGRAM

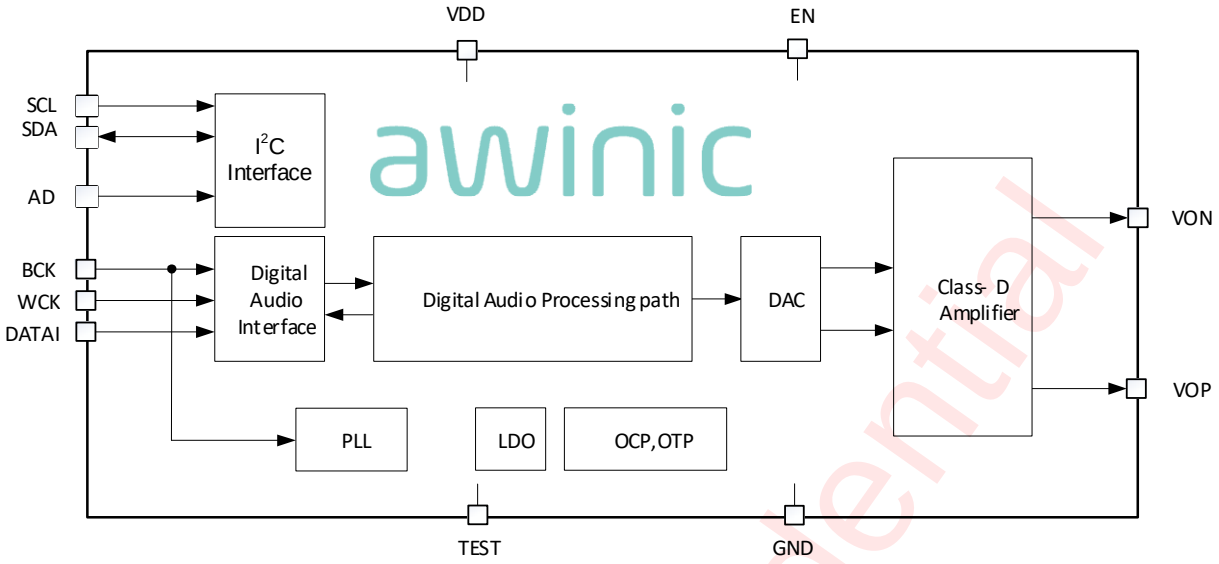


Figure 2 FUNCTIONAL BLOCK DIAGRAM

APPLICATION DIAGRAM

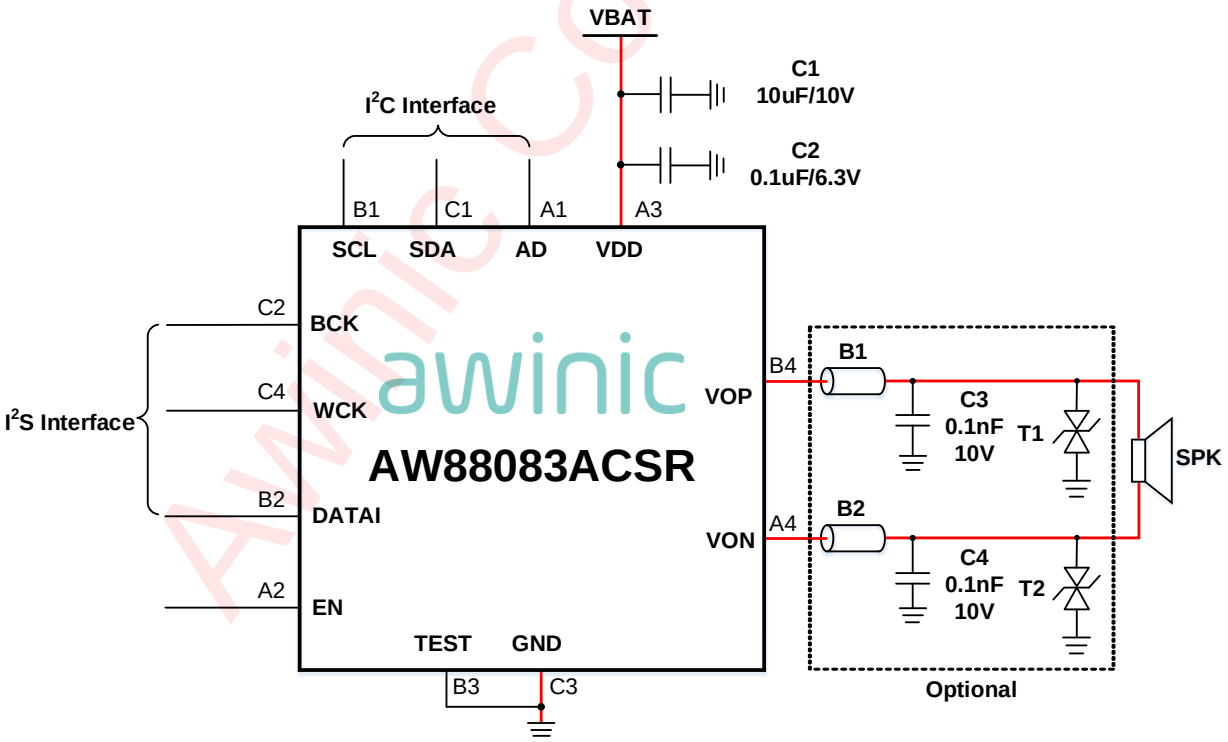


Figure 3 AW88083A Application Circuit

Note: Traces carry high current are marked in red in the above figure

ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage and Digital Interface Voltage (VDD, SDA, SCL, BCK, WCK, DATAI pins)	-0.3V to 6V
All other pins to GND	-0.3V to V_{VDD}+0.3V
Minimum load resistance R_L	3.2Ω(Note2)
Package Thermal Resistance θ_{JA}	107.2°C/W
Ambient Temperature Range	-40°C to +85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 3)	
HBM (Human Body Model)	±2000V
CDM (Charge Device Model)	±1500V
Latch-up	
Test Condition：JESD78F.02	+IT: 200mA
	-IT: 200mA

Note 1：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 2：*Only support Micro Speaker when the Load resistance RL is less than 5Ω;*

Note 3：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2024; (Zap 1 pulse,Interval: >=0.1S)*

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88083ACSR	-40℃～85℃	WLCSP 1.403mmX1.183 mm-12B	CPX	MSL1	ROHS+HF	4500 units/ Tape and Reel

Electrical Characteristics

Test condition: T_A=25°C, VDD=5V, Gain=14.3dB, R_L=8Ω+33μH, f_{wck}=48kHz, f=1kHz (unless otherwise noted)

Symbol	Description	Condition	MIN	TYP	MAX	Units
V_{VDD}	Supply Voltage Range	On pin VDD	2.5		5.5	V
I_{VDD}	Static VDD supply current	Operating mode; VDD=3.7V		1.8		mA
		Standby mode, EN=1.8V, VDD=5.0V, all I²S interface pins at 0V		7.2	9.65	μA
		Standby mode, EN=1.8V, VDD=5.0V, no toggling on I²S interface pins		10	15.55	μA
		EN = 0V, VDD=5V		0.15	0.5	μA
T_{on}	Turn on time	Time from standby to Operating at fast mode		1.0	1.5	ms
Class D						
Pout	RMS Output Power	VDD=3.7V, RL=4Ω+33μH				
		THD+N=1%		1.4		W
		THD+N=10%		1.75		W
		VDD=5.0V, RL=4Ω+33μH				
		THD+N=1%		2.5		W
		THD+N=10%		3.2		W
		VDD=3.7V, RL=8Ω+33μH				
		THD+N=1%		0.77		W
		THD+N=10%		0.93		W
		VDD=5.0V, RL=8Ω+33μH				
		THD+N=1%		1.4		W
		THD+N=10%		1.8		W
		THD+N=1%, RL=20Ω+33μH				
		VDD=3.7V		0.3		W
		VDD=5.0V		0.58		W
Vos	Output offset voltage	IIS signal input 0	-1		1	mV
f_{PWM}	PWM Switching Frequency	VDD = 2.5V to 5.5V	332.5	350	367.5	kHz
f_{ss}	Spread-Spectrum Bandwidth			±17.5		kHz

Symbol	Description	Condition	MIN	TYP	MAX	Units
η	Total Efficiency	THD+N=10%, RL=8Ω+33μH, VDD=5V		92		%
FR	Frequency Response		-0.2		0.3	dB
E_N	Output Noise	A-weighting		10		μV
THD+N	Total harmonic distortion plus noise	f=1kHz, Pout=0.7W, RL=8Ω		0.02		%
SNR	Signal-to-noise ratio	VDD=5V Po=0.29W, RL=40Ω		108		dB
DNR	Dynamic Range	-60dBFS Method, A-weighted		108		dB
PSRR	Power supply rejection ratio	F=217Hz, V_{ripple}=200mV		81		dB
		F=1kHz, V_{ripple}=200mV		81		dB
DAC DIGITAL FILTERS/ NONLINEAR FIR LOWPASS FILTER (LRCLK < 30kHz)						
f_{pass}	Passband	Ripple < δ_P	0.405*fs			Hz
		Droop < 3dB	0.449*fs			
f_{stop}	Stopband	Attenuation > δ_S			0.559*fs	Hz
δ_P	Passband Ripple	f < f_{Pass}, referenced to signal level at 1kHz	-0.05		+0.05	dB
δ_S	Stopband Attenuation	f > f_{stop}	74.6			dB
DAC DIGITAL FILTERS/ LINEAR FIR LOWPASS FILTER (LRCLK ≥ 30kHz)						
f_{pass}	Passband	Ripple < δ_p	0.405*fs			Hz
		Droop < 3dB	0.455*fs			
f_{stop}	Stopband	Attenuation > δ_S			0.589*fs	Hz
δ_p	Passband Ripple	f < f_{Pass}, referenced to signal level at 1kHz	-0.05		+0.05	dB
δ_S	Stopband Attenuation	f > f_{stop}	74.6			dB
DAC DIGITAL FILTERS/DIGITAL DC BLOCKING FILTER						
f_C	DC Blocking Filter -3dB Cutoff Frequency	Fs=96kHz		1.86		Hz
		Fs=48kHz		1.86		
		Fs=44.1kHz		1.71		
		Fs=8kHz		1.24		
V_{IL}	Logic input low voltage	BCK, WCK, DATAI			0.496	V
		EN			0.296	V
V_{IH}	Logic input high voltage	BCK, WCK, DATAI	0.883			V
		EN	0.909			V

Symbol	Description	Condition	MIN	TYP	MAX	Units
T_{SD}	Over Temperature Protection Threshold			150		℃
T_{SDR}	Over Temperature Protection Recovery Threshold			130		℃
UVP	Under Voltage Protection Threshold			2.1	2.3	V
UVP	Under Voltage Protection Hysteresis Threshold			100		mV
OCP	Output current Protection			2.8		A

DIGITAL AUDIO INTERFACE TIMING

I2C

Parameter			Fast mode			Fast mode Plus			UNIT
No.	Sym	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	KHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	the Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

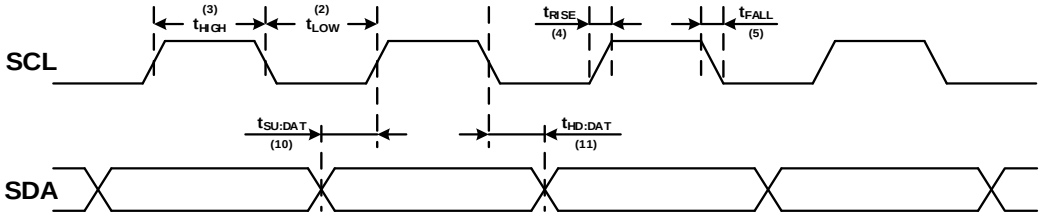


Figure 4 SCL and SDA timing relationships in the data transmission process

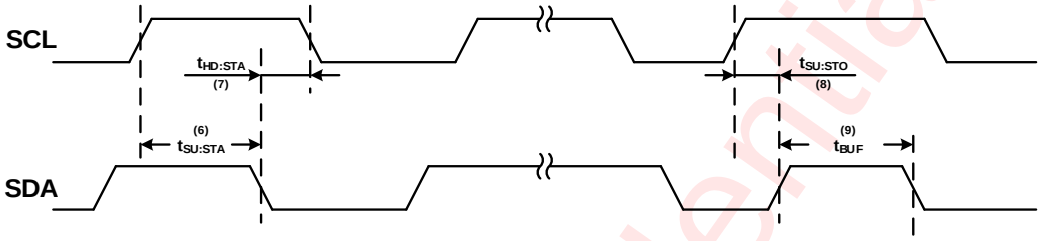


Figure 5 The timing relationship between START and STOP state

I²S

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8	-	96	kHz
f_{bck}	Bit clock frequency, on pin BCK	32*fs		25.804(Note1)	MHz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns

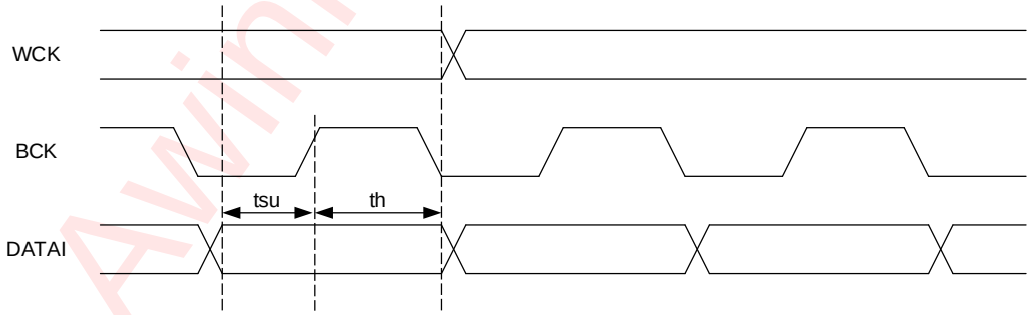
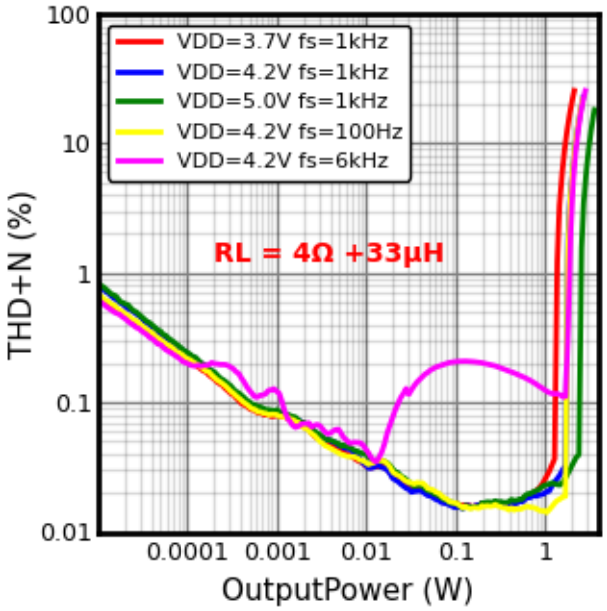


Figure 6 I²S Digital Audio Interface Timing

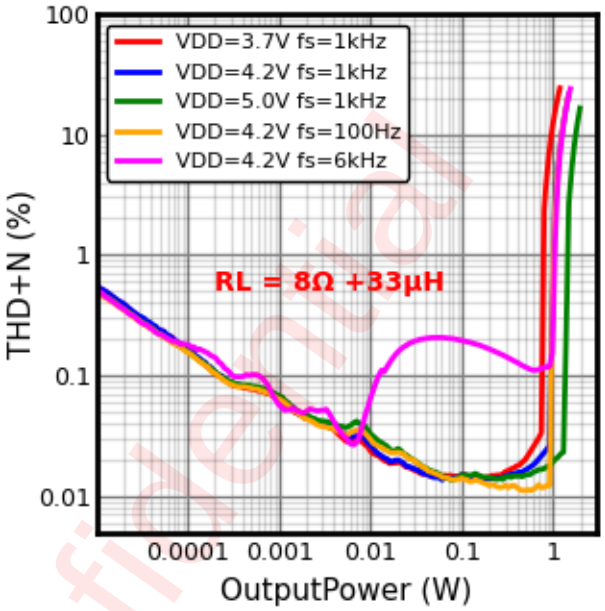
Note 1： *The BCK frequency f_{bck} is determined by sampling frequency, slot number and slot length, please make sure f_{bck} is less than 25.804MHz.*

TYPICAL CHARACTERISTIC CURVES

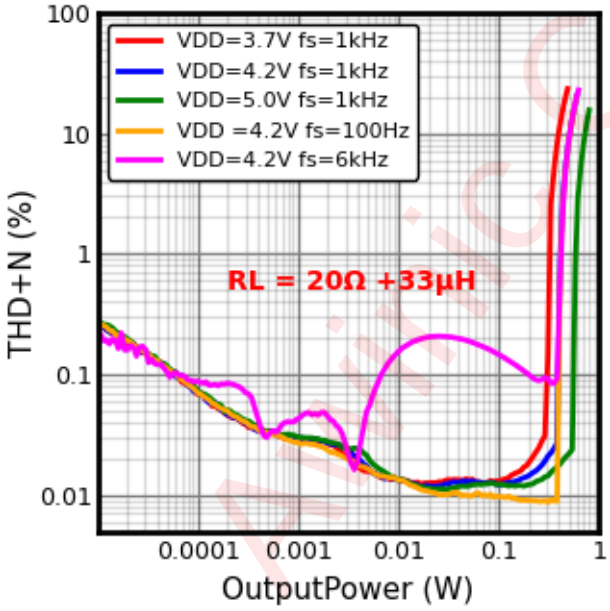
THD+N VS. OUTPUT POWER



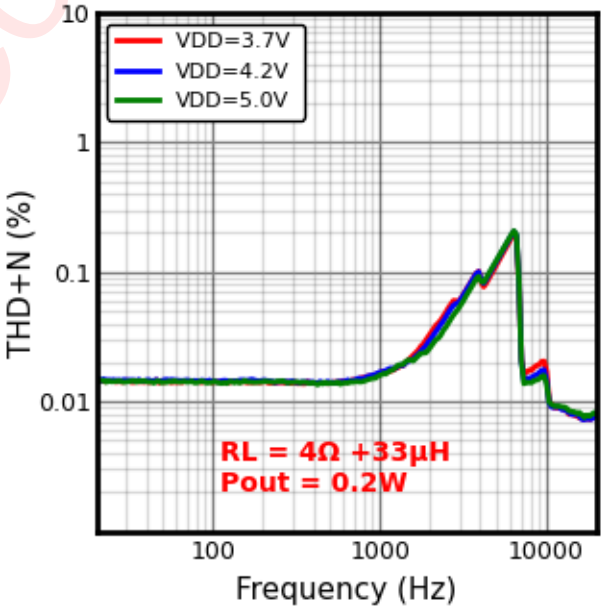
THD+N VS. OUTPUT POWER



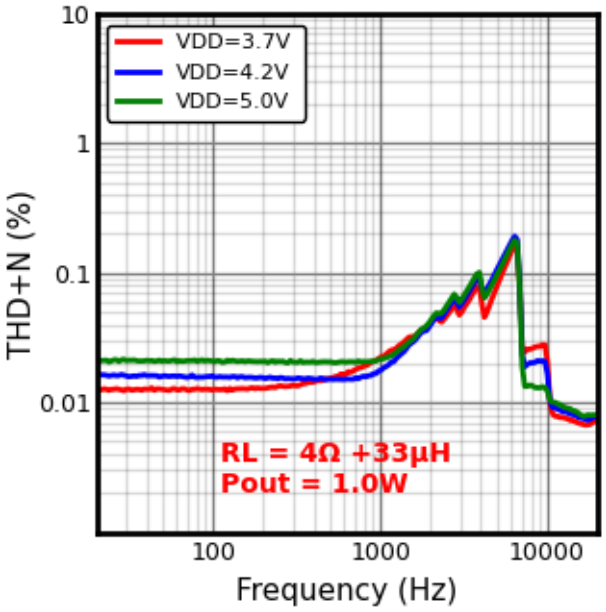
THD+N VS. OUTPUT POWER



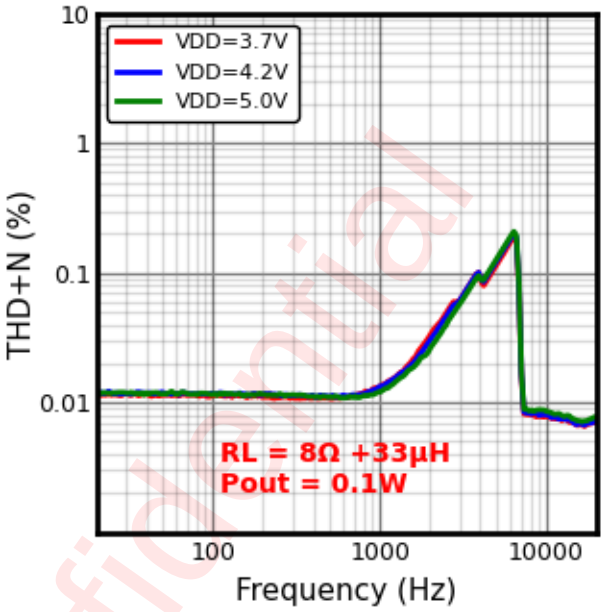
THD+N VS. FREQUENCY



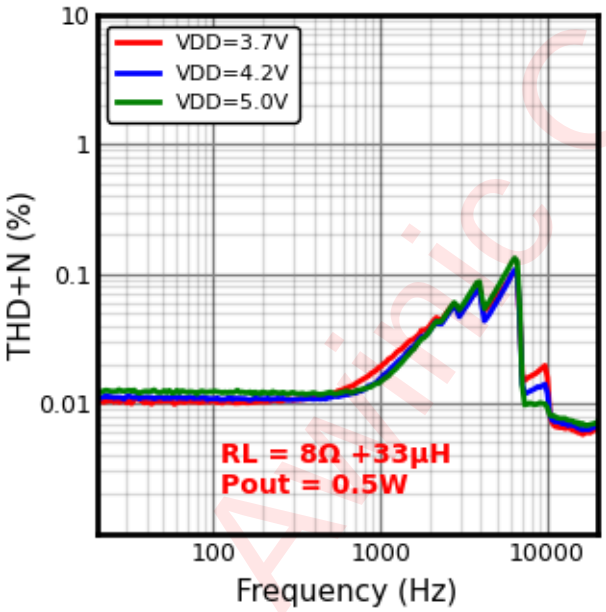
THD+N VS. FREQUENCY



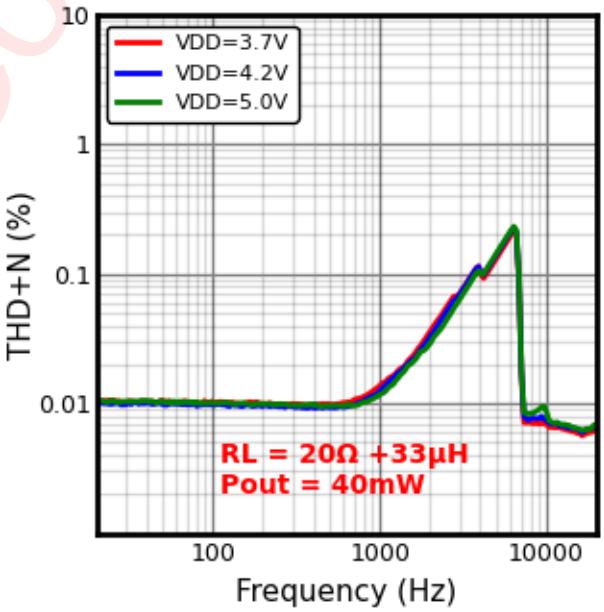
THD+N VS. FREQUENCY



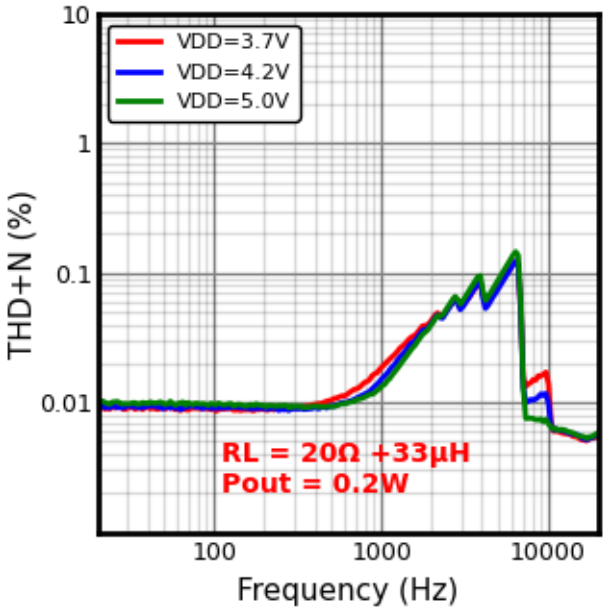
THD+N VS. FREQUENCY



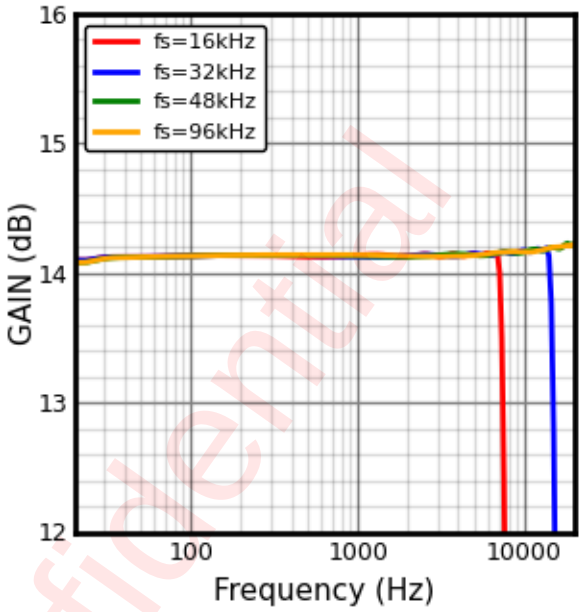
THD+N VS. FREQUENCY



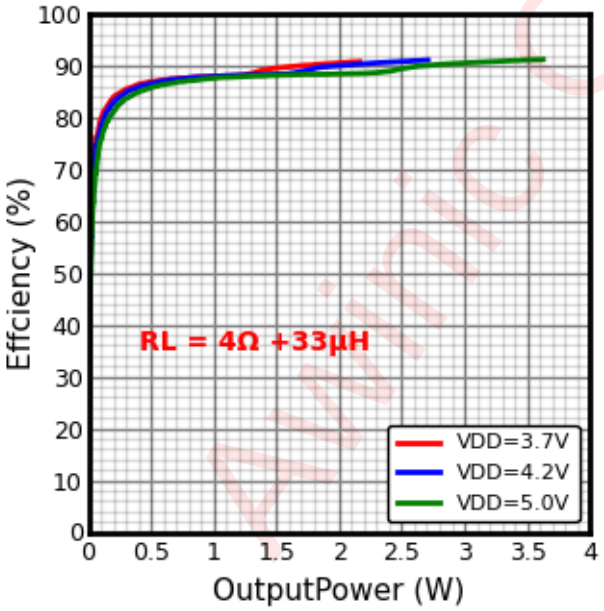
THD+N VS. FREQUENCY



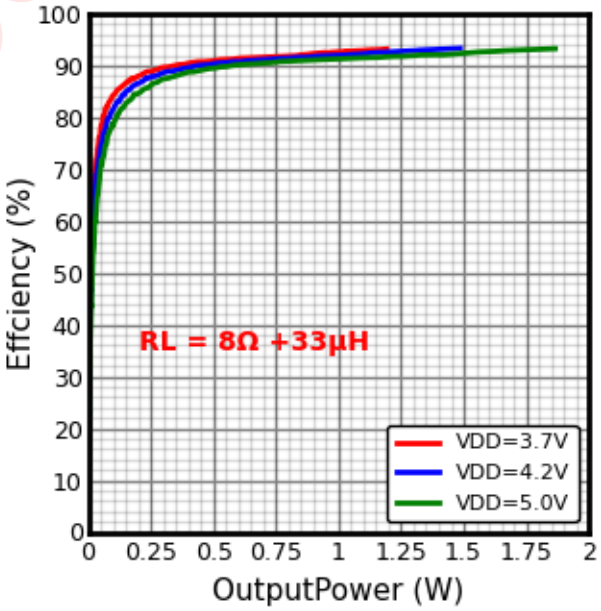
GAIN VS. FREQUENCY



EFF VS. OUTPUT POWER



EFF VS. OUTPUT POWER



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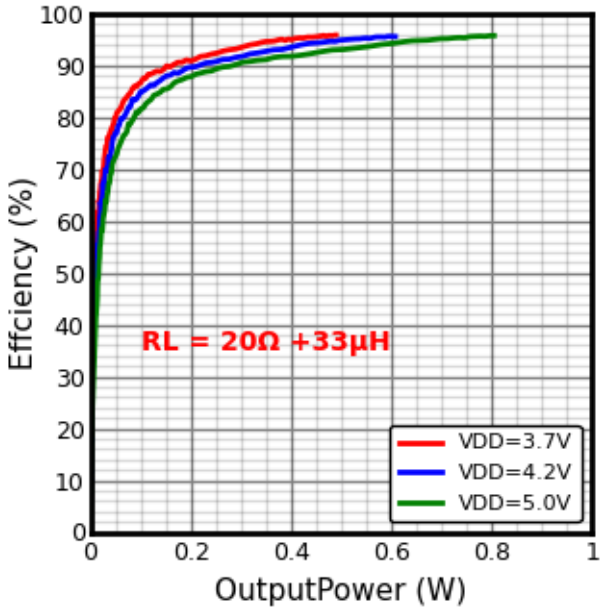
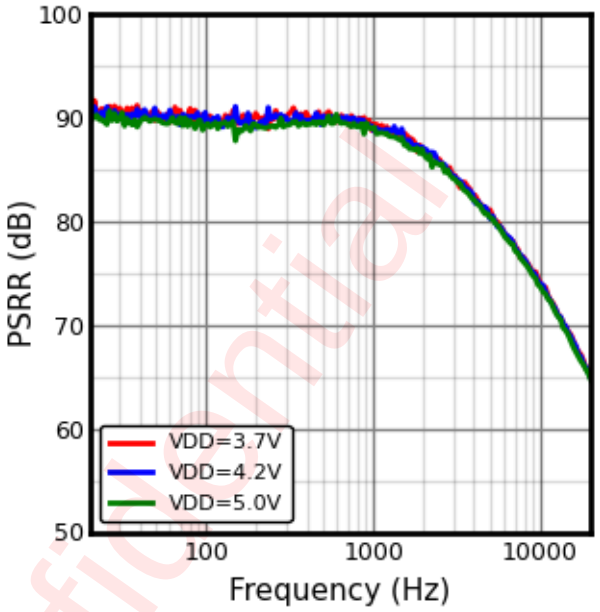
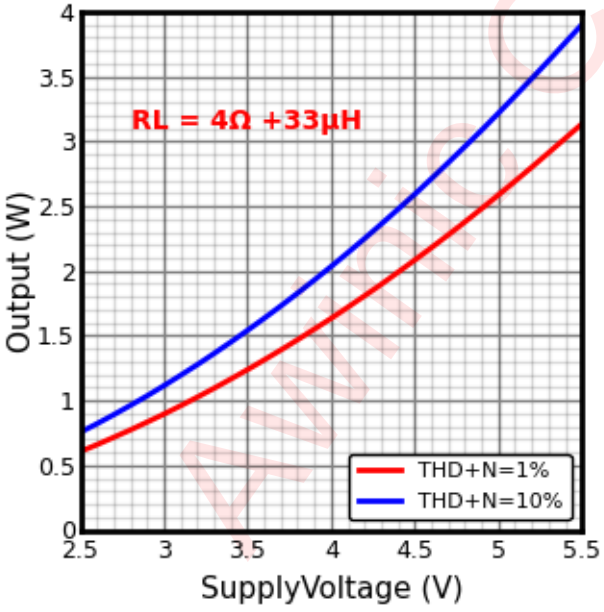


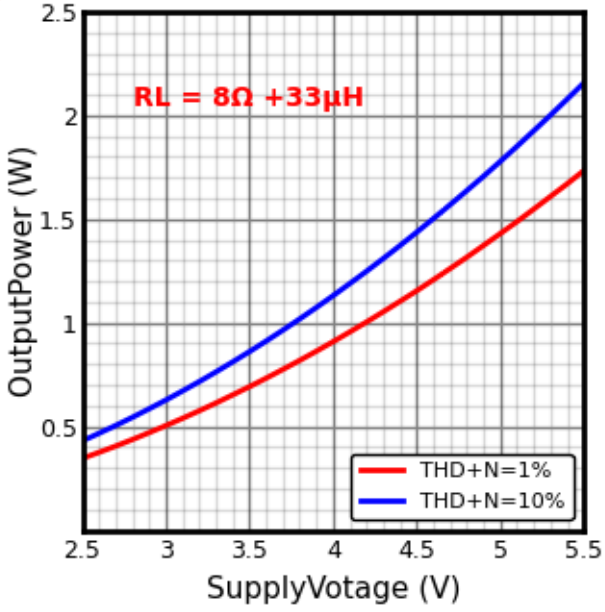
EFF VS. OUTPUT POWER



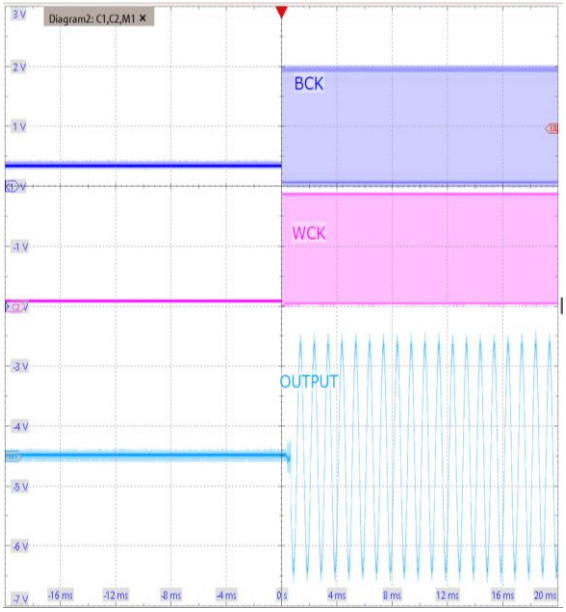
OUTPUT POWER VS. SUPPLY VOLTAGE



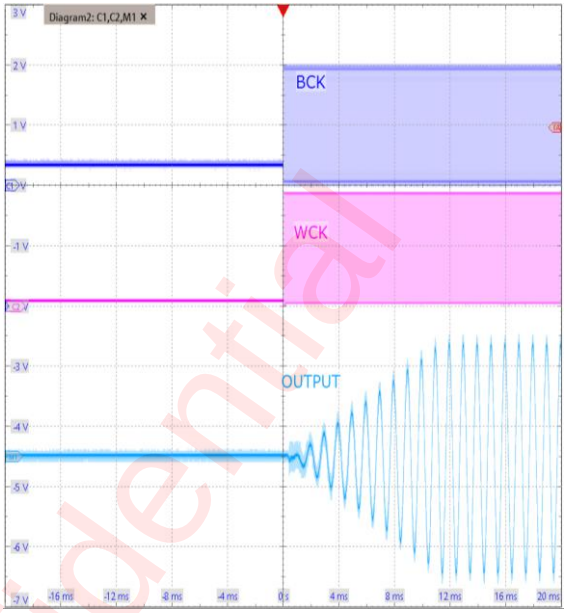
OUTPUT POWER VS. SUPPLY VOLTAGE



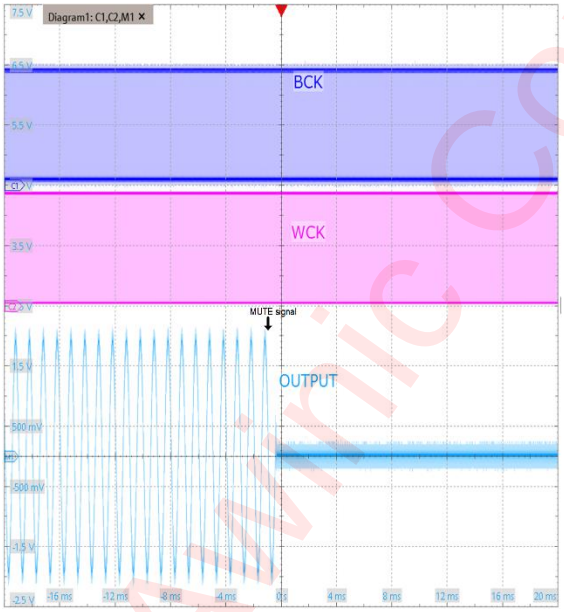
TURN-ON RESPONSE (FAST MODE)



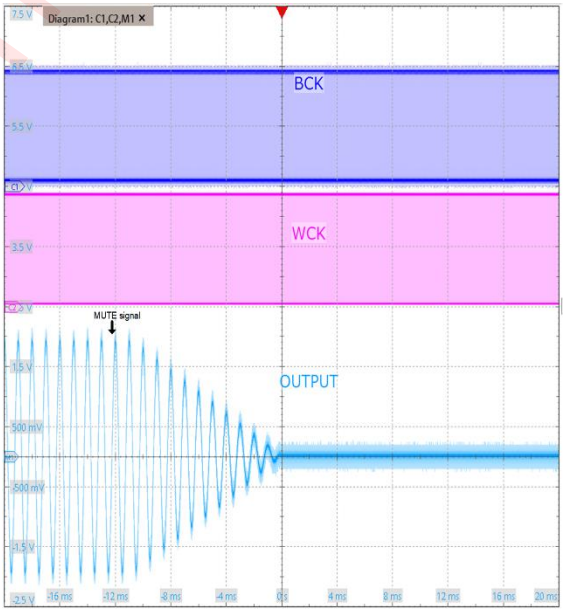
TURN-ON RESPONSE (RAMP MODE)



TURN-OFF RESPONSE (FAST MODE)



TURN-OFF RESPONSE (RAMP MODE) (Note 4)



Note **：** *This figure only shows the difference in output waveforms between Fast-mode and Ramp-mode. Please refer to the Operation Mode section of the Detailed Functional Description chapter for the timing of power on and off.*

DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDD supply voltage. When the VDD supply voltage raises from 0V to 1.8V. The internal reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{VDD} < 1.8V EN Low	Power supply is not ready, chipset is power down.
Stand-By	V_{VDD} > 2.3V EN High	Power supply is ready, most parts of the device are power down for low power consumption except I^2C interface
Configuring	PWDN = 0	Device is biased while boost and Class-D output is floating. System configuration carried out in this mode
Operating	AMPPD = 0	Amplifier is fully operating

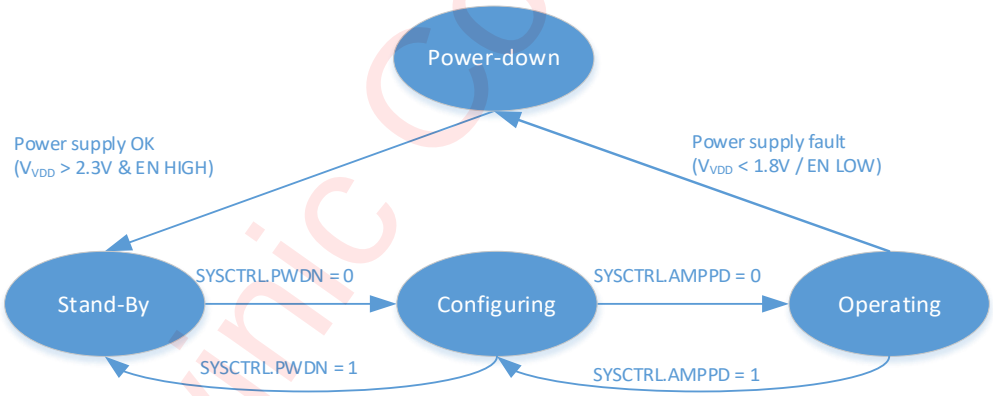


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{VDD} < 1.8 V
- EN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

V_{VDD} >2.3V and EN goes HIGH

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to Stand-By mode when the device is no needed to work.

CONFIG MODE

The device switches to Configuring mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD= 1;

In this mode the internal bias, OSC, PLL will start to work

OPERATING MODE

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.
This device power up sequence is illustrated in the following figure:

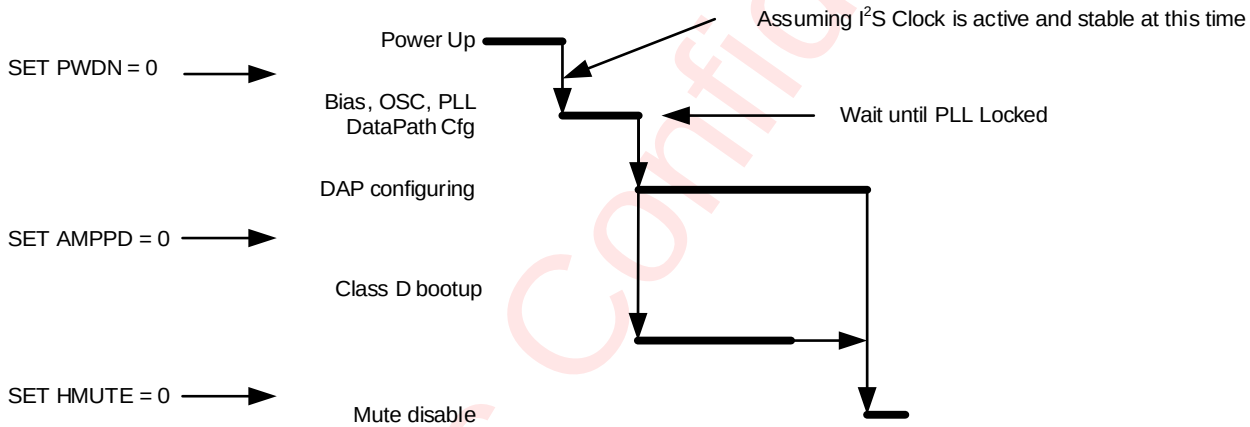


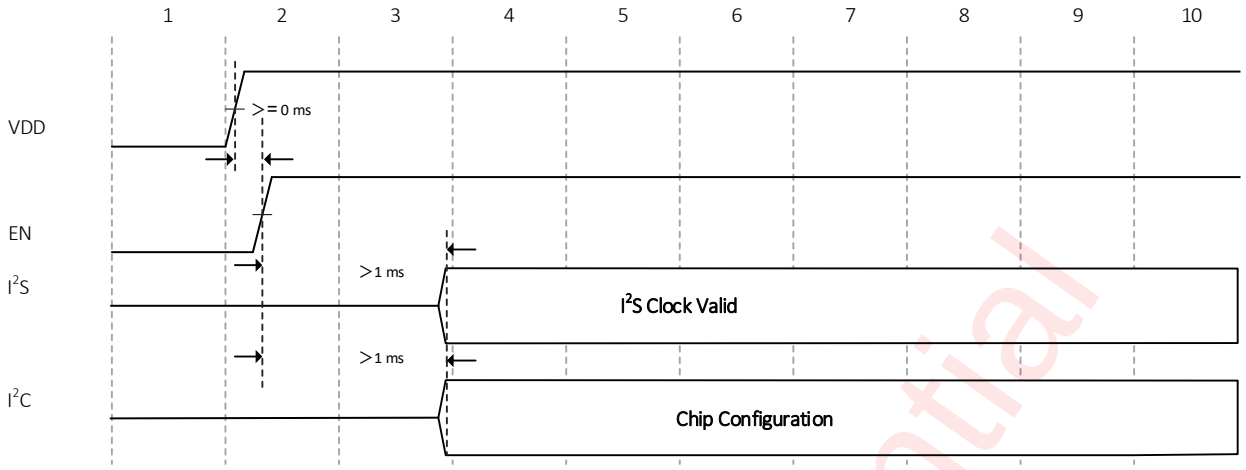
Figure 8 Power up sequence

Detail description for each step is listed in the following table.

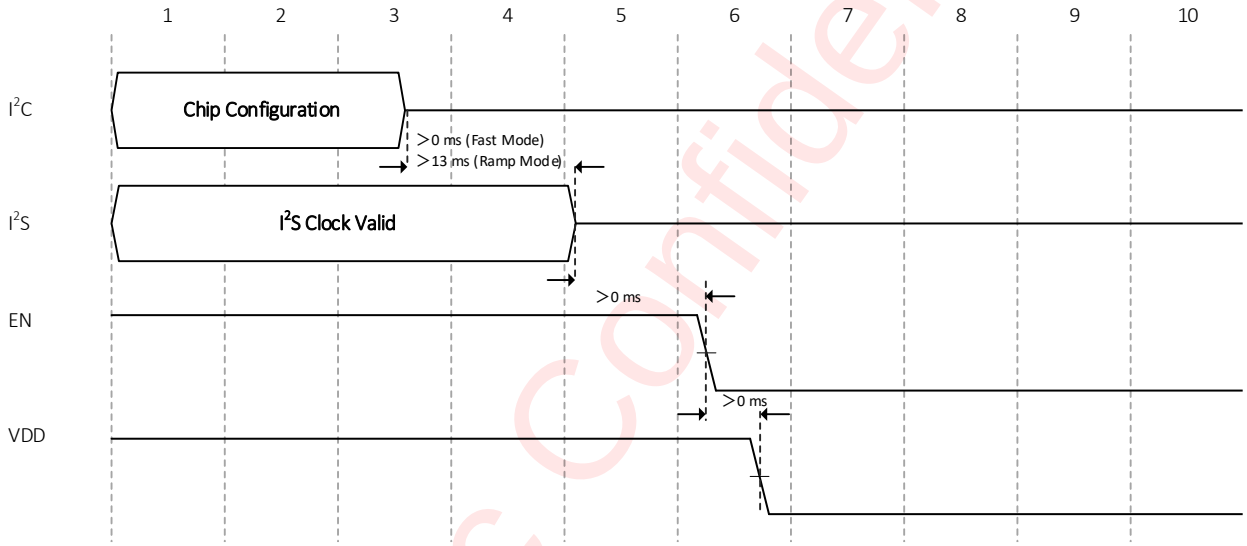
Table 2 Detail Description of Power up sequence

Index	description	Mode
1	Wait for VDD/EN supply power up	Power-Down
2	I²S + Data Path Configuration	Stand-By
3.1	Enable system (SYSCTRL.PWDN = 0)	Configuring
3.2	Active Bias, OSC and PLL	
3.3	Wait for PLL to be locked	
4.1	Enable amplifier (SYSCTRL.AMPPD = 0) Amplifier boot up	Operating
4.2	Wait for SYSST.SWS =1	
5	Release Hard-Mute Data Path active	

Power up sequence considering I²S, I²C timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL AUDIO INTERFACE

The state of each digital input and output are shown in below table. After power on, the input signal pin BCK, WCK, DATAI are set to high impedance by default.

Table 3 Detail Description of Digital I/O

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
TEST	Output	Hi-Z
AD	Input	Weak pull down
BCK	Input	Hi-Z

Digital I/O	Type	Description (Default State)
WCK	Input	Hi-Z
DATAI	Input	Hi-Z

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 3 dedicated pins:

- BCK
- WCK
- DATAI

Two-slot I²S and 1/2/4/6/8-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL2.I2SBCK. The frequency of BCK can be calculated according to the following equation:

BCK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 4-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL.

Table 4 Supported I²S interface parameters

Interface format(MSB first)	Data width	BCK frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs /64fs
left-justified	16b/20b/24b/32b	32fs/48fs /64fs
right-justified	16b/20b/24b/32b	32fs /48fs /64fs

STANDARD I²S MODE

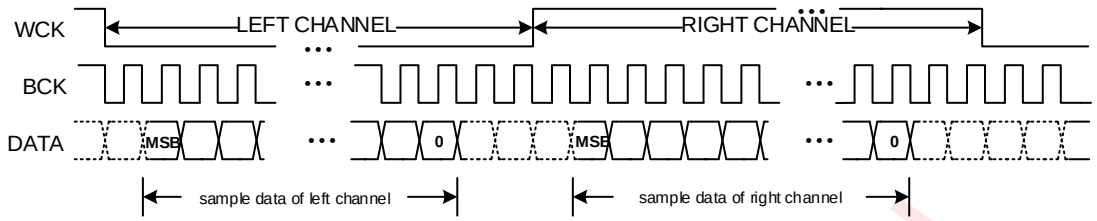


Figure 9 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

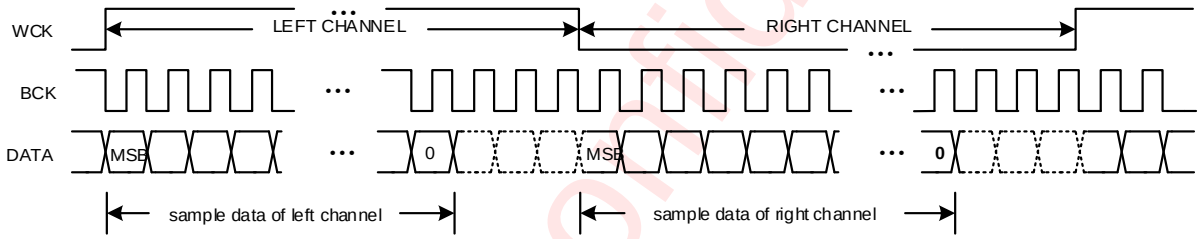


Figure 10 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

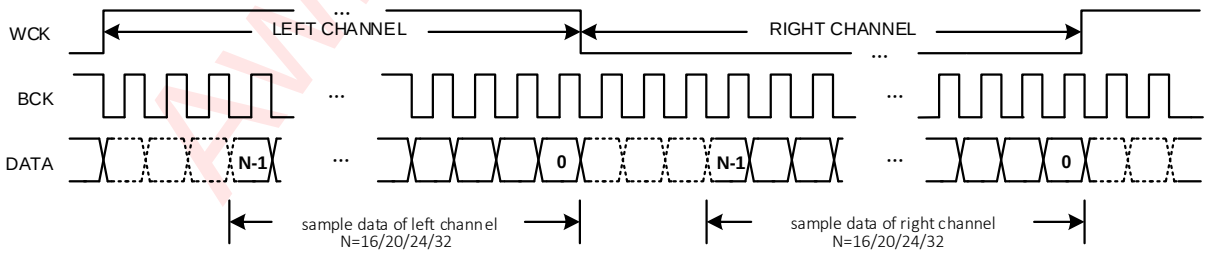


Figure 11 I²S Timing for Right-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock

preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 4-slot is supported in TDM mode, while 2-slot is supported in I²S mode

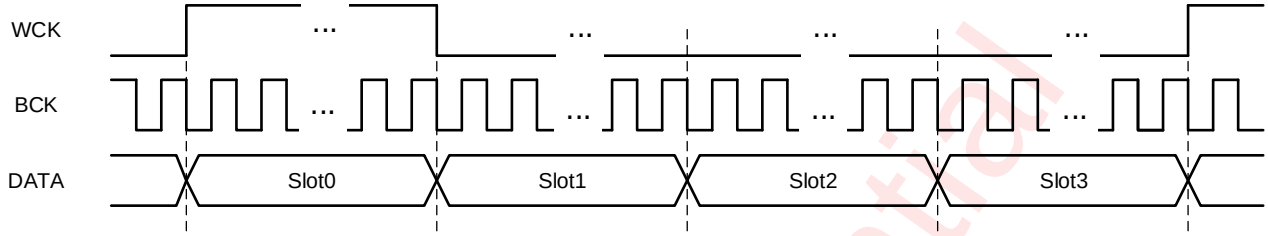


Figure 12 TDM Timing

Note: The high-level pulse width of WCK signal can be one slot time or one period of BCK.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the DAP (Digital Audio Processor) is illustrated in the following figure.

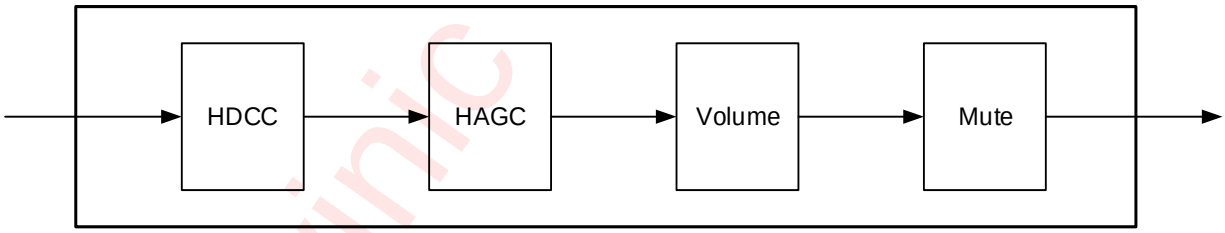


Figure 13 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker, such as in the 5V power supply, as for 4Ω speaker, the maximum undistorted power is about 3.0W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier

with hardware AGC can protect the speaker effectively, When the output power is not exceeding the setting threshold, the hardware AGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the hardware AGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -96.162db with 0.094db/step

MUTE

This module performs mute control for the audio stream. It supports Fast/Ramp modes:

- Fast Mode, device have 1ms turn-on time with mute immediately.
- Ramp Mode, device have 13ms turn-on time for best click-and-pop performance.

Fast/Ramp modes can be selected through register I2SCTRL3.SOFT_MUTE.

PROTECTION MECHANISMS

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to VDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 1 MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.2V~1.8V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

Table 5 Address Selection

AD	Address(7-bit)
Connect to GND	0x34
Connect to High	0x35
Connect to SCL	0x36
Connect to SDA	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

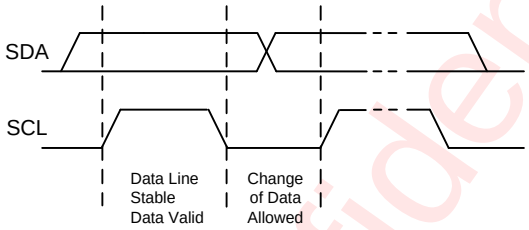


Figure 14 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

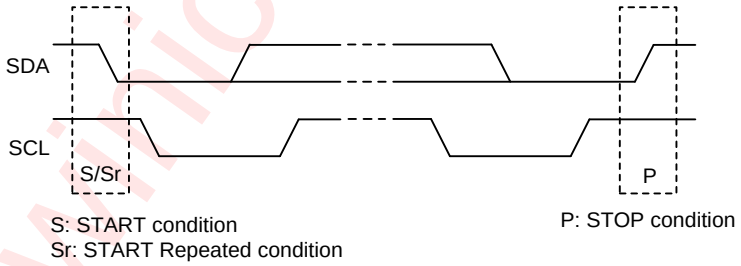


Figure 15 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

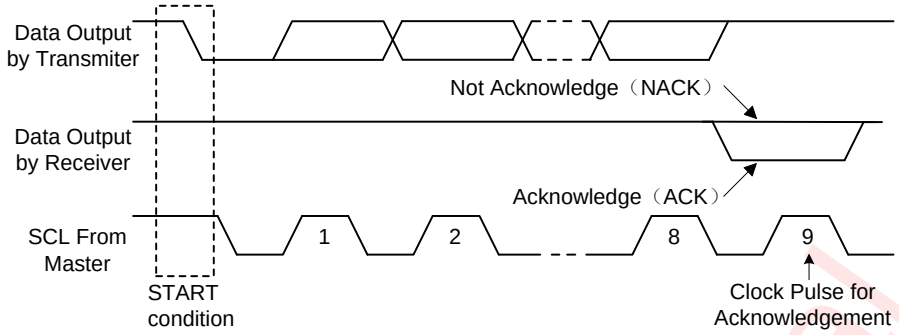


Figure 16 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends high data byte of 16-bit data to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends low data byte of 16-bit data to be written to the addressed register

i) Slave sends acknowledge signal

j) If master will send further 16-bit data bytes, the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)

k) Master generates STOP condition to indicate write cycle end

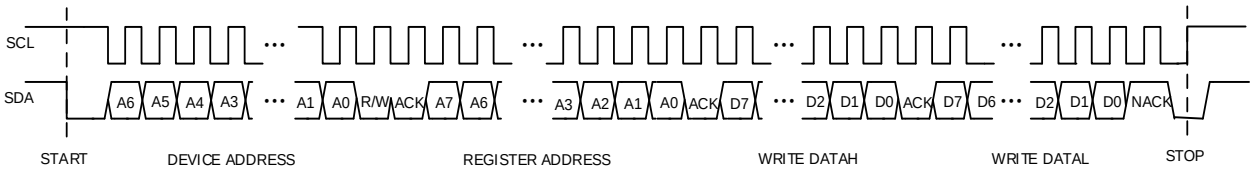


Figure 17 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

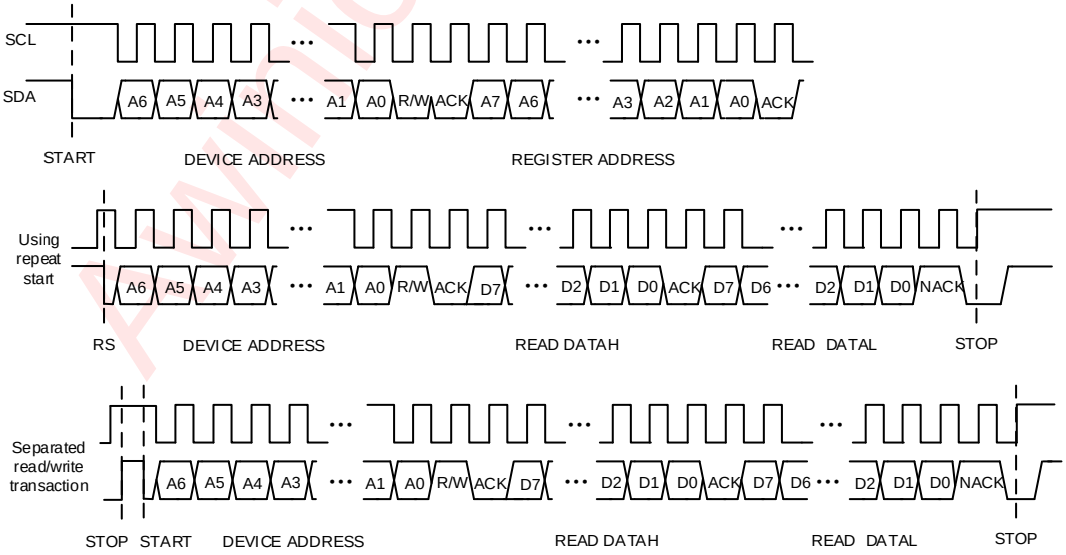


Figure 18 I²C Read Byte Cycle

REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	RO	IDCODE																0x2407
0x01	SYSST	RO		UVLS						SWS			NOCLKS	CLKS	OCDS		OTHS	PLLS	0x0000
0x02	SYSINT	RC		UVLI						SWI			NOCLKI	CLKI	OCDI		OTHI	PLLI	0x0000
0x03	SYSINTM	RW		UVLM						SWM			NOCLKM	CLKM	OCDM		OTHM	PLLM	0x4138
0x04	SYSCTRL	RW	I2C_WEN		I2SRXEN	INTERP_TYPE	RMSE	HAGCE	HDCCE	HMUTE		I2SEN	WSINV	BCKINV	IPLL	PLL_PD	AMPPD	PWDN	0x23C7
0x05	SYSCTRL2	RW	EN_MPD	GAIN_SET			CHSEL		VOL										0Xc402
0x06	I2SCTRL1	RW	FSYNC_TYPE	SLOT_NUM			I2S_RXL_SLOTVLD				I2SFS		I2SMD		I2SSR				0xB0C8
0x07	I2SCTRL2	RW	ULS_HMUTE	ULS_MODE		I2SBCK							I2S_RXL_SLOTVLD						0x1F01
0x08	I2SCTRL3	RW	I2SSHIFTS										INPLEV		SOFT_MUTE				0x0014
0x09	DACCFG1	RW	RVTH								AVTH								0x5E6A
0x0A	DACCFG2	RW	ATTH																0x000F
0x0B	DACCFG3	RW	RTTH																0x01E0
0x0C	DACCFG4	RW									HOLDTH								0x1C1E

DETAILED REGISTER DESCRIPTION

ID: (Address 00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	IDCODE	RO	Chip ID will be returned after read. All configuration registers will be reset to default value after 0x55aa is written	0x2407

SYSST: (Address 01h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RO	Not used	0
14	UVLS	RO	VDD under UVLO threshold voltage indicator 0: Normal 1: UVLO	0
13:9	Reserved	RO	Not used	0
8	SWS	RO	Amplifier switching status. 0: Not switching 1: Switching	0
7:6	Reserved	RO	Not used	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0
4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCDS	RO	Over current status in amplifier 0: Normal 1: OC	0
2	Reserved	RO	Not used	0
1	OTHS	RO	Die Temperature is higher than 160degrees 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RC	Not used	0
14	UVLI	RC	Interrupt indicator for Power on and VDD UVLS	0
13:9	Reserved	RC	Not used	0
8	SWI	RC	Interrupt indicator for SWS.	0
7:6	Reserved	RC	Not used	0
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCDI	RC	Interrupt indicator for OCDS	0
2	Reserved	RC	Not used	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

SYSINTM: (Address 03h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	Reserved	RW	Not used	0
14	UVLM	RW	Interrupt mask for UVLI.	1
13:9	Reserved	RW	Not used	0
8	SWM	RW	Interrupt indicator for SWI.	1
7:6	Reserved	RW	Not used	0
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCDM	RW	Interrupt mask for OCDI.	1
2	Reserved	RW	Not used	0
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

SYSCTRL: (Address 04h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:14	I2C_WEN	RW	I2C write enable 10: enable others: disable	0
13	I2SRXEN	RW	Disable/Enable I2S receiver module 0: disable 1: enable	1
12	INTERP_TYPE	RW	DAC interpolator type 1'b0： liner phase 1'b1： nonliner phase	0
11	RMSE	RW	Hardware HAGC mode selection 0: Peak AGC 1: RMS AGC	0
10	HAGCE	RW	Disable/Enable Hardware AGC 0: disable 1: enable	0
9	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: disable 1: enable	1
8	HMUTE	RW	Disable/Enable Hardware mute module 0: disable 1: enable	1
7	Reserved	RW	Not used	1
6	I2SEN	RW	Disable/Enable whole I2S interface module 0: disable 1: enable	1
5	WSINV	RW	I2S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I2S bit clock invert control 0: Not invert 1: Inverted	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: No used	0

2	PLL_PD	RW	PLL power down: 0: power up 1: power down	1
1	AMPPD	RW	Amplifier power down control bit, PowerDown until system configuration finished 0: Working 1: Power Down	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	1

SYSCTRL2: (Address 05h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	EN_MPD	RW	Disable/Enable MPD multi stage power mode, Gain will be automatically adjusted only when SPK_GAIN > 10. It can enable the small-signal detection or not, based on the audio input, so that the quiescent current could be reduced and the noise level will be smaller. 0: disable 1: enable	1
14:12	GAIN_SET	RW	Class-D Gain Set： 000：-0.7dB 001：5.3dB 010：8.3dB 011：11.3dB 100：14.3dB(default) 101：17.3dB 110：20.3dB 111：23.3dB	4
11:10	CHSEL	RW	Left/right channel selection for I2S input 00: Reserved 01: Left 10: Right 11: Mono	1
9:0	VOL	RW	Volume control, from 0 to -96dB, in unit of -6.02/64dB	2

I2SCTRL1: (Address 06h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-BCK	1
14:12	SLOT_NUM	RW	I2S TDM mode control (support max to 16 slots). 000: I2S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: TDM16s	3

11:8	I2S_RXL_SLOTVLD	RW	RX left channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 …… 1111: Slot 15	0
7:6	I2SFS	RW	I2S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	3
5:4	I2SMD	RW	I2S interface mode selection00: Philip Standard01: MSB justified10: LSB justified11: Reserved	0
3:0	I2SSR	RW	I2S interface sample rate configuration 0000: 8 kHz 0001: 11 kHz 0010: 12 kHz 0011: 16 kHz 0100: 22 kHz 0101: 24 kHz 0110: 32 kHz 0111: 44 kHz 1000: 48 kHz 1001: 88 kHz 1010: 96 kHz 1011: 192 kHz 1100: Auto_detect Others: Reserved	8

I2SCTRL2: (Address 07h)

Bit	Symbol	R/W	Description	Default
15	ULS_HMUTE	RW	Only when HMUTE&ULS_HMUTE=1, ultrasound can be muted 0: disable 1: enable	0
14	ULS_MODE	RW	Ultrasonic mode control 0: Legacy 1: TDM	0
13	Reserved	RW	Not used	0
12:8	I2SBCK	RW	I2S BCK mode 0: 2*fs 1: 4*fs 2: 6*fs 3: 8*fs …… 31: 64*fs	31
7:4	Reserved	RW	Not used	0
3:0	I2S_RXR_SLOTVLD	RW	RX right channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3	1

			0100: Slot 4 0101: Slot 5 0110: Slot 6 …… 1111: Slot 15	

I2SCTRL3: (Address 08h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:11	I2SSHIFTS	RW	The bit width of shift from WCK edge	0
10:6	Reserved	RW	Not used	0
5	INPLEV	RW	Input level selection bit, IIS input signal will be attenuated by -6dB at first when this register is set to 1. 0: Not attenuated 1: Attenuated	0
4	Reserved	RW	Not used	1
3	SOFT_MUTE	RW	Soft mute enables 0: disable 1: enable	0
2:0	Reserved	RW	Not used	0x04

DACCFG1: (Address 09h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale	0x5E
7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC): P0= ((i/256*((GAIN_SET+3)/20)) **2)/RLoad/2 RMSE = 1 (RMS AGC): P0= ((i/256*((GAIN_SET+3)/20)) **2)/RLoad i is the register value, default 0x6a GAIN_SET is the Amplifier Gain configured by SYSCTRL2 RLoad is 8ohm/4ohm for different application, default 4 ohm	0x6a

DACCFG2: (Address 0Ah)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8us	0x000F

DACCFG3: (Address 0Bh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x01E0

DACCFG4: (Address 0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:8	Reserved	RW	Not used	0x1C
7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	0x1E

APPLICATION INFORMATION

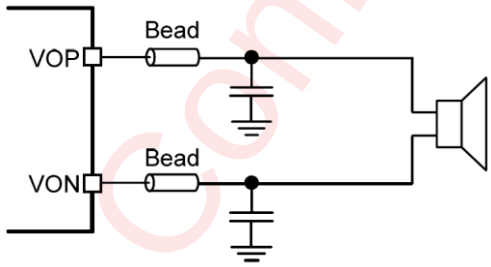
EXTERNAL COMPONENTS

SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A 0.1μF low equivalent-series-resistance (ESR) ceramic capacitor are recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the DEVICE is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1μF ceramic capacitor, place a 10μF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 10V.

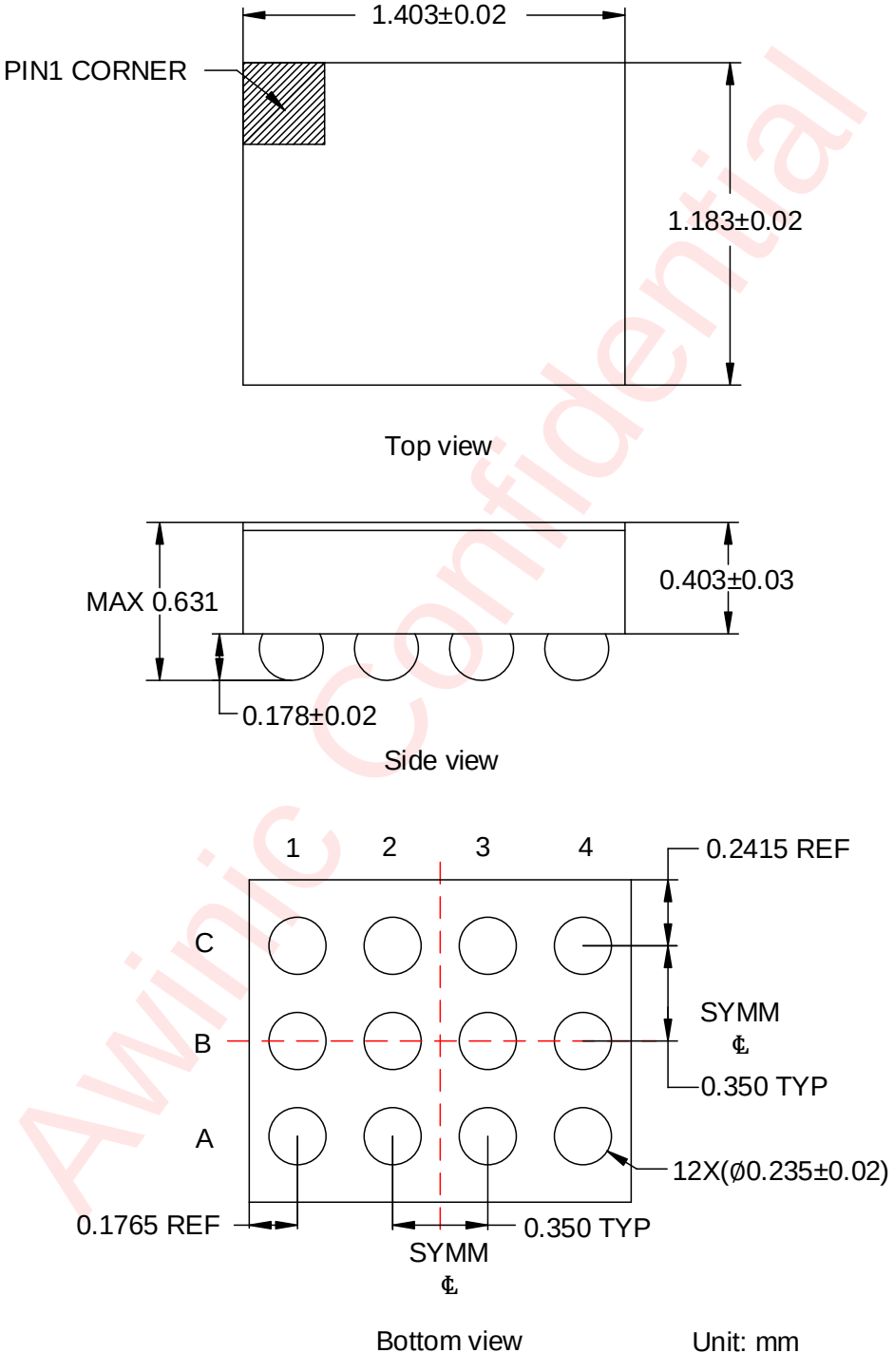


LAYOUT CONSIDERATION

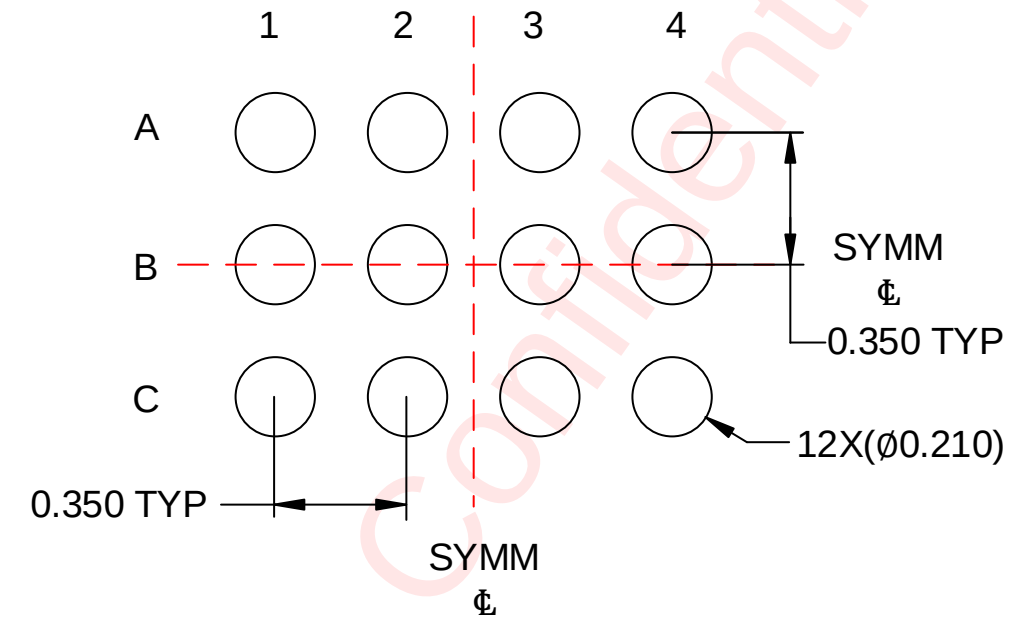
In order to obtain excellent performance of the amplifier, the below PCB layout guidelines should be followed:

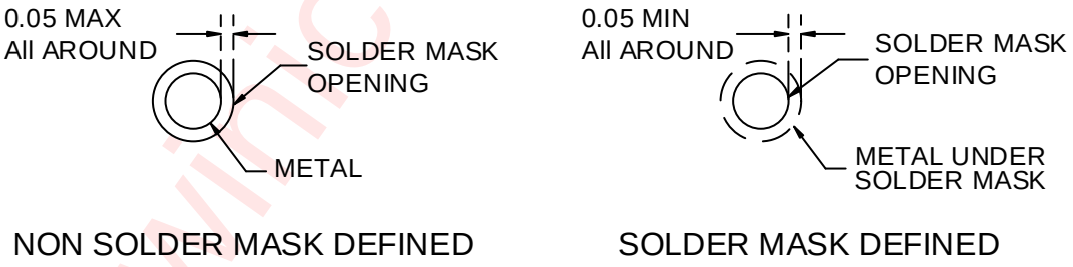
1. The filter capacitors of VDD should be placed close to the corresponding pins of the amplifier, and the small high -frequency filter capacitors are closer to the pins than the large.
2. VDD input of the audio power amplifier must first pass through the capacitor and then go to the pins of the chip, and the line width requirements can meet the maximum current required for the current set power output, so it is necessary to pay attention to the line width and the number of vias when routing the wire, so as to avoid the insufficient number of line width and vias, which will cause the voltage drop on the line to be too large and affect the final output of the audio power amplifier;
3. The signal line using the differential connection method is completely treated as equal length and width according to the requirements of the differential line, which not only requires the equal length and width between the signal lines, but also requires the distance between the signal line and the ground on both sides to be of equal width.
4. The beads and capacitor should be placed close to the VON and VOP pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.
5. The capacitance on the output lines or on the long speaker tracks should be less than 1nF.

PACKAGE DESCRIPTION



LAND PATTERN DATA





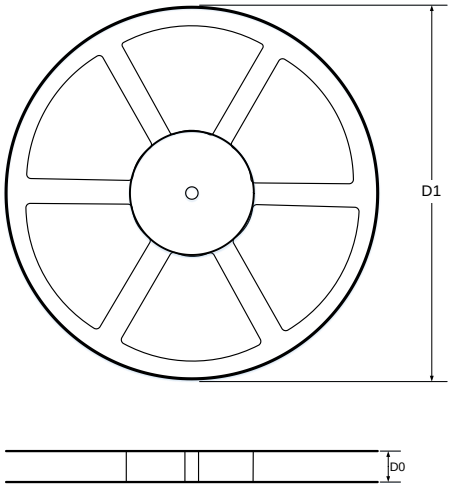
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

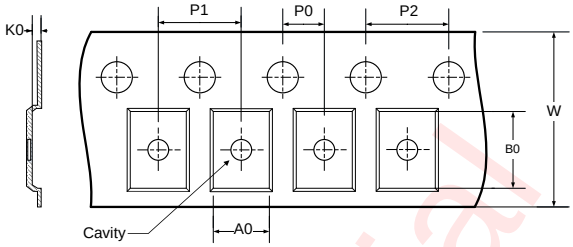
Unit: mm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

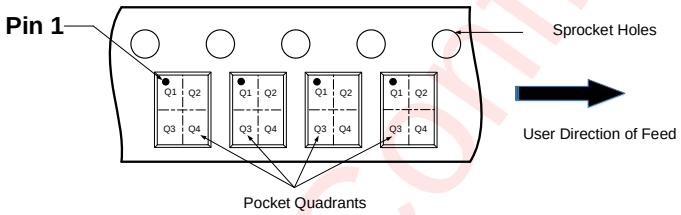


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.55	1.35	0.75	2	4	4	8	Q1

All dimensions are nominal

REVISION HISTORY

Version	Date	Change Record
V1.0	Jan. 2026	Officially released

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