AW89403 Quad-Channel High Performance Low-latency Audio ADC

Features

- **Multichannel high-performance ADC:**
  - 4 channel analog microphones or line-in
  - 4 channel digital PDM microphones
- **ADC line and microphone differential input Performance**
  - 103 dB signal to noise ratio, SUM OFF
  - 103 dB dynamic range, SUM OFF
  - -95 dB THD+N Ratio
- **ADC channel sum-mixer mode, DR performance**
  - 105dB SUM ON,2-channels summing
  - 108dB SUM ON,4-channels summing
- **ADC input voltage**
  - Differential, 2-VRMS full-scale inputs
  - Single-ended, 1-VRMS full-scale inputs
- **Programmable channel settings:**
  - Channel gain: -6 dB to 36 dB,1 dB/step
  - Digital volume control: -96dB to 30dB, 0.094dB/step
  - Phase calibration with 163 ns resolution
- **Programmable microphone bias**
- **Low-latency signal processing filter selection**
  - ADC linear-phase data-path group delay 240us(@fs=48kHz)
  - ADC low-latency data-path group delay 120us(@fs=48kHz)
- **Programmable high pass filter (HPF)**
- **Automatic gain controller (AGC)**
- **I2C-bus control interface**
- **Integrated high-performance audio PLL**
- **I2S/TDM interface (Advanced)**
  - I2S, Left-Justified and Right-Justified
  - Supports 1/2/4/6/8/16 slots TDM
  - Supports 8 to 768kHz sample rates
  - Data Width: 8~32 Bits
  - Master or slave interface
- **Power Supplies**
  - VDDA、VDDM: 3.3V
  - VDDIO: 3.3 V or 1.8 V
- **WBQFN 4X4-32L (Height 0.75) Package**

General Description

The AW89403 is a high performance, low power 4-channel audio analog-to-digital converter (ADC) for microphone array application.

The device supports line and microphone inputs. The device integrates four PGAs for quad differential inputs, MIC1P & MIC1N, MIC2P & MIC 2N, MIC3P & MIC3N and MIC4P & MIC4N. The device supports simultaneous sampling of up to four analog channels or four digital channels for the pulse density modulation (PDM) microphone input.

The device integrates programable channel gain, digital volume control, a programmable microphone bias voltage, a phase-locked loop (PLL), a programmable high-pass filter (HPF), low-latency filter mode, sum-mixer mode and allows for sample rates up to 768 kHz.

The device supports time-division multiplexing (TDM), I2S, or left-justified (LJ) audio formats, and can be controlled with the I2C interface

The device is very suitable for music and voice application, such as Microphone Array, Far field voice capture, Smart speaker, Conference system, Sound bar, Audio Interface, etc.

AW89403 is available in a WBQFN 4X4-32L (Height 0.75) Package.

Applications

- Microphone array systems
- Smart Speaker
- Far field voice capture
- Conference system

Functional Block Diagram

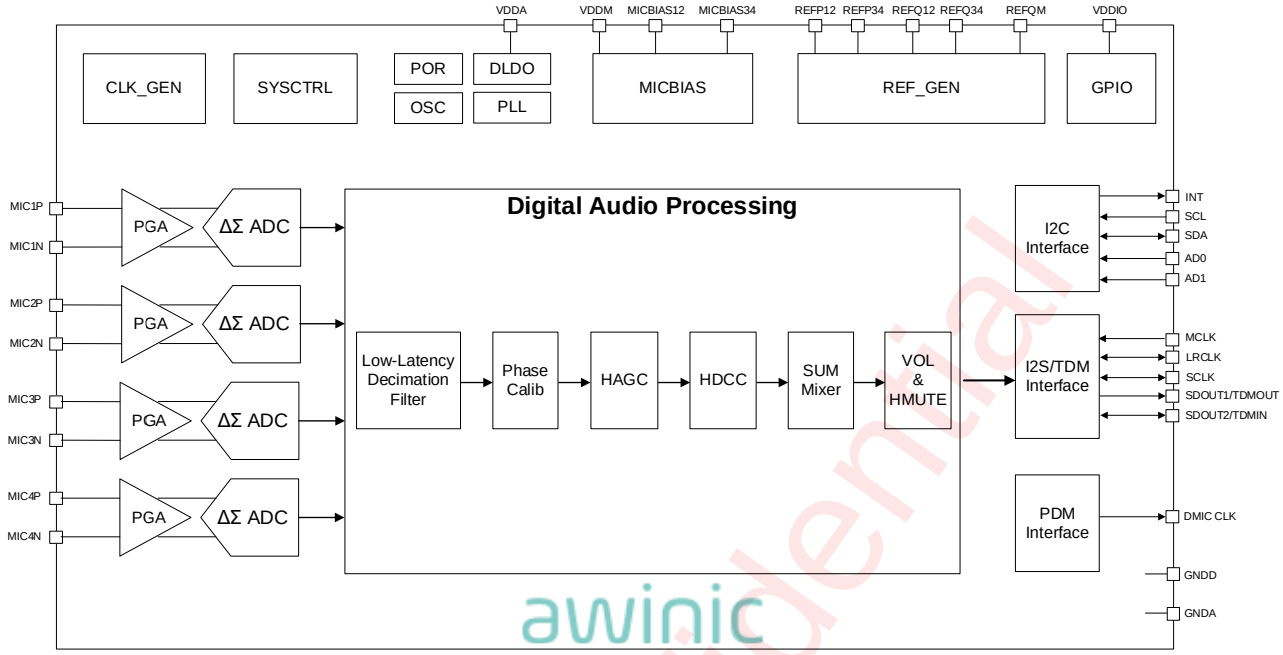
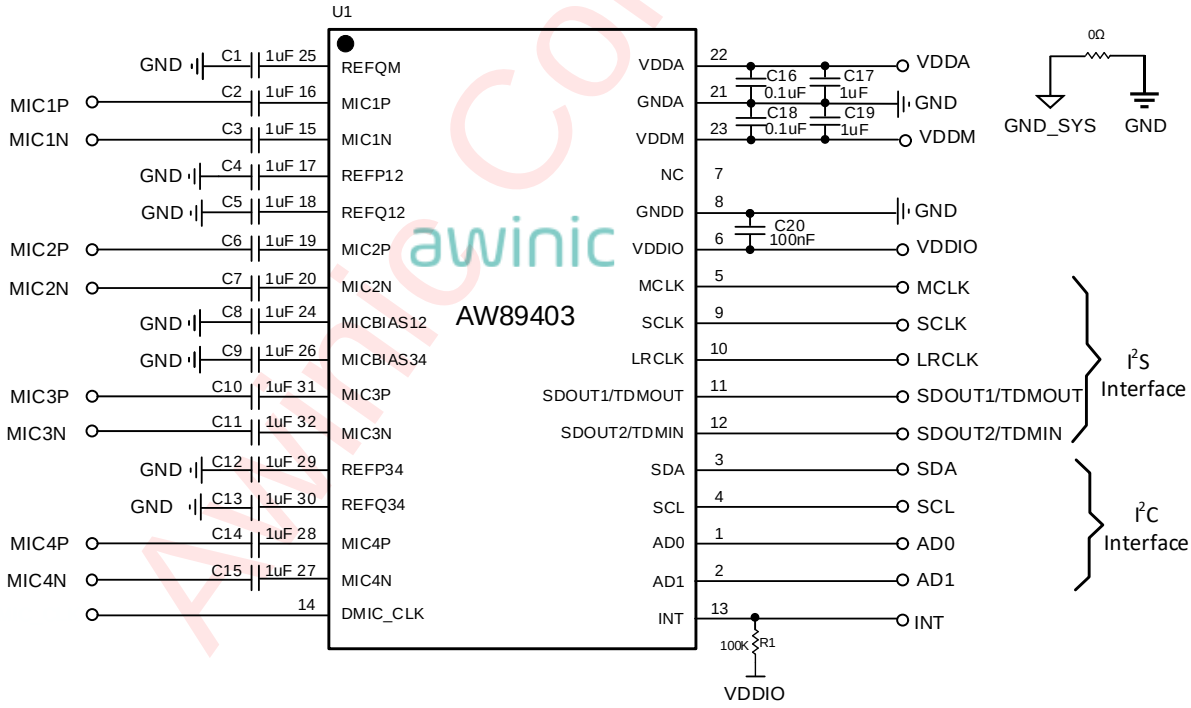


Figure 1 AW89403 Functional Diagram

Typical Application Circuit



Notes: Thermal pad at the bottom of the chip must be grounded

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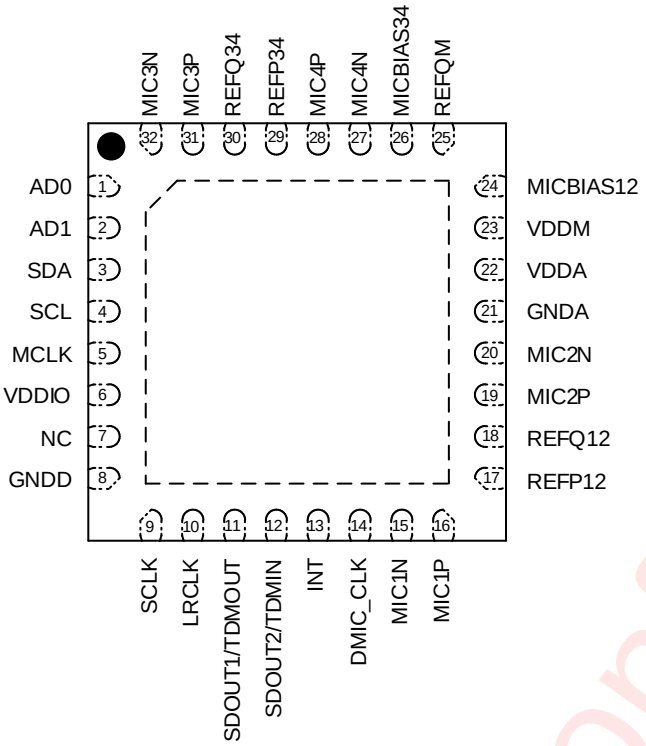
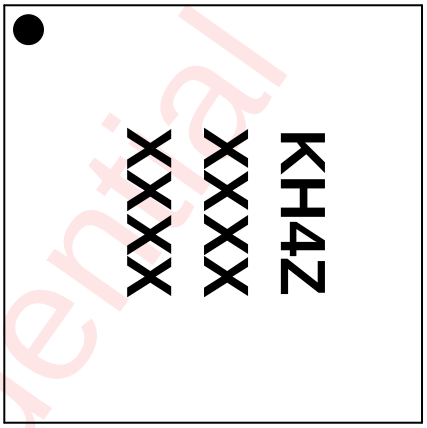
Figure 2 AW89403 Application Circuit

Pin Configuration and Top Mark

AW89403QNR
(Top View)



AW89403QNR Marking
(Top View)



KH4Z – AW89403QNR
XXXX/XXXX - Production Tracing Code

Figure 3 AW89403 pin diagram top view and device marking

Pin Description

Pin No	Pin Name	Description
1	AD0	I2C address bit0
2	AD1	I2C address bit1
3	SDA	I2C serial control data interface input/output
4	SCL	I2C serial control clock input
5	MCLK	I2S master clock
6	VDDIO	Digital IO power
7	NC	Not connected, can be connected to GNDD, GNDA or VDDIO
8	GNDD	Digital ground
9	SCLK	I2S/TDM bit clock input
10	LRCLK	I2S word select input / TDM frame sync signal
11	SDOUT1/TDMOUT	I2S data/TDM output
12	SDOUT2/TDMIN	I2S data/TDM input
13	INT	Interrupt
14	DMIC_CLK	Digital MIC clock output
15	MIC1N	CH1 analog negative input
16	MIC1P	CH1 analog positive input or DMIC CH1&CH2 data input
17	REFP12	CH1&2 ADC positive reference
18	REFQ12	CH1&2 ADC negative reference
19	MIC2P	CH2 analog positive input
20	MIC2N	CH2 analog negative input
21	GNDA	Analog ground
22	VDDA	3.3V analog power
23	VDDM	3.3V Mic-Bias Power
24	MICBIAS12	Mic-bias for CH1&CH2
25	REFQM	Common Voltage
26	MICBIAS34	Mic-bias for CH3&CH4
27	MIC4N	CH4 analog negative input
28	MIC4P	CH4 analog positive input
29	REFP34	CH3&4 ADC positive reference
30	REFQ34	CH3&4 ADC negative reference
31	MIC3P	CH3 analog positive input or DMIC CH3&CH4 data input
32	MIC3N	CH3 analog negative input

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW89403QNR	-40℃～85℃	WBQFN 4X4-32L (Height 0.75)	KH4Z	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Analog Supply Voltage Level VDDA、VDDM		-0.3V to 3.63V
Digital Supply Voltage Level VDDIO		-0.3V to 3.63V
Input voltage range	VDDIO referenced digital inputs (NOTE 2)	-0.5V to VDDIO+0.5V
Operating Temperature Range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		165°C
Storage temperature T_{STG}		-65°C to 150°C
ESD Rating (NOTE 3)		
HBM (human body model)		±2kV
CDM (charged-device model)		±500V
Latch-up		
Test Condition：JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: VDDIO referenced digital pins include: AD0, AD1, MCLK, LRCLK, SCLK, SDOUT2, SDA, SCL

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2023;
Test method of the charge device model: ESDA/JEDEC JS-002-2022.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDIO	IO supply voltage	1.62	1.8/3.3	3.63	V
VDDA	Input voltage	2.97	3.3	3.63	V
VDDM	Input voltage	2.97	3.3	3.63	V

Electrical Characteristics

Characteristics

Test condition: T_A = 25°C, VDDA=VDDM = 3.3 V, VDDIO = 3.3 V, Fin = 1kHz sinusoidal signal, fs = 48 kHz, 32-bit audio data, SCLK = 128 × fs, TDM slave mode, PLL on, Differential input (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Digital Logical Interface						
V_{IH}	Logic input high level	VDDIO = 3.3 V &1.8V, MCLK, SCLK, LRCLK, SDOUT1, SDOUT2, SDA, SCL PIN	0.7 x VDDIO			V
V_{IL}	Logic input low level				0.5	V
V_{OH}	Logic output high level	VDDIO = 3.3 V &1.8V, I_{OH} = 2 mA	80%			VDDIO
V_{OL}	Logic output low level	VDDIO = 3.3 V &1.8V, I_{OH} = –2 mA			20%	VDDIO
ADC Input & Gain Configuration						
RIN	AC input impedance			9		Kohm
GAIN	Channel gain range	Programmable range with1dB/step	-6		36	dB
ADC Performance For Line/Microphone Input Recording						
VFS	Differential input full-scale AC signal voltage	AC-coupled input ；0dB channel gain；		2		Vrms
	Single-ended input full-scale AC signal voltage	AC-coupled input ；0dB channel gain；		1		Vrms
SNR〈NOTE4〉	Signal-to-noise ratio, A-weighted	AC signal shorted,0dB channel gain, SUM OFF	97	103	105	dB
		AC signal shorted,12dB channel gain, SUM OFF	95	100	103	dB
		AC signal shorted,20dB channel gain, SUM OFF	91	96	99	dB
		AC signal shorted,0dB channel gain, SUM ON, 2-channels summing	100	105	108	dB
		AC signal shorted,12dB channel gain, SUM ON, 2-channels summing	98	103	106	dB
		AC signal shorted,20dB channel gain, SUM ON, 2-channels summing	94	99	102	dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		AC signal shorted,0dB channel gain, SUM ON, 4-channels summing	103	108	111	dB
		AC signal shorted,12dB channel gain, SUM ON, 4-channels summing	101	106	109	dB
		AC signal shorted,20dB channel gain, SUM ON, 4-channels summing	97	102	105	dB
DR（NOTE4）	Dynamic range, A-weighted	Input level: -60dBFS,0dB channel gain, SUM OFF	97	103	105	dB
		Input level: -72dBFS,12dB channel gain, SUM OFF	95	100	103	dB
		Input level: -80dBFS,20dB channel gain, SUM OFF	91	96	99	dB
		Input level: -60dBFS,0dB channel gain, SUM ON, 2-channels summing	100	105	108	dB
		Input level: -72dBFS,12dB channel gain, SUM ON, 2-channels summing	98	103	106	dB
		Input level: -80dBFS,20dB channel gain, SUM ON, 2-channels summing	94	99	102	dB
		Input level: -60dBFS,0dB channel gain, SUM ON, 4-channels summing	103	108	111	dB
		Input level: -70dBFS,12dB channel gain, SUM ON, 4-channels summing	101	106	109	dB
		Input level: -80dBFS,20dB channel gain, SUM ON, 4-channels summing	97	102	105	dB
THD+N（NOTE4）	Total harmonic distortion	Input level: -1dBFS,0dB channel gain	-98	-95	-90	dB
		Input level: -13dBFS,12dB channel gain	-96	-93	-88	dB
		Input level: -21dBFS,20dB channel gain	-93	-90	-85	dB
ADC Other Performance						
X talk	Channel Separation	No measured channel amplitude with -1dBFS input		100		dB
Gain mismatch	Inter-channel gain mismatch	Input level: -6dBFS,0dB channel gain		0.1		dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	100mVPP, 1kHz sinusoidal signal on VDDA ,0dB channel gain		80		dB
CMRR	Common rejection ratio	100mVPP, 1kHz sinusoidal signal on MICxP & MICxN,0dB channel gain		60		dB
Microphone Bias						
	MICBIAS noise	BW = 20~20KHz, A-weighted		10		uVrms
	MICBIAS voltage	50mV/step	1.7	2.1	2.45	V
	MICBIAS current drive			10		mA
Typical Supply Current Consumption						
IVDDA+IVDDM	Standby mode	VDDA=VDDM=3.3V		15		uA
IVDDIO		VDDIO=3.3V		3		uA
IVDDIO		VDDIO=1.8V		1.5		uA
IVDDA+IVDDM	Current consumption with ADC 4-channel operating at f_s =16-kHz, PLL OFF, SCLK = 128 ×f_s	VDDA=VDDM=3.3V		16.5		mA
IVDDIO		VDDIO=3.3V		0.15		mA
IVDDIO		VDDIO=1.8V		0.08		mA
IVDDA+IVDDM	Current consumption with ADC 4-channel operating at f_s =16-kHz, PLL ON, SCLK = 128 ×f_s	VDDA=VDDM=3.3V		17.5		mA
IVDDIO		VDDIO=3.3V		0.15		mA
IVDDIO		VDDIO=1.8V		0.08		mA
IVDDA+IVDDM	Current consumption with ADC 4-channel operating at f_s =48-kHz, PLL OFF, SCLK = 128 ×f_s	VDDA=VDDM =3.3V		18		mA
IVDDIO		VDDIO=3.3V		0.25		mA
IVDDIO		VDDIO=1.8V		0.13		mA
IVDDA+IVDDM	Current consumption with ADC 4-channel operating at f_s =48-kHz, PLL ON, SCLK = 128 ×f_s	VDDA=VDDM =3.3V		19.5		mA
IVDDIO		VDDIO=3.3V		0.25		mA
IVDDIO		VDDIO=1.8V		0.13		mA
Digital Filter Characteristics						
	Digital volume control range	Programmable 0.094dB/step	-96		30	dB
	Output data sample rate	Programmable	8		768	kHz
	Output data sample word length	Programmable	8		32	Bits

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3dB point (default setting)		2		Hz
	Linear Digital filter response @8~192KHz					
	Passband frequency		0		0.453	Fs
	Stopband frequency		0.60			Fs
	Passband ripple		-0.025		0.025	dB
	Stopband attenuation		73			dB
	Group Delay 〔NOTE5〕				11	1/fs
	Low-Latency Digital filter response @8~192KHz					
	Passband frequency		0		0.453	Fs
	Stopband frequency		0.60			Fs
	Passband ripple		-0.025		0.025	dB
	Stopband attenuation		73			dB
	Group Delay Distortion (0~20kHz)				2.1	1/fs
	Group Delay				5.8	1/fs
	Digital filter response @ 384KHz					
	Passband frequency		0		0.208	Fs
	Stopband frequency		0.796			Fs
	Passband ripple		-0.25		0.25	dB
	Stopband attenuation		48			dB

NOTE4: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

NOTE5: The Calculated delay time inducted by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDOUT.

I2C INTERFACE TIMING

Parameter			Fast mode			UNIT
No.	Sym	Name	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400	kHz
2	t_{LOW}	SCL Low level Duration	1.3			μs
3	t_{HIGH}	SCL High level Duration	0.6			μs
4	t_{RISE}	SCL, SDA rise time			0.3	μs
5	t_{FALL}	SCL, SDA fall time			0.3	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			μs
9	t_{BUF}	The Bus idle time START state to STOP state	1.3			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			μs
11	$t_{HD:DAT}$	SDA hold time	10			ns

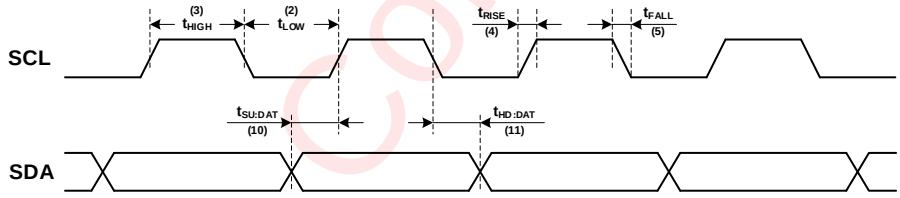


Figure 4 SCL and SDA timing relationships in the data transmission process

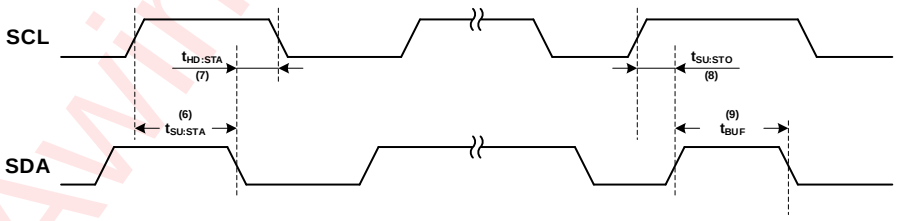


Figure 5 The timing relationship between START and STOP state

DIGITAL AUDIO INTERFACE TIMING (NOTE4)

Parameter Name			Min	Typ.	Max	Units
$t_{(SCLK)}$	SCLK period		40 (NOTE6)			ns
$t_{H(SCLK)}$	SCLK high pulse duration		18			ns
$t_{L(SCLK)}$	SCLK low pulse duration		18			ns
$t_{d(SDOUT-SCLK)}$	SCLK to SDOUT1/SDOUT2 delay				18	ns
$t_{d(SDOUT-LRCLK)}$	LRCLK to SDOUT1/SDOUT2 delay in TDM or LJ mode (for MSB data with = 0)				18	ns
$t_{d(LRCLK)}$	SCLK to LRCLK delay: master mode				18	ns
$t_{SU(LRCLK)}$	LRCLK setup time		8			ns
$t_{HLD(LRCLK)}$	LRCLK hold time		8			ns
$t_{r(SCLK)}$	SCLK rise time	10% - 90% rise time			10	ns
$t_{f(SCLK)}$	SCLK fall time	90% - 10% fall time			10	ns
$t_{r(SCLK)}$	SCLK rise time: master mode	10% - 90% rise time			8	ns
$t_{f(SCLK)}$	SCLK fall time: master mode	90% - 10% fall time			8	ns

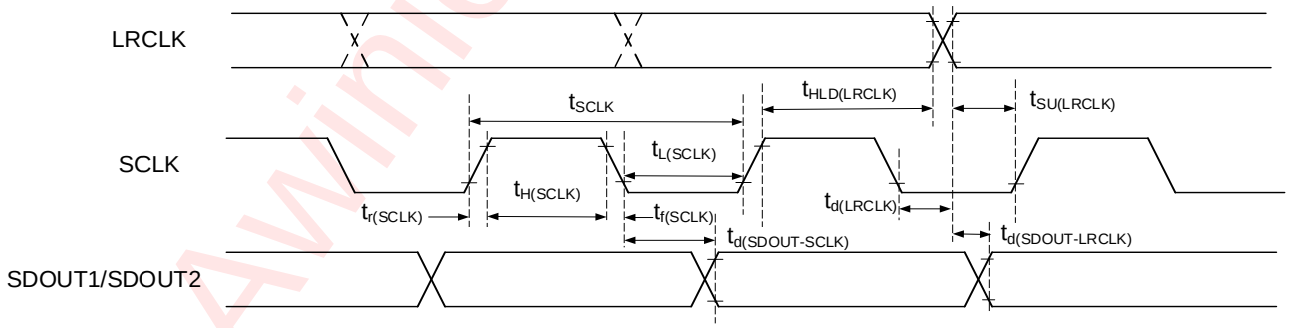


Figure 6 Digital Audio Interface Timing

NOTE6: The SCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT1/SDOUT2 data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT1/SDOUT2 data.

PDM INTERFACE TIMING (NOTE4)

Parameter Name			Min	Typ.	Max	Units
$f_{(PDMCLK)}$	PDMCLK clock frequency		0.768		6.144	MHz
$t_{H(PDMCLK)}$	PDMCLK high pulse duration		72			ns
$t_{L(PDMCLK)}$	PDMCLK low pulse duration		72			ns
$t_{SU(PDMINx)}$	PDMINx setup time		30			ns
$t_{HLD(PDMINx)}$	PDMINx hold time		0			ns
$t_{r(PDMCLK)}$	PDMCLK rise time	10% - 90% rise time			18	ns
$t_{f(PDMCLK)}$	PDMCLK fall time	90% - 10% fall time			18	ns

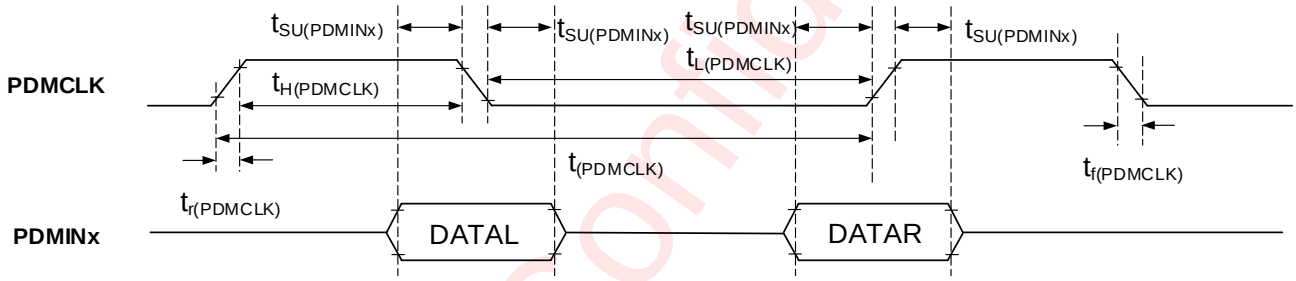
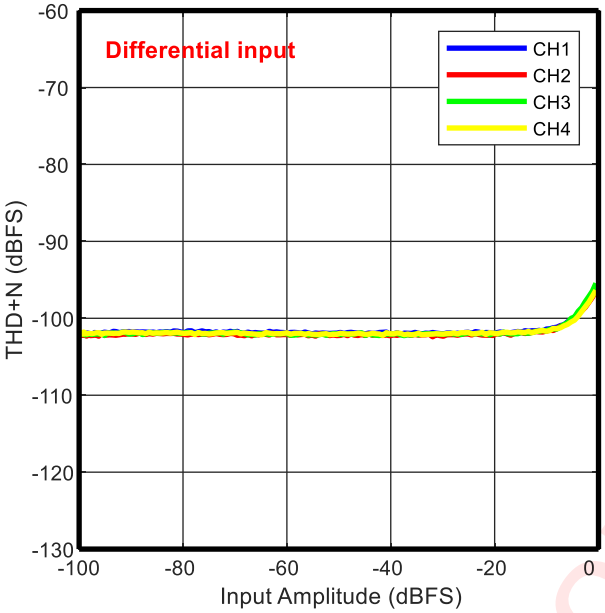


Figure 7 PDM Digital Microphone Interface Timing

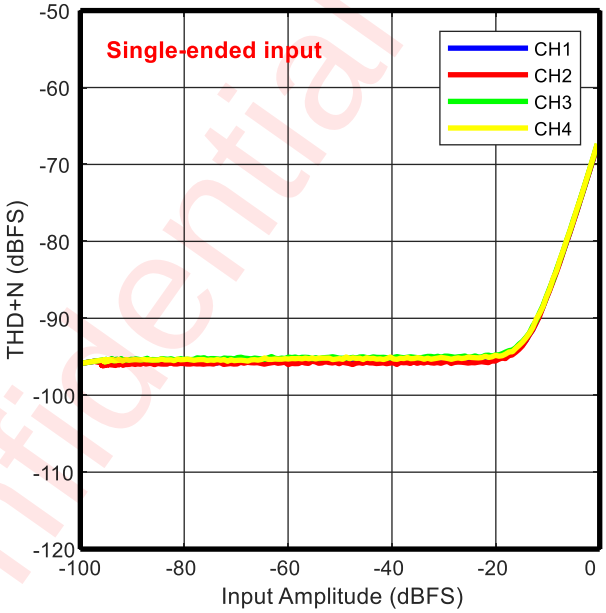
Typical Characteristics Curves

Test condition: T_A = 25°C, VDDA=VDDM = 3.3 V, VDDIO = 3.3 V, Fin = 1kHz sinusoidal signal, fs = 48 kHz, 32-bit audio data, SCLK = 128 × fs, TDM slave mode, PLL on, Sum-mixer off, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

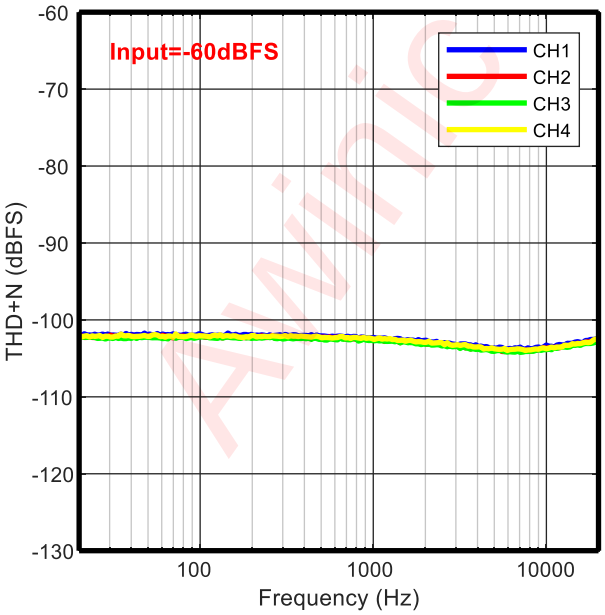
THD+N VS. Input Amplitude



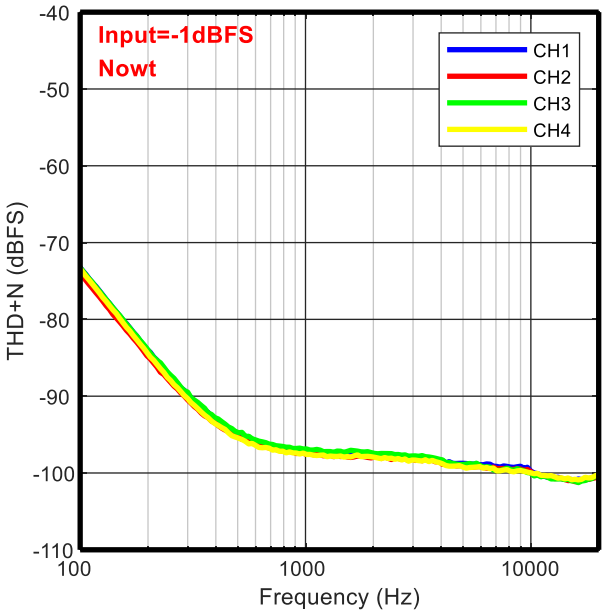
THD+N VS. Input Amplitude



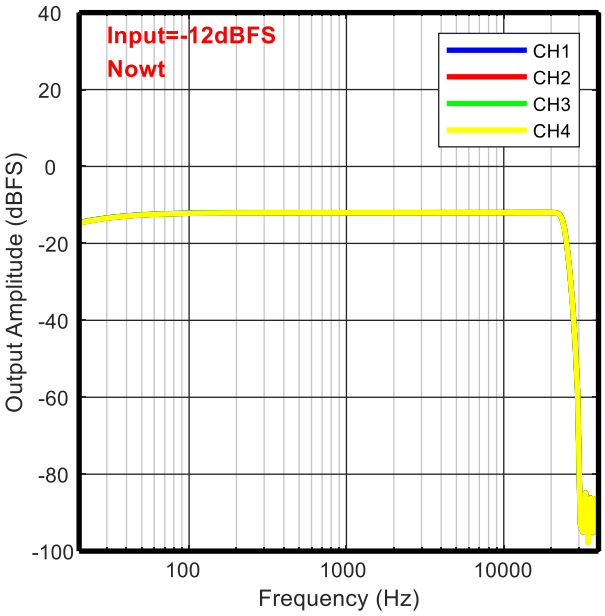
THD+N VS. Frequency



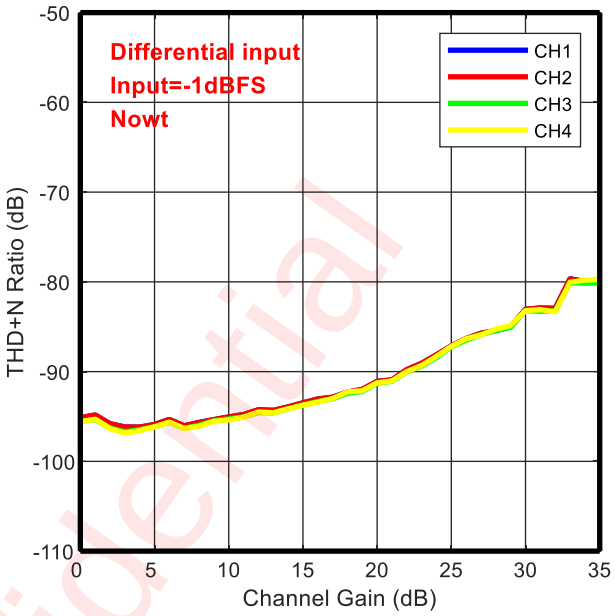
THD+N VS. Frequency



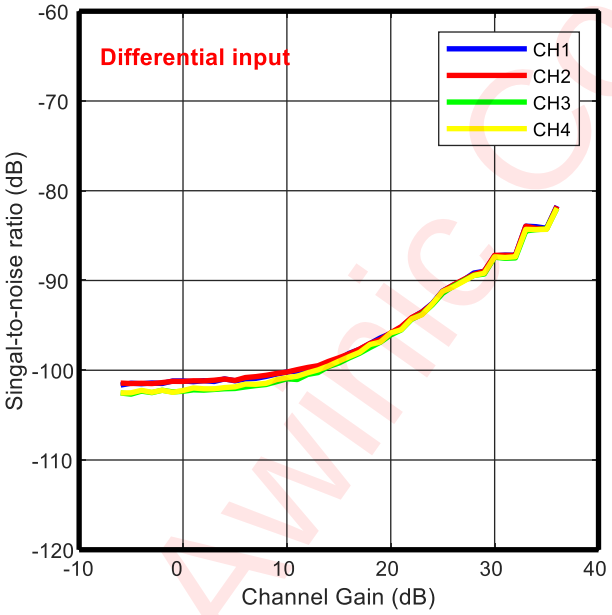
Output Amplitude VS. Frequency



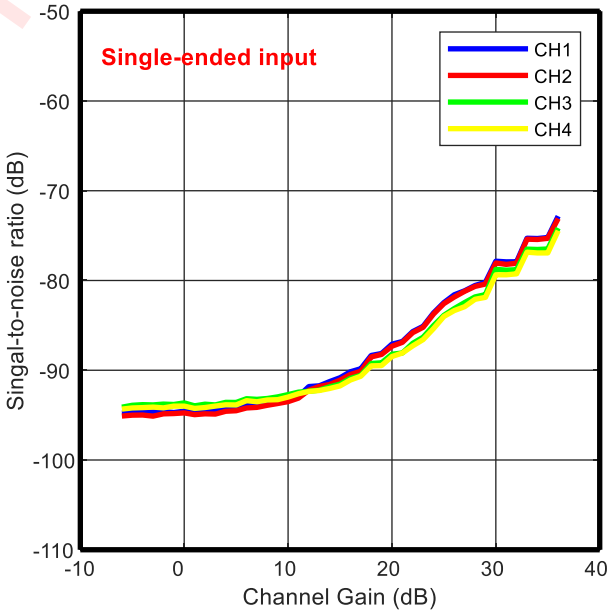
THD+N Ratio VS. Channel Gain



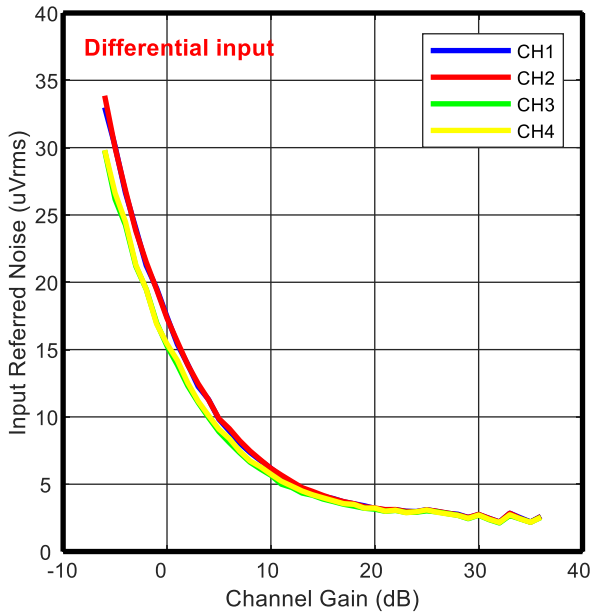
SNR VS. Channel Gain



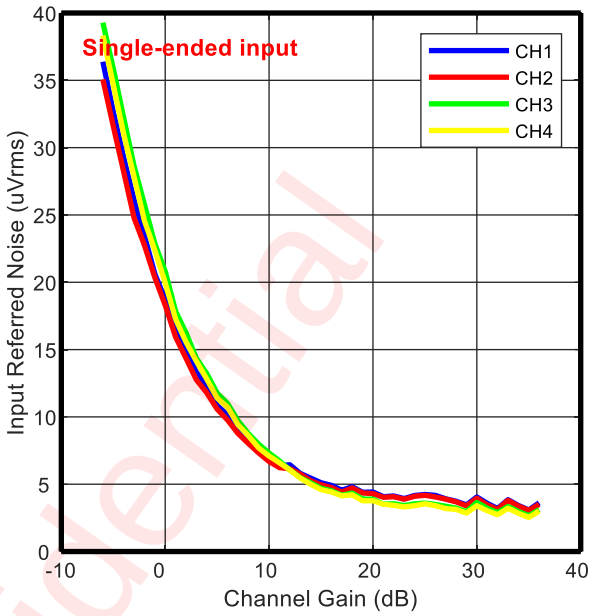
SNR VS. Channel Gain



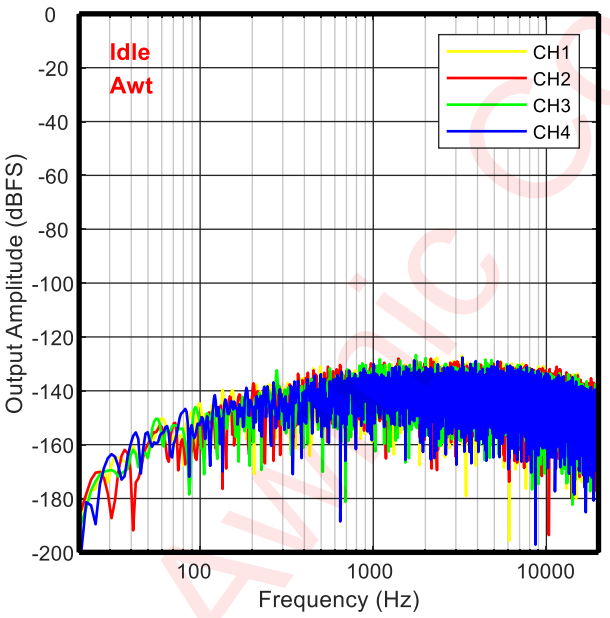
Input-Referred Noise VS. Channel Gain



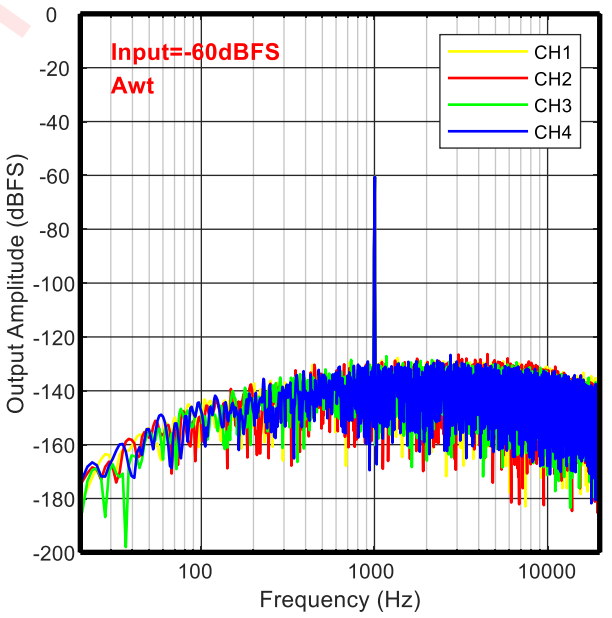
Input-Referred Noise VS. Channel Gain

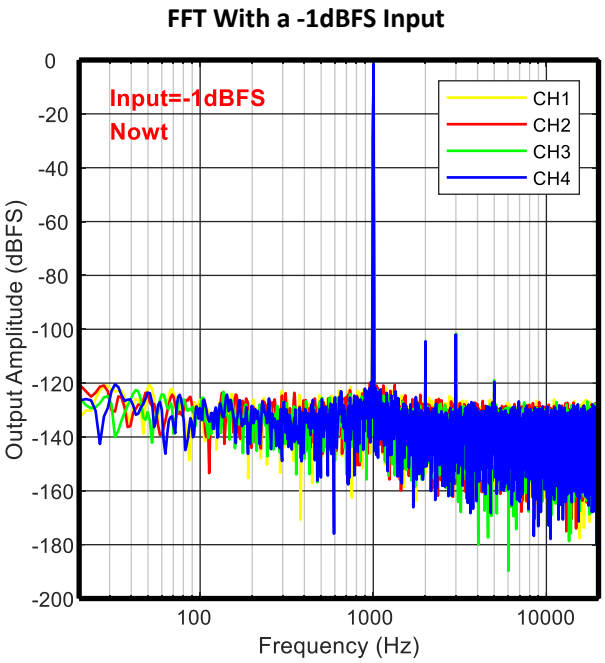


FFT With Idle Input



FFT With a -60dBFS Input





Detailed Functional Description

POWER ON RESET

The device provides a power-on reset feature that is controlled by VDDA&VDDIO supply voltage. When the VDDA supply voltage raises from 0V to 2V or VDDIO supply voltage from 0V to 1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 3 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	V_{VDDA} < 2.2V V_{VDDIO} < 1.2V	Power supply is not ready, chipset is power down.
Standby	V_{VDDA} > 2.97V V_{VDDIO} > 1.62V	Power supply is ready, most parts of the device are power down for low power consumption except I²C interface
Normal work (NOTE7)	V_{VDDA} > 2.97V V_{VDDIO} > 1.62V	1. Turn on Internal LDO& Bias 2. Turn on PLL&CLK_GEN 3. Turn on ADC path 4. Turn on Digital path

NOTE7: Detailed registers config need refer to DG_AW8940X_Software_Design_Guide_EN.

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- V_{VDDA} < 2.2V
- V_{VDDIO} < 1.2 V

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

V_{VDDA} > 2.97 V and V_{VDDIO} > 1.62V

STANDBY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

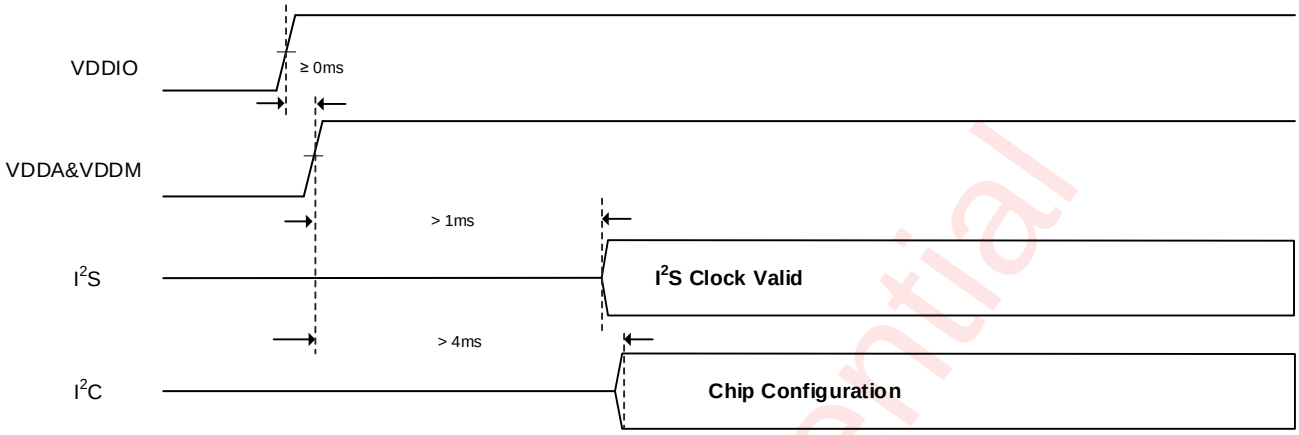
NORMAL WORK

The device switches to Normal mode when:

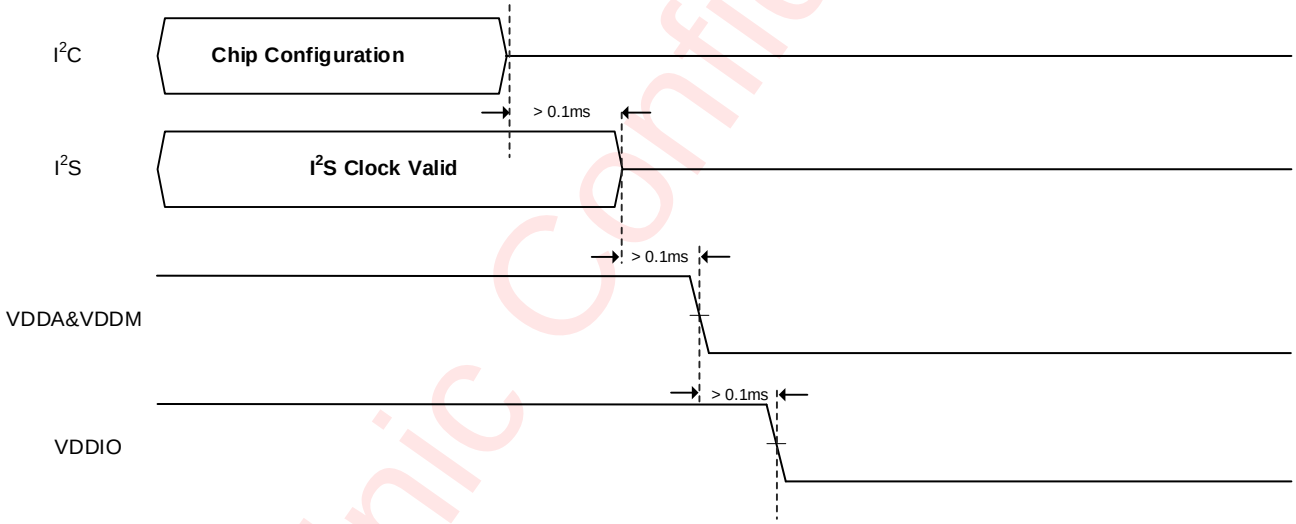
- Turn on internal LDO& Bias;
- Turn on PLL&CLK_GEN

- Turn on ADC path
- Turn on Digital path

Power up sequence considering I²S, I²C timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



SOFTWARE RESET

Writing 0xAA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL I/O STATUS

The state of each digital input and output are shown in below table. In standby mode I2C related IOs (SCL, SDA, AD0, AD1) are weakly pull down inside chip and I2S related IOs are Hi-Z.

Table 2 Digital I/O status description

Digital I/O	Type	Description (Standby)
SCL	Input	Weak pull down

Digital I/O	Type	Description (Standby)
SDA	Input/ Output	Weak pull down
AD0	Input	Weak pull down
AD1	Input	Weak pull down
INT	Output	Hi-Z
SCLK	Input/ Output	Hi-Z
LRCLK	Input/ Output	Hi-Z
SDOUT1	Output	Hi-Z
SDOUT2	Input/ Output	Hi-Z
MCLK	Input	Hi-Z

PROGRAMMABLE MICROPHONE BIAS

The device integrates two built-in, low-noise microphone bias pins that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The integrated bias amplifier supports up to 10 mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine-tuned for specific microphone combinations.

When using this MICBIAS12/MICBIAS34 pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS12/MICBIAS34 connection to minimize coupling across microphones. Table 11 shows the available microphone bias programmable options.

Table 3 MICBIAS Programmable Settings

MICBIAS12_SEL<3:0> MICBIAS34_SEL<3:0>	Microphone Bias Voltage
0000	1.7V
0001	1.75V
0010	1.8V
0011	1.85V
…	…
1000	2.1V
…	…
1110	2.4V
1111	2.45V

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 5 dedicated pins:

- MCLK
- SCLK
- LRCLK
- SDOUT1
- SDOUT2/TDMIN

Two-slot I²S and 1/2/4/6/8/16-slot TDM are supported in this device. The digital audio Interface on this device supports slave/master mode and flexible with data width options, including 8~32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL2.I2S_LRCLK_INV and I2SCTRL3.I2S_LRCLK_SL. These modes are all MSB-first, with data width programmable via I2SCTRL4.I2S_WORD_WIDTH and I2SCTRL5.I2S_BIT_DEEPTH.

The word clock LRCLK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8kHz~768kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock SCLK is used to transmit the digital audio data across the digital audio interface. The number of bit-clock pulses in an audio slot defined as slot length. The kind of slot length are supported (8~32) via configurable register I2SCTRL4.I2S_WORD_WIDTH. The frequency of SCLK can be calculated according to the following equation:

$$SCLK\ frequency = \boldsymbol{SampleRate} * \boldsymbol{SlotLength} * \boldsymbol{SlotNumber}$$

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of SCLK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 1/2/4/6/8/16-slot supported in TDM mode.

The word selected signal (LRCLK), bit clock signal (SCLK) and master clock signal (MCLK) of the I²S input can be the reference signals for the digital audio interface and Phased Locked Loop (PLL) in slaver mode. While using I2S/TDM master mode, only MCLK can be reference clock of PLL. LRCLK and SCLK are generated by AW89403.

Four channels audio signals can be configured on any slot on data-line SDOUT1 or SDOUT2 via I2SCTRL7.I2S_CH1_SLOTVLD, I2SCTRL8.I2S_CH2_SLOTVLD, I2SCTRL9.I2S_CH3_SLOTVLD and I2SCTRL10.I2S_CH4_SLOTVLD.

Table 4 Supported I²S interface parameters

Interface format (MSB first)	Data width	CLK frequency
Standard I²S	8~32b	16fs~64fs
Left-justified	8~32b	16fs~64fs
Right-justified	8~32b	16fs~64fs

The output port SDOUT1/SDOUT2, can be enabled or disabled via bit I2SCTRL6.I2S_TX_EN. In addition, SDOUT1 and SDOUT2 can be enabled or disabled separately via I2SCTRL6.I2S_TX_CH1_EN and I2SCTRL6.I2S_TX_CH2_EN. The unused slots can be set to Hi-z or normal working, which is controlled by I2SCTRL6.I2S_SLOT_DOHZ. The unused bits of each slot can be set Hi-z or normal working via bit I2SCTRL3.I2S_DOHZ

STANDARD I²S MODE

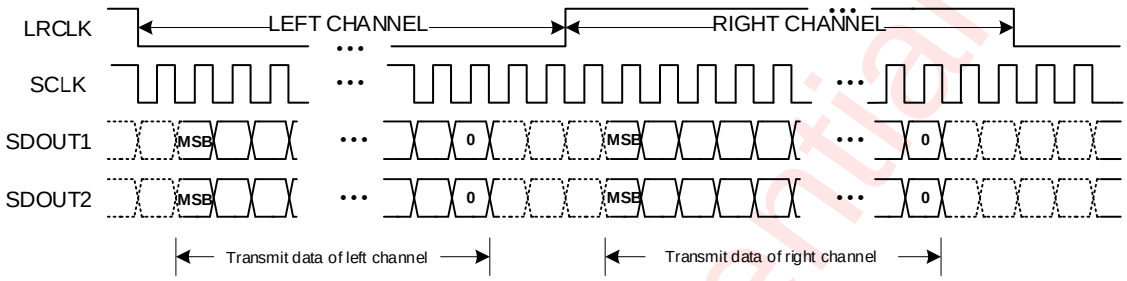


Figure 8 I²S Timing for Standard I²S Mode

- When LRCLK=0 indicating the left channel data, and LRCLK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

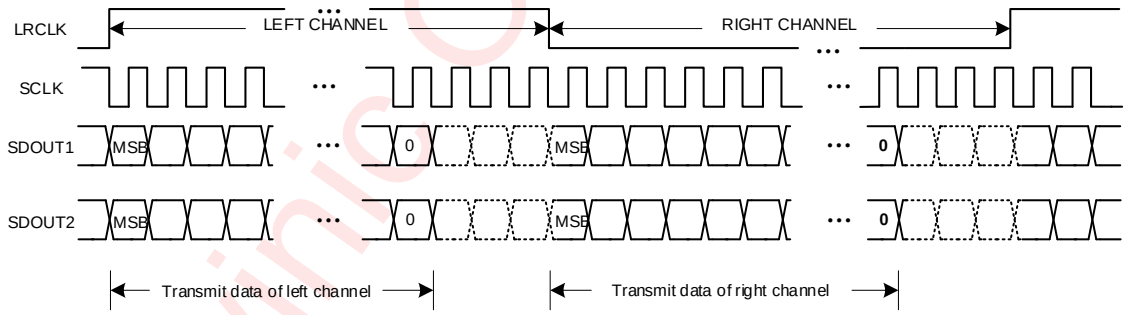


Figure 9 I²S Timing for Left-Justified Mode

- When LRCLK=1 indicating the left channel data, and LRCLK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

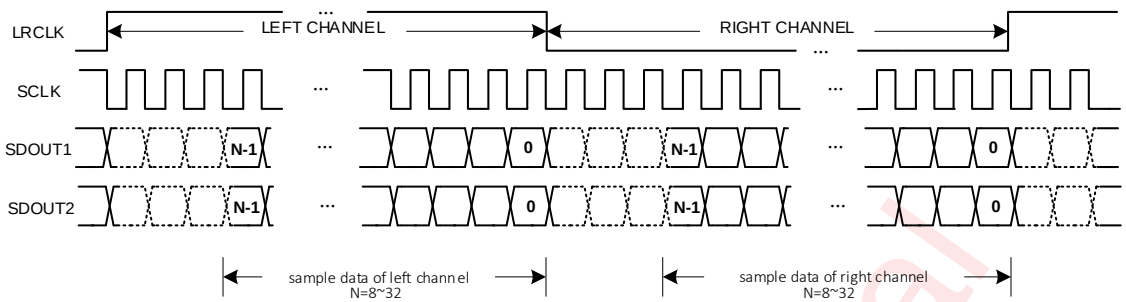


Figure 10 I²S Timing for Right-Justified Mode

- When LRCLK is high indicating the left channel data, and LRCLK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number. 1/2/4/6/8/16-slot is supported in TDM mode, while 2-slot is supported in I²S mode. The offset bits between slot0 and rise edge of LRCLK can configured via I2SCTRL3.I2S_LRCLK_SL.

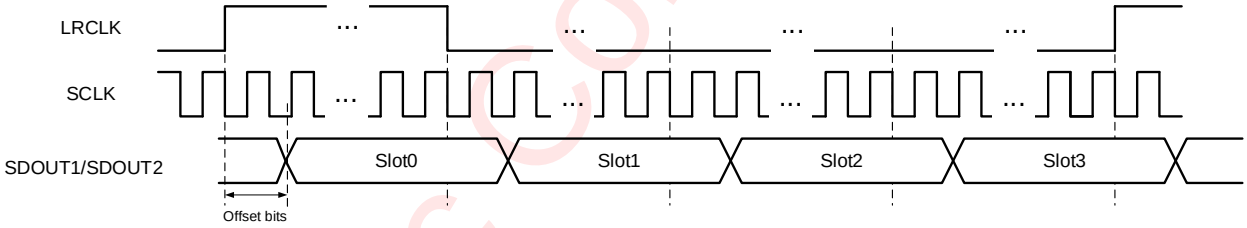


Figure 11 TDM Timing

Note: The high-level pulse width of LRCLK signal can be one slot time or one period of SCLK.

DIGITAL AUDIO PROCESSING

This device incorporates one programmable Digital Audio Processor (DAP) block. It provides the algorithm for audio signal processing and speaker protection. The following functions are available in this module.

- Decimation Filter
- Phase Calibration
- HDCC
- Hardware AGC
- Sum-Mixer

- Volume control
- Hardware Mute

The signal processing flow in the Digital Audio Processor (DAP) is illustrated in the following figure.

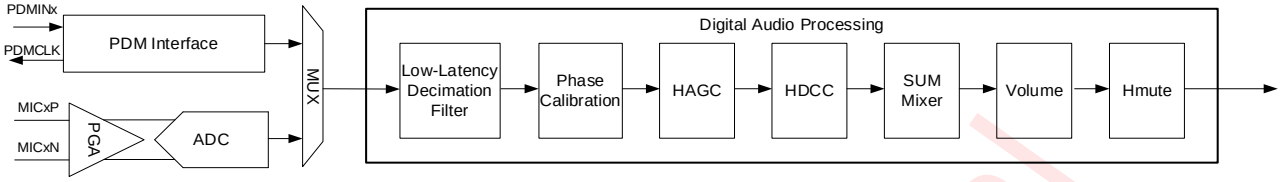


Figure 12 Block Diagram of DAP

DECIMATION FILTER

The device record channel includes a high dynamic range, built-in digital decimation filter to process the over sampled data from the multibit delta-sigma ($\Delta\Sigma$) modulator to generate digital data at the same Nyquist sampling rate as the LRCLK rate. As illustrated in Figure 12, this decimation filter can also be used for processing the oversampled PDM stream from the digital microphone.

The digital decimation filter includes two modes, namely linear-phase mode and low-latency mode. In scenarios that require high phase linearity, such as high-quality speech recording, the linear phase mode can be selected. In scenarios with low channel delay, such as active noise cancelling, the low-latency mode can be used.

PHASE CALIBRATION

The phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 128 for the phase error. The modulator clock is 6.144 MHz (the output data sample rate is multiples or submultiples of 48 kHz), 5.6448 MHz (the output data sample rate is multiples or submultiples of 44.1 kHz) or 4.096 MHz (the output data sample rate is multiples or submultiples of 32 kHz) irrespective of the analog microphone or digital microphone use case. This feature is very useful for many applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones.

HDCC

This module performs hardware DC canceling for the audio stream sampled from Microphone. It blocks DC components transmitted to the host via I2S/TDM interface.

HAGC

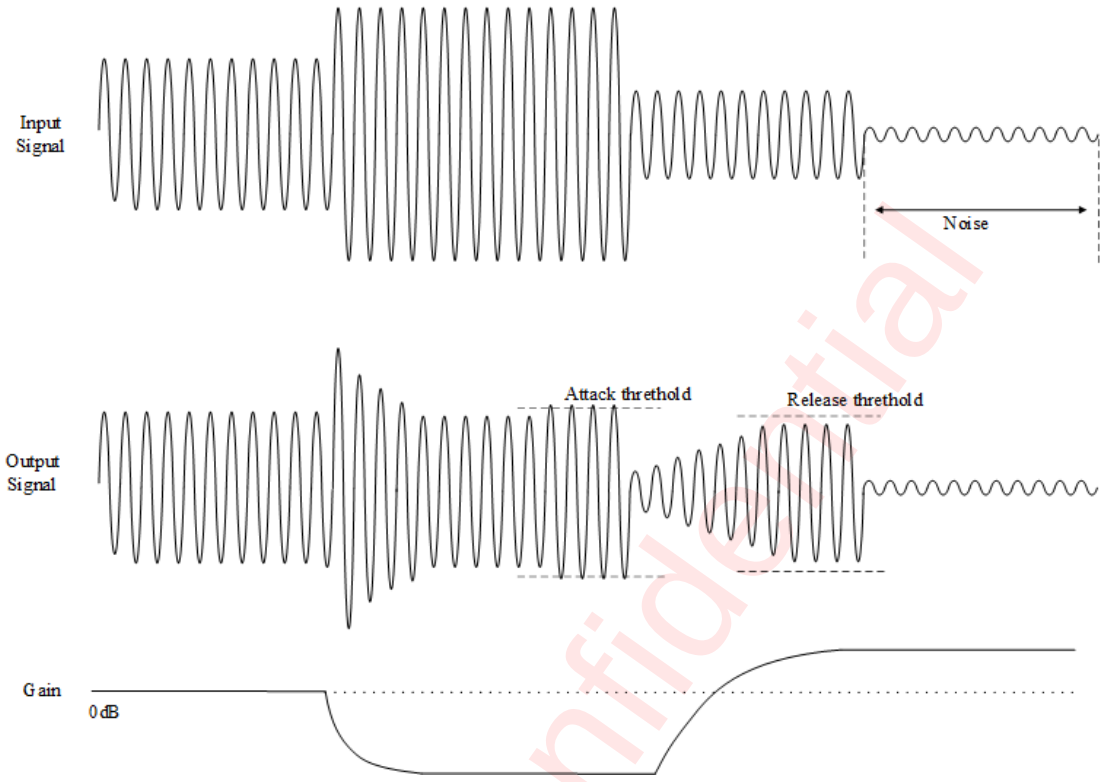


Figure 13 HAGC Characteristics

The AGC function ensures that the amplitude of the output signal stays within a preset range by monitoring the level of the input signal in real time and adjusting the gain accordingly. It can attenuate the large signal and increase the small signal, while ensuring that the noise is not amplified. For example, speaker moves closer and further away from the microphone in a voice meeting, and the listener hears the sound louder and smaller, the AGC can be used to send a normal constant output. The AGC function is controlled by several parameters, including the attack threshold, release threshold, noise threshold, attack time, release time, noise time, max gain and gain step, which allow to make adjustment for any particular application.

SUM-MIXER

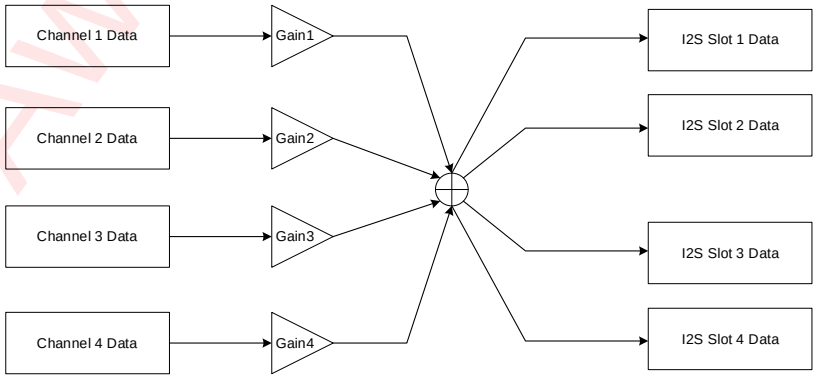


Figure 14 Sum-mixer Block Diagram

For applications that require an even higher SNR than that supported for each channel, the sum-mixer mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise.

VOLUME CONTROL

The volume control function attenuates or gains the audio signal at the end of digital audio processing. The range of volume setting is from +30dB to -96dB with 0.094dB/step.

HMUTE

This module performs mute control for the audio stream which is sampled from microphone.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 10000xx. The permitted I²C addresses are 0x40(7-bit) through 0x43(7-bit).

Table 5 Address Selection

AD1	AD0	Address(7-bit)
GND	GND	0x40
GND	VDDIO	0x41
VDDIO	GND	0x42
VDDIO	VDDIO	0x43

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

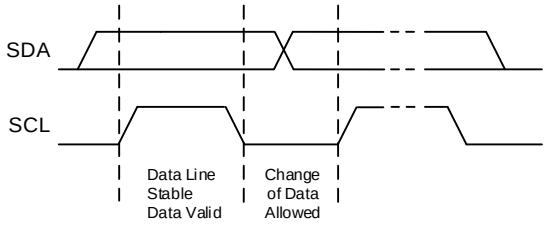


Figure 15 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

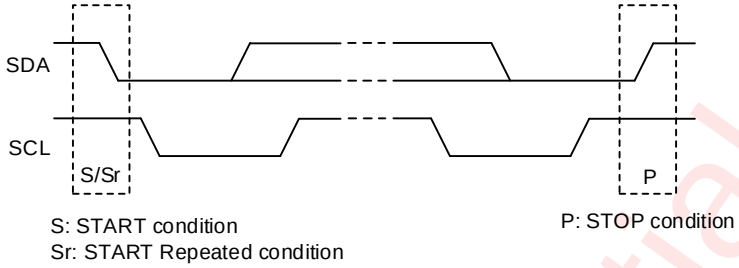


Figure 16 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

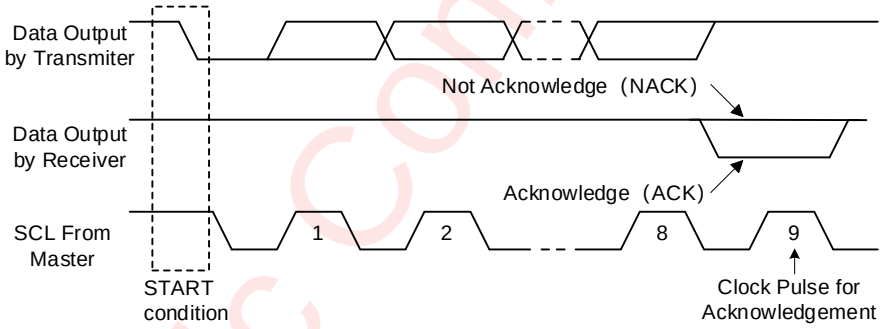


Figure 17 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends 8-bit data to be written to the addressed register.

g) Slave sends acknowledge signal.

h) If master will send further 8-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g).

i) Master generates STOP condition to indicate write cycle end.

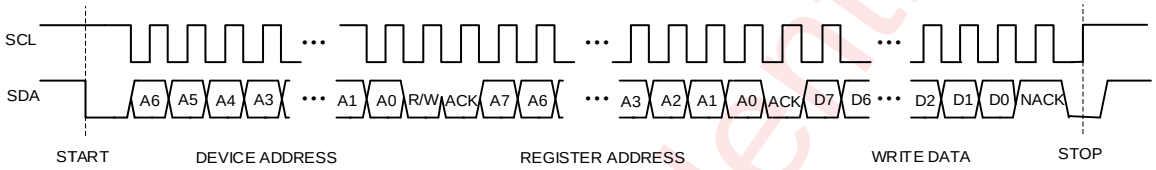


Figure 18 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates STOP condition followed with START condition or REPEAT START condition.

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read 8-bit data from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 8-bit data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

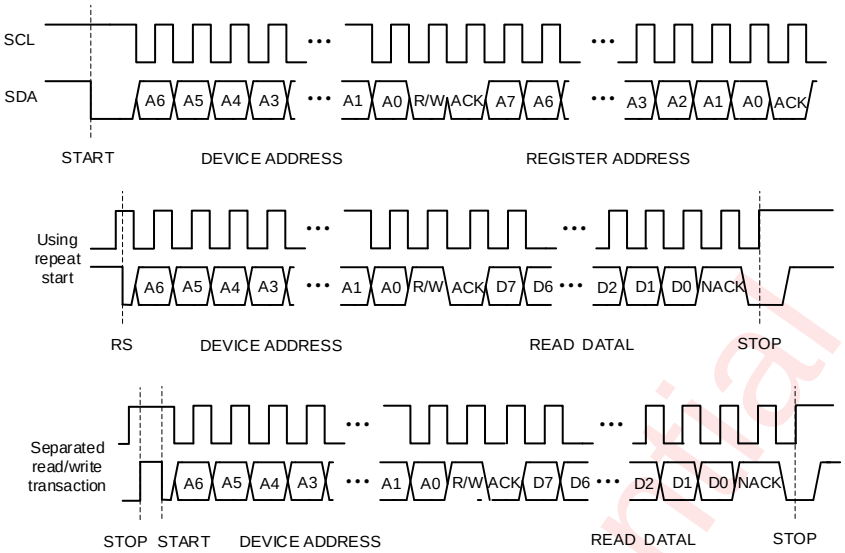
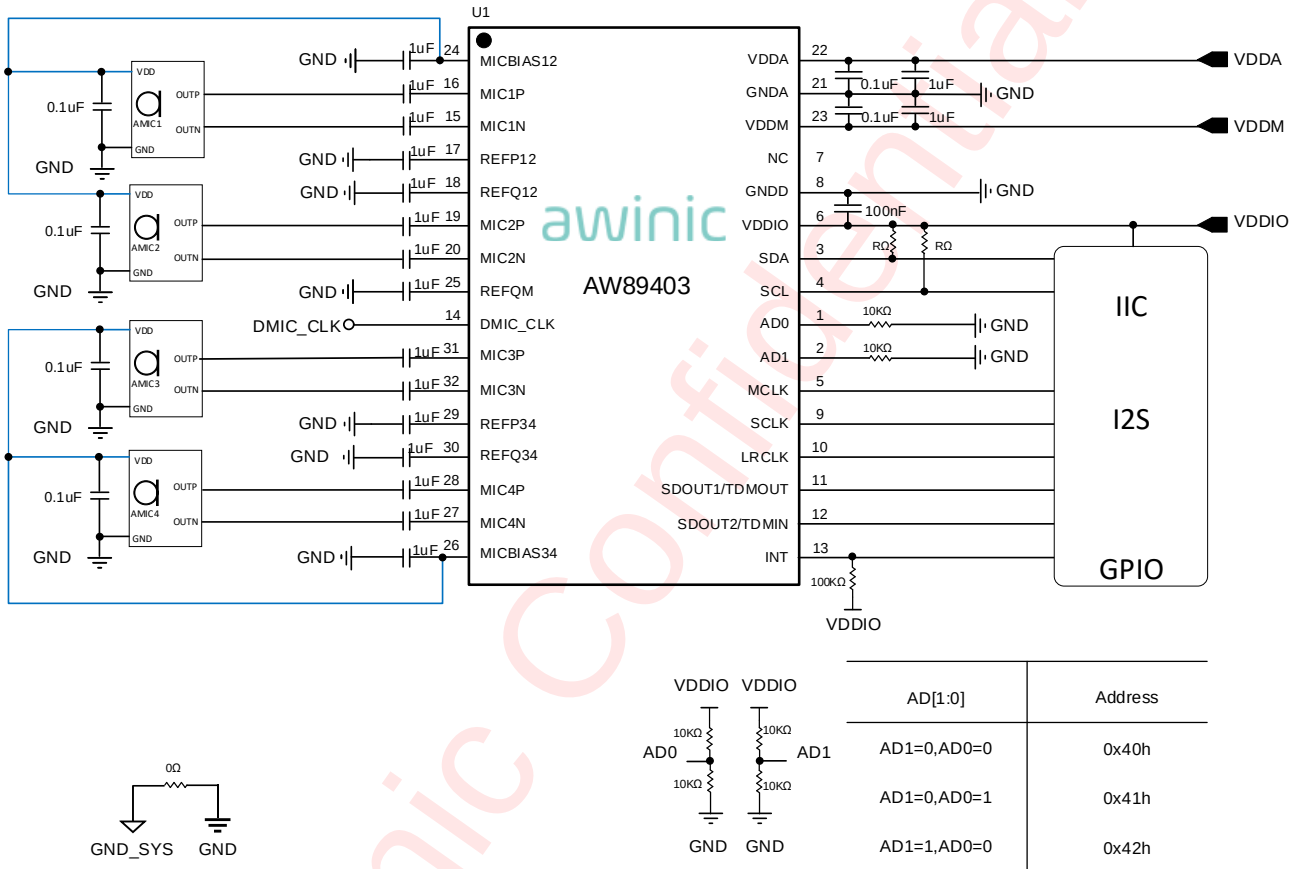


Figure 19 I²C Read Byte Cycle

Application Information

APPLICATION CIRCUIT FOR ANALOG MICROPHONE

Figure20 shows a typical configuration of the AW89403 for an application using four analog micro-electrical mechanical system (MEMS) microphones for simultaneous recording operation with an I2C control interface and a time-division multiplexing (TDM) audio data slave interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

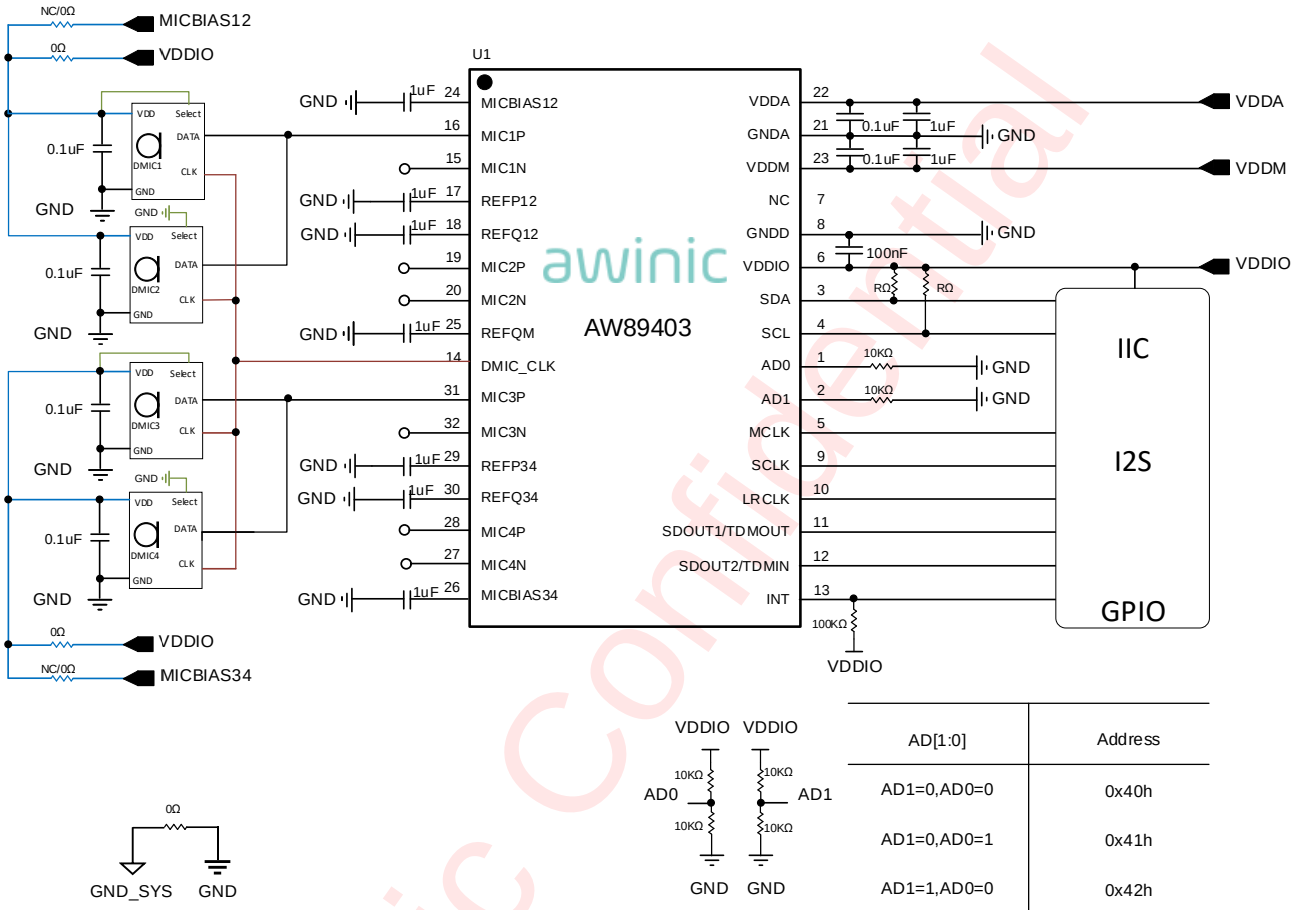


AD[1:0]	Address
AD1=0,AD0=0	0x40h
AD1=0,AD0=1	0x41h
AD1=1,AD0=0	0x42h
AD1=1,AD0=1	0x43h

Figure 20 Four-Channel Analog Microphone Recording Diagram

APPLICATION CIRCUIT FOR DIGITAL PDM MICROPHONE

Figure21 shows a typical configuration of the AW89403 for an application using four digital PDM MEMS microphones with simultaneous recording operation using an I2C control interface and the TDM audio data slave interface.



AD[1:0]	Address
AD1=0,AD0=0	0x40h
AD1=0,AD0=1	0x41h
AD1=1,AD0=0	0x42h
AD1=1,AD0=1	0x43h

Figure 21 Four-Channel Digital PDM Microphone Recording Diagram

LAYOUT CONSIDERATION

In order to obtain excellent performance of the ADC, the below PCB layout guidelines should be followed:

1. The power supply of AW89403 must be isolate from system power supply. A LDO specified for AW89403 is recommended in order to get the best audio performance.
2. GNDD and GNDA must be connect to the same analog ground plane, and then join into system ground at a single point nearby the power supply. It is important to prevent high frequency noise or high current noise from going into audio ground plane.
3. There need some decoupling and filter capacitors on VDDM, VDDA, MICBIAS, REFP and REFQ pins. These decoupling and filter capacitors must be as near to AW89403 package as possible, with the low value ceramic capacitor being the nearest
4. All signals, especially clocks, should be kept away from MICBIAS, REFP and REFQM in order to avoid unwanted coupling to ADC modulators.
5. There is a thermal pad on the bottom of AW89403 package. In practical system, the thermal pad must be connected to ground plane by via.

Register Configuration

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	IDH	*RO*	IDCODE_H								0x22
0x01	IDL	*RO*	IDCODE_L								0x16
0x02	SYSST	*RO*	SCLK_ERRS	NO_MCLKS	NO_LRCLKS	NO_SCLKS	NOCLKS	CLKS	OC_FLAG34S	OC_FLAG12S	0x00
0x03	SYSINT	*RC*	SCLK_ERRI	NO_MCLKI	NO_LRCLKI	NO_SCLKI	NOCLKI	CLKI	OC_FLAG34I	OC_FLAG12I	0x00
0x04	SYSINTM	*RW*	SCLK_ERRM	NO_MCLKM	NO_LRCLKM	NO_SCLKM	NOCLKM	CLKM	OC_FLAG34M	OC_FLAG12M	0xFF
0x06	SYSCTRL1	*RW*	VOL_CZBYP	CH_SUM_SUB_EN	INTN	I2S_EN	CH_SUM		SYSCE	PWDN	0x03
0x07	SYSCTRL2	*RW*	I2C_WEN		CH4_EN	CH3_EN	CH2_EN	CH1_EN			0x3D
0x08	CHCTRL1	*RW*	CH1_HAGCE	CH1_HDCCE	CH1_HMUTE						0x60
0x09	CHCTRL2	*RW*	CH2_HAGCE	CH2_HDCCE	CH2_HMUTE						0x60
0x0A	CHCTRL3	*RW*	CH3_HAGCE	CH3_HDCCE	CH3_HMUTE						0x60
0x0B	CHCTRL4	*RW*	CH4_HAGCE	CH4_HDCCE	CH4_HMUTE						0x60
0x0C	VOLCTRL1	*RW*		CH1_VOL_UP			CH1_VOL_DOWN_INT				0x10
0x0D	VOLCTRL2	*RW*			CH1_VOL_DOWN_FRAC						0x3F
0x0E	VOLCTRL3	*RW*		CH2_VOL_UP			CH2_VOL_DOWN_INT				0x10
0x0F	VOLCTRL4	*RW*			CH2_VOL_DOWN_FRAC						0x3F
0x10	VOLCTRL5	*RW*		CH3_VOL_UP			CH3_VOL_DOWN_INT				0x10
0x11	VOLCTRL6	*RW*			CH3_VOL_DOWN_FRAC						0x3F
0x12	VOLCTRL7	*RW*		CH4_VOL_UP			CH4_VOL_DOWN_INT				0x10
0x13	VOLCTRL8	*RW*			CH4_VOL_DOWN_FRAC						0x3F
0x20	I2SCTRL1	*RW*	I2S_CLK_MODE			I2SSR					0x08
0x21	I2SCTRL2	*RW*	I2S_FR_PLS_TYP		I2S_LRCLK_INV	I2S_SCLK_IPN	I2S_SCLK_OPN		I2S_JUSTIF_TYP		0x14
0x22	I2SCTRL3	*RW*	I2S_DOHZ	I2S_LRCLK_SL							0x00
0x23	I2SCTRL4	*RW*	I2S_LRCLK_SR	I2S_WORD_WIDTH							0x1F
0x24	I2SCTRL5	*RW*				I2S_BIT_DEPTH					0x1F
0x25	I2SCTRL6	*RW*	I2S_CHANNELS			I2S_TX_SDOUT2_EN	I2S_TX_SDOUT1_EN	I2S_SLOT_DOHZ	I2S_TX_EN	I2S_CASCADE_MD	0x1C

0x26	I2SCTRL7	RW				I2S_CH1_SLOTVLD					0x00
0x27	I2SCTRL8	RW				I2S_CH2_SLOTVLD					0x01
0x28	I2SCTRL9	RW				I2S_CH3_SLOTVLD					0x10
0x29	I2SCTRL10	RW				I2S_CH4_SLOTVLD					0x11
0x2D	FLTCTRL1	RW		HBF_PHASE_CTRL							0xC3
0x2E	PDMCTRL	RW				PDM_MD	PDM12_EDGE	PDM34_EDGE	DMIC_CLK_SEL		0x02
0x31	ADC1CTRL2	RW			PGA1_GAINSEL						0x00
0x33	ADC2CTRL2	RW			PGA2_GAINSEL						0x00
0x35	ADC3CTRL2	RW			PGA3_GAINSEL						0x00
0x37	ADC4CTRL2	RW			PGA4_GAINSEL						0x00
0x3C	ADCSCTRL5	RW						SDM_PDIREF			0x04
0x3D	ADCSCTRL6	RW						VCM_FSTUP	VCM_EN		0x00
0x3E	ADCSCTRL7	RW								CH12_ADC_CLKEN	0x00
0x3F	ADCSCTRL8	RW								CH34_ADC_CLKEN	0x00
0x40	MICBIAS12CTRL1	RW			MICB12_SEL				MICB12_FST	MICB12_PWD	0x01
0x42	MICBIAS34CTRL1	RW			MICB34_SEL				MICB34_FST	MICB34_PWD	0x01
0x45	PLL_CTRL2	RW		PLL_PD							0x40
0x49	PLL_CTRL6	RW	IPLL		MCLK_FREQ_SEL						0x10
0x4C	MISCCTRL2	RW					LDO_LP_EN	BG_V2I_EN			0x88
0x4F	ANA_SYSCTRL	RW	PGA4_PD	PGA3_PD	PGA2_PD	PGA1_PD	SDM4_PD	SDM3_PD	SDM2_PD	SDM1_PD	0xFF
0x50	CH1_DLY	RW		CH1_FRAC_DLY2		CH1_FRAC_DLY1					0x00
0x51	CH2_DLY	RW		CH2_FRAC_DLY2		CH2_FRAC_DLY1					0x00
0x52	CH3_DLY	RW		CH3_FRAC_DLY2		CH3_FRAC_DLY1					0x00
0x53	CH4_DLY	RW		CH4_FRAC_DLY2		CH4_FRAC_DLY1					0x00
0x54	HDCC_COEF1	RW		CH2_ALPHA_HDCC				CH1_ALPHA_HDCC			0x44
0x55	HDCC_COEF2	RW		CH4_ALPHA_HDCC				CH3_ALPHA_HDCC			0xC4

0x5A	ANAST A1	*RO*			PGA1_GAINSEL_ST						0x00
0x5B	ANAST A2	*RO*			PGA2_GAINSEL_ST						0x00
0x5C	ANAST A3	*RO*			PGA3_GAINSEL_ST						0x00
0x5D	ANAST A4	*RO*			PGA4_GAINSEL_ST						0x00
0x60	AGC_ CTRL1	*RW*					AGC_MAX_GAIN				0x0B
0x61	AGC_ CTRL2	*RW*	AGC_NOISE_TH								0x10
0x62	AGC_ CTRL3	*RW*	AGC_ATT_TH								0x09
0x63	AGC_ CTRL4	*RW*	AGC_REL_TH								0x05
0x64	AGC_ CTRL6	*RW*	ATTH								0x00
0x65	AGC_ CTRL8	*RW*	RTTH								0x00
0x66	AGC_ CTRL9	*RW*	ATT_HOLDTH								0x02
0x67	AGC_ CTRL10	*RW*	REL_HOLDTH								0x64
0x68	AGC_ CTRL11	*RW*	NOISE_HOLDTH								0x32
0x69	AGC_ CTRL12	*RW*		REL_GAIN_STEP				ATT_GAIN_STEP			0x11
0x6F	IOCTR L2	*RW*				MCLK_E N	SDOUT1_I NPUT_EN	SDOUT2_I NPUT_EN	LRCK_INP UT_EN	SCLK_INP UT_EN	0x00

Register Detailed Description

IDH: (Address 00h)				
Bit	Symbol	R/W	Description	Default
7:0	IDCODE_H	RO	Chip ID (22h) will be returned after read.	0x22

IDL: (Address 01h)				
Bit	Symbol	R/W	Description	Default
7:0	IDCODE_L	RO	Chip ID (16h) will be returned after read. All configuration registers will be reset to default value after 0xaa is written	0x16

SYSST: (Address 02h)				
Bit	Symbol	R/W	Description	Default
7	SCLK_ERRS	RO	SCLK Error status: 0: OK 1: Error	0
6	NO_MCLKS	RO	No MCLK status: 0: Normal 1: Abnormal	0
5	NO_LRCLKS	RO	No LRCLK status: 0: Normal 1: Abnormal	0
4	NO_SCLKS	RO	No SCLK status: 0: Normal 1: Abnormal	0
3	NOCLKS	RO	No Clock (SCLK or LRCLK) Status 0: Normal 1: Abnormal	0
2	CLKS	RO	Clock (PLL or MCLK) Status 0: Unstable 1: Stable	0
1	OC_FLAG34S	RO	Micbias34 OC flag: 0: not OC 1: OC	0
0	OC_FLAG12S	RO	Micbias12 OC flag: 0: not OC 1: OC	0

SYSINT: (Address 03h)				
Bit	Symbol	R/W	Description	Default
7	SCLK_ERRI	RC	Interrupt indicator for SCLK_ERRS. 0: No Interrupt 1: Interrupt	0
6	NO_MCLKI	RC	Interrupt indicator for NO_MCLKS. 0: No Interrupt 1: Interrupt	0

5	NO_LRCLKI	RC	Interrupt indicator for NO_LRCLKS. 0: No Interrupt 1: Interrupt	0
4	NO_SCLKI	RC	Interrupt indicator for NO_SCLKS. 0: No Interrupt 1: Interrupt	0
3	NOCLKI	RC	Interrupt indicator for NOCLKS. 0: No Interrupt 1: Interrupt	0
2	CLKI	RC	Interrupt indicator for CLKS. 0: No Interrupt 1: Interrupt	0
1	OC_FLAG34I	RC	Interrupt indicator for FLAG34S. 0: No Interrupt 1: Interrupt	0
0	OC_FLAG12I	RC	Interrupt indicator for FLAG12S. 0: No Interrupt 1: Interrupt	0

SYSINTM: (Address 04h)

Bit	Symbol	R/W	Description	Default
7	SCLK_ERRM	RW	Interrupt mask for SCLK_ERRI 0: Not Mask 1: Mask	1
6	NO_MCLKM	RW	Interrupt mask for NO_MCLKI 0: Not Mask 1: Mask	1
5	NO_LRCLKM	RW	Interrupt mask for NO_LRCLKI 0: Not Mask 1: Mask	1
4	NO_SCLKM	RW	Interrupt mask for NOSCLKI 0: Not Mask 1: Mask	1
3	NOCLKM	RW	Interrupt mask for NOCLKI 0: Not Mask 1: Mask	1
2	CLKM	RW	Interrupt mask for CLKI 0: Not Mask 1: Mask	1
1	OC_FLAG34M	RW	Interrupt mask for OC_FLAG34I. 0: Not Mask 1: Mask	1
0	OC_FLAG12M	RW	Interrupt mask for OC_FLAG12I. 0: Not Mask 1: Mask	1

SYSCTRL1: (Address 06h)

Bit	Symbol	R/W	Description	Default

7	VOL_CZBYP	RW	Volume cross zero option: 0: Cross Zero 1: Do not cross zero	0
6	CH_SUM_SUB_EN	RW	When CH_SUM is setting 2'b01, Sub enable: 0: Disable 1: Enable	0
5	INTN	RW	Interrupt pad INTN pin-source selection 0: SYSINT 1: SYSST	0
4	I2S_EN	RW	I2S Interface Enable: 0: Disable 1: Enable	0
3:2	CH_SUM	RW	Channels Sum mixer Mode: 00: Disable Sum mixer mode 01: ch1=ch2=(ch1+ch2)/2; ch3=ch4=(ch3+ch4)/2 10: ch1=ch2=ch3=ch4=(ch1+ch2+ch3+ch4)/4 11: Reserved	0
1	SYSCE	RW	System Clock (MCLK or PLL) Enable 0: Disable 1: Enable	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	1

SYSCTRL2: (Address 07h)

Bit	Symbol	R/W	Description	Default
7:6	I2C_WEN	RW	I2C Write Enable: 10: Write enable others：Write disable	0
5	CH4_EN	RW	Digital Data-path Enable for Channel4 0: Disable 1: Enable	1
4	CH3_EN	RW	Digital Data-path Enable for Channel3 0: Disable 1: Enable	1
3	CH2_EN	RW	Digital Data-path Enable for Channel2 0: Disable 1: Enable	1
2	CH1_EN	RW	Digital Data-path Enable for Channel1 0: Disable 1: Enable	1
1	Reserved	RW	Not used	0
0	Reserved	RW	Not used	1

CHCTRL1: (Address 08h)

Bit	Symbol	R/W	Description	Default
7	CH1_HAGCE	RW	CH1 Disable/Enable Hardware Automatic Gain Control module 0: Disable 1: Enable	0

6	CH1_HDCCE	RW	Channel 1 Hardware DC cancelation unit (Which is HPF filter) Enable: 0: Disable 1: Enable	1
5	CH1_HMUTE	RW	CH1 Disable/Enable Hardware mute module 0: Disable 1: Enable	1
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2:0	Reserved	RW	Not used	0

CHCTRL2: (Address 09h)

Bit	Symbol	R/W	Description	Default
7	CH2_HAGCE	RW	CH2 Disable/Enable Hardware Automatic Gain Control module 0: Disable 1: Enable	0
6	CH2_HDCCE	RW	Channel 2 Hardware DC cancelation unit (Which is HPF filter) Enable: 0: Disable 1: Enable	1
5	CH2_HMUTE	RW	CH2 Disable/Enable Hardware mute module 0: Disable 1: Enable	1
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2:0	Reserved	RW	Not used	0

CHCTRL3: (Address 0Ah)

Bit	Symbol	R/W	Description	Default
7	CH3_HAGCE	RW	CH3 Disable/Enable Hardware Automatic Gain Control module 0: Disable 1: Enable	0
6	CH3_HDCCE	RW	Channel 3 Hardware DC cancelation unit (Which is HPF filter) Enable: 0: disable 1: enable	1
5	CH3_HMUTE	RW	CH3 Disable/Enable Hardware mute module 0: Disable 1: Enable	1
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2:0	Reserved	RW	Not used	0

CHCTRL4: (Address 0Bh)

Bit	Symbol	R/W	Description	Default
7	CH4_HAGCE	RW	CH4 Disable/Enable Hardware Automatic Gain Control module	0

			0: Disable 1: Enable	
6	CH4_HDCCE	RW	Channel 4 Hardware DC cancelation unit (Which is HPF filter) Enable: 0: Disable 1: Enable	1
5	CH4_HMUTE	RW	CH4 Disable/Enable Hardware mute module 0: Disable 1: Enable	1
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2:0	Reserved	RW	Not used	0

VOLCTRL1: (Address 0Ch)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:4	CH1_VOL_UP	RW	Channel1 vol positive gain (differential input Application): 000: 0 dB 001: 6 dB 010: 12 dB … 101: 30 dB others: Reserved Channel1 vol positive gain (single-end input Application): 000: -6 dB 001: 0 dB 010: 6 dB … 101: 24 dB others: Reserved	1
3:0	CH1_VOL_DOWN_INT	RW	Channel1 vol int negative gain: 0000: 0 dB 0001: -6 dB 0010: -12 dB … 1111:-90 dB	0

VOLCTRL2: (Address 0Dh)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5:0	CH1_VOL_DOWN_FRAC	RW	Channel1 vol fraction negative gain: 000000: 0 dB 000001: -0.09407 dB 000010: -0.1881 dB … 111111:-5.9264 dB	63

VOLCTRL3: (Address 0Eh)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:4	CH2_VOL_UP	RW	Channel2 vol positive gain (differential input Application): 000: 0 dB 001: 6 dB 010: 12 dB … 101: 30 dB others: Reserved Channel2 vol positive gain (single-end input Application): 000: -6 dB 001: 0 dB 010: 6 dB … 101: 24 dB others: Reserved	1
3:0	CH2_VOL_DOWN_INT	RW	Channel2 vol int negative gain: 0000: 0 dB 0001: -6 dB 0010: -12 dB … 1111:-90 dB	0

VOLCTRL4: (Address 0Fh)				
Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5:0	CH2_VOL_DOWN_FRAC	RW	Channel2 vol fraction negative gain: 000000: 0 dB 000001: -0.09407 dB 000010: -0.1881 dB … 111111:-5.9264 dB	63

VOLCTRL5: (Address 10h)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:4	CH3_VOL_UP	RW	Channel3 vol positive gain (differential input Application): 000: 0 dB 001: 6 dB 010: 12 dB … 101: 30 dB others: Reserved Channel3 vol positive gain (single-end input Application):	1

			000: -6 dB 001: 0 dB 010: 6 dB … 101: 24 dB others: Reserved	
3:0	CH3_VOL_DOWN_INT	RW	Channel3 vol int negative gain: 0000: 0 dB 0001: -6 dB 0010: -12 dB … 1111:-90 dB	0

VOLCTRL6: (Address 11h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RW	Not used	0
5:0	CH3_VOL_DOWN_FRAC	RW	Channel3 vol fraction negative gain: 000000: 0 dB 000001: -0.09407 dB 000010: -0.1881 dB … 111111:-5.9264 dB	63

VOLCTRL7: (Address 12h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6:4	CH4_VOL_UP	RW	Channel4 vol positive gain (differential input Application): 000: 0 dB 001: 6 dB 010: 12 dB … 101: 30 dB others: Reserved Channel4 vol positive gain (single-end input Application): 000: -6 dB 001: 0 dB 010: 6 dB … 101: 24 dB others: Reserved	1
3:0	CH4_VOL_DOWN_INT	RW	Channel4 vol int negative gain: 0000: 0 dB 0001: -6 dB 0010: -12 dB … 1111:-90 dB	0

VOLCTRL8: (Address 13h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**

7:6	Reserved	RW	Not used	0
5:0	CH4_VOL_DOWN_FRAC	RW	Channel4 vol fraction negative gain: 000000: 0 dB 000001: -0.09407 dB 000010: -0.1881 dB ... 111111:-5.9264 dB	63

I2SCTRL1: (Address 20h)

Bit	Symbol	R/W	Description	Default
7	I2S_CLK_MODE	RW	I2S clock mode: 0: Slaver mode 1: Master mode	0
6:5	Reserved	RW	Not used	0
4:0	I2SSR	RW	I2S sample rate configuration: 00000: 8 kHz 00001: 11 kHz 00010: 12 kHz 00011: 16 kHz 00100: 22 kHz 00101: 24 kHz 00110: 32 kHz 00111: 44 kHz 01000: 48 kHz 01001: 64kHz 01010: 88kHz 01011: 96kHz 01100: 128kHz 01101: 176kHz 01110: 192kHz 01111: 256kHz 10000: 352kHz 10001: 384kHz 10010: 512 kHz 10011: 705kHz 10100: 768kHz Others: Reserved	8

I2SCTRL2: (Address 21h)

Bit	Symbol	R/W	Description	Default
7:6	I2S_FR_PLS_TYP	RW	I2S frame pulse type: 00: one-slot 01: one-SCLK 10: 50% duty cycle of Frame 11: Reserved	0
5	I2S_LRCLK_INV	RW	I2S word clock invert state: 0: Not Invert 1: Invert	0
4	I2S_SCLK_IPN	RW	Whether the leading edge of the frame/data are synchronized with the rising/falling edge of SCLK (bit clock), for the I2S input signals (exclude SCLK) of the ADC:	1

			0: Negedge 1: Posdege	
3	I2S_SCLK_OPN	RW	Whether the leading edge of the frame/data are synchronized with the rising/falling edge of SCLK (bit clock), for the I2S output signals (exclude SCLK) of the ADC: 0: Negedge 1: Posdege	0
2	Reserved	RW	Not used	0
1:0	I2S_JUSTIF_TYP	RW	00: Left-justified 01: Right-justified	0

I2SCTRL3: (Address 22h)

Bit	Symbol	R/W	Description	Default
7	I2S_DOHZ	RW	I2S DATAO1/DATAO2 output config2: 0: The bits without used will output 0 1: The bits without used will output HiZ	0
6:0	I2S_LRCLK_SL	RW	I2S word clock shift left relative DATAO: 0000000: 0 SCLKs offset 0000001: 1 SCLKs offset 0000010: 2 SCLKs offset ... 1111111: 127 SCLKs offset	0

I2SCTRL4: (Address 23h)

Bit	Symbol	R/W	Description	Default
7	I2S_LRCLK_SR	RW	LRCLK shift right relative DATAO: 0: 0 SCLK cycle 1: 1 SCLK Cycle	0
6:0	I2S_WORD_WIDTH	RW	I2S word width configuration:(real word-width is I2S_WORD_WIDTH+1) 0000000~00000110: Reserved 0000111: 8 SCLKs/slot 0001000: 9 SCLKs/slot ... 1111111: 128 SCLKs/slot	31

I2SCTRL5: (Address 24h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4:0	I2S_BIT_DEPTH	RW	I2S data resolution selection (I2S_BIT_DEPTH <= I2S_WORD_WIDTH), The real bit-depth is I2S_BIT_DEPTH+1: 00000~00110: Reserved 00111: 8 bits/slot 01000: 9 bits/slot ... 11111: 32 bits/slot	31

I2SCTRL6: (Address 25h)

Bit	Symbol	R/W	Description	Default

7:5	I2S_CHANNELS	RW	I2S TDM mode control: 000: I2S mode (TDM2s) 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: Reserved	0
4	I2S_TX_SDOUT2_EN	RW	I2S transmitter Unit PAD DATAO2 enable/disable: 0: Disable 1: Enable	1
3	I2S_TX_SDOUT1_EN	RW	I2S transmitter Unit PAD DATAO1 enable/disable: 0: Disable 1: Enable	1
2	I2S_SLOT_DOHZ	RW	I2S DATAO1/DATAO2 output config1: 0: The slots without used will output 0 1: The slots without used will output HiZ	1
1	I2S_TX_EN	RW	I2S transmitter Unit enable/disable: 0: Disable 1: Enable	0
0	I2S_CASCADE_MD	RW	I2S DATAO1/DATAO2 daisy chain mode enable: 0: Disable 1: Enable	0

I2SCTRL7: (Address 26h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4:0	I2S_CH1_SLOTVLD	RW	The index of i2s slot, which channel1 data transmitted on: 0~31: slot0~31	0

I2SCTRL8: (Address 27h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4:0	I2S_CH2_SLOTVLD	RW	The index of i2s slot, which channel2 data transmitted on: 0~31: slot0~31	1

I2SCTRL9: (Address 28h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4:0	I2S_CH3_SLOTVLD	RW	The index of i2s slot, which channel3 data transmitted on: 0~31: slot0~31	16

I2SCTRL10: (Address 29h)

Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0

4:0	I2S_CH4_SLOTVLD	RW	The index of i2s slot, which channel4 data transmitted on: 0~31: slot0~31	17

FLTCTRL1: (Address 2Dh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	1
6	HBF_PHASE_CTRL	RW	Low-Latency Filter enable: 0: Low-latency Filter 1: Near-linear Filter	1
5	Reserved	RW	Not used	0
4:3	Reserved	RW	Not used	0
2:0	Reserved	RW	Not used	3

PDMCTRL: (Address 2Eh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RW	Not used	0
5	Reserved	RW	Not used	0
4	PDM_MD	RW	PDM Mode (PDM code transmit by MIC1P&MIC3P): 0: Analog MIC 1: Digital MIC	0
3	PDM12_EDGE	RW	DMIC_CLK latching edge used for channel 1 and channel 2 data: 0: Channel-1 latched on the negative， Channel-2 inverse 1: Channel-1 latched on the posedge， Channel-2 inverse	0
2	PDM34_EDGE	RW	DMIC_CLK latching edge used for channel 3 and channel 4 data: 0: Channel-3 latched on the negative， Channel-4 inverse 1: Channel-3 latched on the posedge， Channel-4 inverse	0
1:0	DMIC_CLK_SEL	RW	DMIC clock select: 00: 768kHz 01: 1.562MHz 10: 3.072MHz 11: 6.144MHz	2

ADC1CTRL2: (Address 31h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	0
5:0	PGA1_GAINSEL	RW	corresponding CH1 PGA Gain select: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB	0

			101001: 35dB 101010: 36dB others: Reserved	

ADC2CTRL2: (Address 33h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	0
5:0	PGA2_GAINSEL	RW	corresponding CH2 PGA Gain select: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB 101001: 35dB 101010: 36dB others: Reserved	0

ADC3CTRL2: (Address 35h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	0
5:0	PGA3_GAINSEL	RW	corresponding CH3 PGA Gain select: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB 101001: 35dB 101010: 36dB others: Reserved	0

ADC4CTRL2: (Address 37h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	0
5:0	PGA4_GAINSEL	RW	corresponding CH4 PGA Gain select: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB 101001: 35dB 101010: 36dB others: Reserved	0

ADCSCTRL5: (Address 3Ch)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	Reserved	RW	Not used	0
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2	SDM_PDIREF	RW	ADC 2CH current reference power down: 0: normal work (default) 1: power down	1
1:0	Reserved	RW	Not used	0

ADCSCTRL6: (Address 3Dh)				
Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	Reserved	RW	Not used	0
4	Reserved	RW	Not used	0
3	Reserved	RW	Not used	0
2	VCM_FSTUP	RW	VMID fast-up enable: 0: fast-up disable (default) 1: fast-up enable	0
1	VCM_EN	RW	VMID enable: 0: Disable 1: Enable (default)	0
0	Reserved	RW	Not used	0

ADCSCTRL7: (Address 3Eh)				
Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Not used	0
0	CH12_ADC_CLKEN	RW	ADC channel 1&2 clock enable： 0: Disable 1: Enable	0

ADCSCTRL8: (Address 3Fh)				
Bit	Symbol	R/W	Description	Default
7:1	Reserved	RW	Not used	0
0	CH34_ADC_CLKEN	RW	ADC channel 3&4 clock enable： 0: Disable 1: Enable	0

MICBIAS12CTRL1: (Address 40h)				
Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5:2	MICB12_SEL	RW	corresponding MICBIAS output select: 0000~1111: 1.7~2.45V, 50mV step (default 1000: 2.1V)	0
1	MICB12_FST	RW	corresponding MICBIAS fast-up enable: 0: Fast-up enable (default) 1: Fast-up disabled	0

0	MICB12_PWD	RW	corresponding MICBIAS Power down 0: Normal work 1: Power down	1

MICBIAS34CTRL1: (Address 42h)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RW	Not used	0
5:2	MICB34_SEL	RW	corresponding MICBIAS output select: 0000~1111: 1.7~2.45V, 50mV step (default 1000: 2.1V)	0
1	MICB34_FST	RW	corresponding MICBIAS fast-up enable: 0: Fast-up enable (default) 1: Fast-up disabled	0
0	MICB34_PWD	RW	corresponding MICBIAS Power down 0: Normal work 1: Power down	1

PLL_CTRL2: (Address 45h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6	PLL_PD	RW	PLL power down: 0: Working 1: Power Down	1
5	Reserved	RW	Not used	0
4	Reserved	RW	Not used	0
3:0	Reserved	RW	Not used	0

PLL_CTRL6: (Address 49h)

Bit	Symbol	R/W	Description	Default
7:6	IPLL	RW	PLL reference clock selection 00: SCLK 01: LRCLK 10: OSC 11: MCLK	0
5:2	MCLK_FREQ_SEL	RW	MCLK frequency select, if need more complex clock application, ADC can use programable PLL(PLL_DBG). : 0000: 1.536MHz @48kHz; 1.4112MHz @44.1kHz; 1.024MHz @32kHz; 0001: 3.072MHz @48kHz; 2.8224MHz @44.1kHz; 2.048MHz @32kHz; 0010: 6.144MHz @48kHz; 5.6448MHz @44.1kHz; 4.096MHz @32kHz; 0011: 12MHz 0100: 12.288MHz @48kHz; 11.2896MHz @44.1kHz; 8.192MHz @32kHz; 0101: 13MHz 0110: 16MHz 0111: 19.2MHz 1000: 19.68MHz 1001: 24MHz 1010: 24.576MHz @48kHz; 22.5792MHz @44.1kHz; 16.384MHz @32kHz; Others: Reserved	4

1:0	Reserved	RW	Not used	0

MISCCTRL2: (Address 4Ch)

Bit	Symbol	R/W	Description	Default
7:4	Reserved	RW	Not used	8
3	LDO_LP_EN	RW	Digital LDO low power mode EN 0: Normal power 1: Low power	1
2	BG_V2I_EN	RW	BG V2I enable (PLL, OSC, MICBIAS bias) 0: Disable 1: Enable	0
1:0	Reserved	RW	Not used	0

ANA_SYSCTRL: (Address 4Fh)

Bit	Symbol	R/W	Description	Default
7	PGA4_PD	RW	corresponding CH4 PGA Power down 0: Normal work 1: Power down	1
6	PGA3_PD	RW	corresponding CH4 PGA Power down 0: Normal work 1: Power down	1
5	PGA2_PD	RW	corresponding CH3 PGA Power down 0: Normal work 1: Power down	1
4	PGA1_PD	RW	corresponding CH2 PGA Power down 0: Normal work 1: Power down	1
3	SDM4_PD	RW	corresponding CH4 ADC Core Power Down: 0: Normal work 1: Power down	1
2	SDM3_PD	RW	corresponding CH4 ADC Core Power Down: 0: Normal work 1: Power down	1
1	SDM2_PD	RW	corresponding CH3 ADC Core Power Down: 0: Normal work 1: Power down	1
0	SDM1_PD	RW	corresponding CH2 ADC Core Power Down: 0: Normal work 1: Power down	1

CH1_DLY: (Address 50h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	CH1_FRAC_DLY2	RW	Channel1 fraction2 delay: Delay = N*5.21us	0
4:0	CH1_FRAC_DLY1	RW	Channel1 fraction1 delay: Delay = N*162.76ns	0

CH2_DLY: (Address 51h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0

6:5	CH2_FRAC_DLY2	RW	Channel2 fraction2 delay: Delay = N*5.21us	0
4:0	CH2_FRAC_DLY1	RW	Channel2 fraction1 delay: Delay = N*162.76ns	0

CH3_DLY: (Address 52h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	CH3_FRAC_DLY2	RW	Channel3 fraction2 delay: Delay = N*5.21us	0
4:0	CH3_FRAC_DLY1	RW	Channel3 fraction1 delay: Delay = N*162.76ns	0

CH4_DLY: (Address 53h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:5	CH4_FRAC_DLY2	RW	Channel4 fraction2 delay: Delay = N*5.21us	0
4:0	CH4_FRAC_DLY1	RW	Channel4 fraction1 delay: Delay = N*162.76ns	0

HDCC_COEF1: (Address 54h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:4	CH2_ALPHA_HDCC	RW	Alpha coefficient for CH2 HDCC module value = ALPHA_HDCC + 8	4
3	Reserved	RW	Not used	0
2:0	CH1_ALPHA_HDCC	RW	Alpha coefficient for CH1 HDCC module value = ALPHA_HDCC + 8	4

HDCC_COEF2: (Address 55h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	1
6:4	CH4_ALPHA_HDCC	RW	Alpha coefficient for CH4 HDCC module value = ALPHA_HDCC + 8	4
3	Reserved	RW	Not used	0
2:0	CH3_ALPHA_HDCC	RW	Alpha coefficient for CH3 HDCC module value = ALPHA_HDCC + 8	4

ANASTA1: (Address 5Ah)

Bit	Symbol	R/W	Description	Default
7:6	Reserved	RO	Not used	0
5:0	PGA1_GAINSEL_ST	RO	The status of PGA1 Gain: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB	0

			101001: 35dB 101010: 36dB others: Reserved	

ANASTA2: (Address 5Bh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	PGA2_GAINSEL_ST	RO	The status of PGA2 Gain: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB 101001: 35dB 101010: 36dB others: Reserved	0

ANASTA3: (Address 5Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	PGA3_GAINSEL_ST	RO	The status of PGA3 Gain: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB 101001: 35dB 101010: 36dB others: Reserved	0

ANASTA4: (Address 5Dh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7:6	Reserved	RO	Not used	0
5:0	PGA4_GAINSEL_ST	RO	The status of PGA4 Gain: 000000: -6dB 000001: -5dB 000010: -4dB ... 000110: 0dB ... 101000: 34dB 101001: 35dB 101010: 36dB others: Reserved	0

AGC_CTRL1: (Address 60h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
7	Reserved	RW	Not used	0

6	Reserved	RW	Not used	0
5	Reserved	RW	Not used	0
4	Reserved	RW	Not used	0
3:0	AGC_MAX_GAIN	RW	Upper limit of gain in dB for signal below target level AGC_MAX_GAIN=(3+n*3) dB 0000:3dB 0001:6dB 0010:9dB ..... 1011:36dB 1100:36dB 1111:36dB	11

AGC_CTRL2: (Address 61h)

Bit	Symbol	R/W	Description	Default
7:0	AGC_NOISE_TH	RW	Attack Amplitude threshold, in percent of signal full scale dB=20*log10(AGC_NOISE_TH*2^5/2^21) 00000000:-Inf dB 00000001: -96.33dB 00000010: -90.309dB 11111111:-48.199dB	16

AGC_CTRL3: (Address 62h)

Bit	Symbol	R/W	Description	Default
7:0	AGC_ATT_TH	RW	Attack Amplitude threshold, in percent of signal full scale dB=20*log10(AGC_ATT_TH*2^13/2^21) 00000000:-Inf dB 00000001:-48.165dB 00000010: -42.144dB 00000011: -38.662dB 11111111:-0.034dB	9

AGC_CTRL4: (Address 63h)

Bit	Symbol	R/W	Description	Default
7:0	AGC_REL_TH	RW	Release Amplitude threshold, in percent of signal full scale dB=20*log10(AGC_REL_TH*2^13/2^21) 00000001:-Inf dB 00000001: -48.165dB 00000010: -42.144dB 00000011: -38.662dB 11111111:-0.034dB	5

AGC_CTRL6: (Address 64h)

Bit	Symbol	R/W	Description	Default

7:0	ATTH	RW	Attack time in unit of T of AGC, the unit is 20.8us 00000000: 0us 00000001:20.8us 00000010:41.6us 11111111: 5.3ms	0

AGC_CTRL8: (Address 65h)

Bit	Symbol	R/W	Description	Default
7:0	RTTH	RW	Release time in unit of AGC, the unit is 0.66ms 00000000: 0ms 00000001:0.66ms 00000010:1.32ms 11111111:168.3ms	0

AGC_CTRL9: (Address 66h)

Bit	Symbol	R/W	Description	Default
7:0	ATT_HOLDTH	RW	Attack hold time before attack control, the unit is 20.8us 00000000:0us 00000001:20.8us 00000010:41.6us 11111111: 5.3ms	2

AGC_CTRL10: (Address 67h)

Bit	Symbol	R/W	Description	Default
7:0	REL_HOLDTH	RW	Release hold time before release control, the unit is 2.6ms 00000000:0ms 00000001:2.6ms 00000010:5.2ms 11111111: 663ms	100

AGC_CTRL11: (Address 68h)

Bit	Symbol	R/W	Description	Default
7:0	NOISE_HOLDTH	RW	Release hold time before release control, the unit is 2.6ms 00000001:2.6ms 00000010:5.2ms 11111111: 663ms	50

AGC_CTRL12: (Address 69h)

Bit	Symbol	R/W	Description	Default
7	Reserved	RW	Not used	0
6:4	REL_GAIN_STEP	RW	The changing step of gain in the release process of AGC 000：Reserved 001:1dB/step 010:2dB/step	1

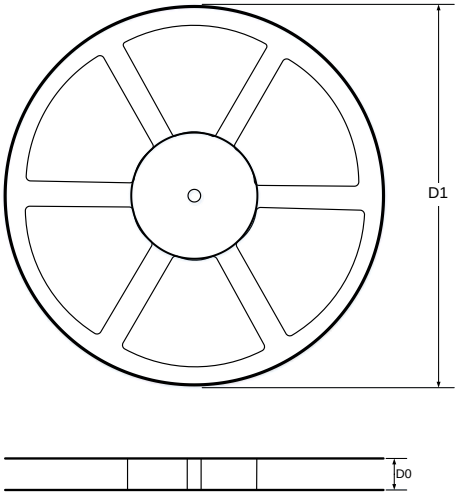
			…… 111:7dB/step	
3	Reserved	RW	Not used	0
2:0	ATT_GAIN_STEP	RW	The changing step of gain in the attack process of AGC 000: Reserved 001:1dB/step 010:2dB/step …… 111:7dB/step	1

IOCTRL2: (Address 6Fh)

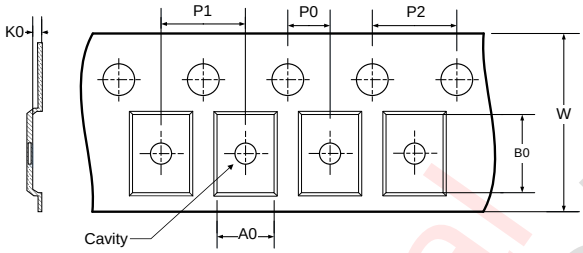
Bit	Symbol	R/W	Description	Default
7:5	Reserved	RW	Not used	0
4	MCLK_EN	RW	MCLK IO EN 0: Disable 1: Enable	0
3	SDOUT1_INPUT_EN	RW	I2S DATAO1 input Enable: 0: Disable 1: Enable	0
2	SDOUT2_INPUT_EN	RW	I2S DATAO2 input Enable: 0: Disable 1: Enable	0
1	LRCK_INPUT_EN	RW	I2S LRCLK IO input Enable: 0: Disable 1: Enable	0
0	SCLK_INPUT_EN	RW	I2S SCLK IO input Enable: 0: Disable 1: Enable	0

Tape and Reel Information

REEL DIMENSIONS

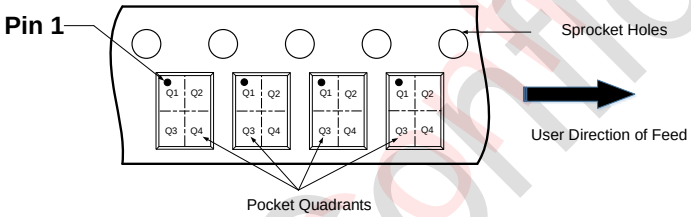


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



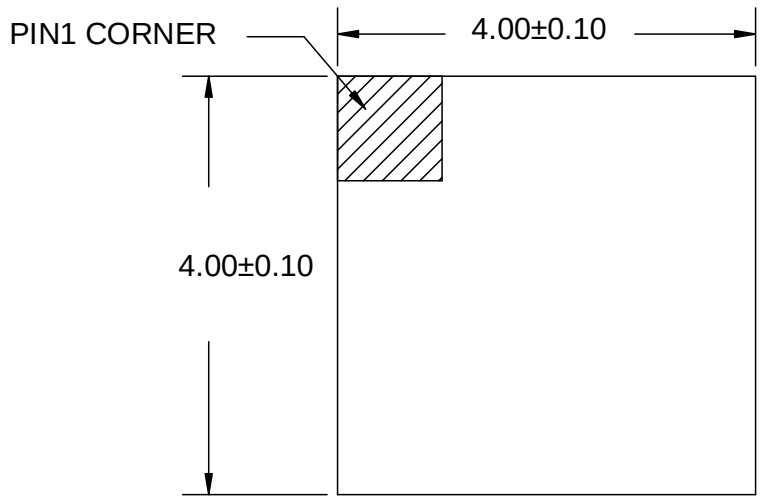
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

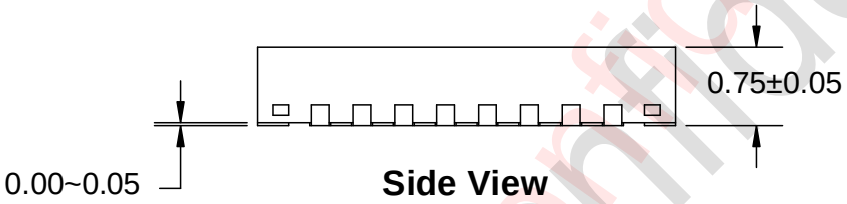
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2	8	4	12	Q1

All dimensions are nominal

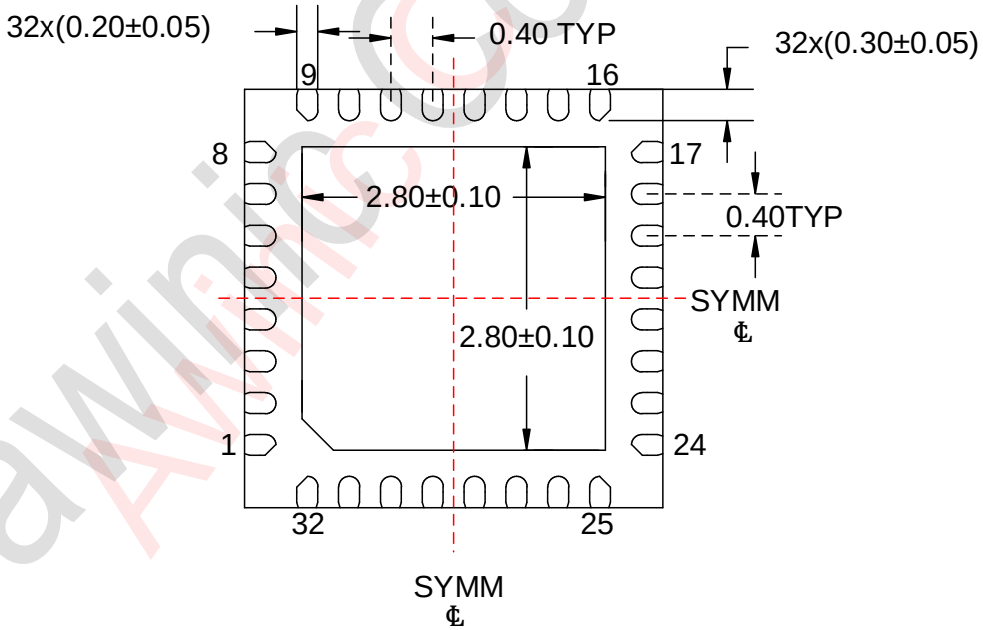
Package Description



Top View



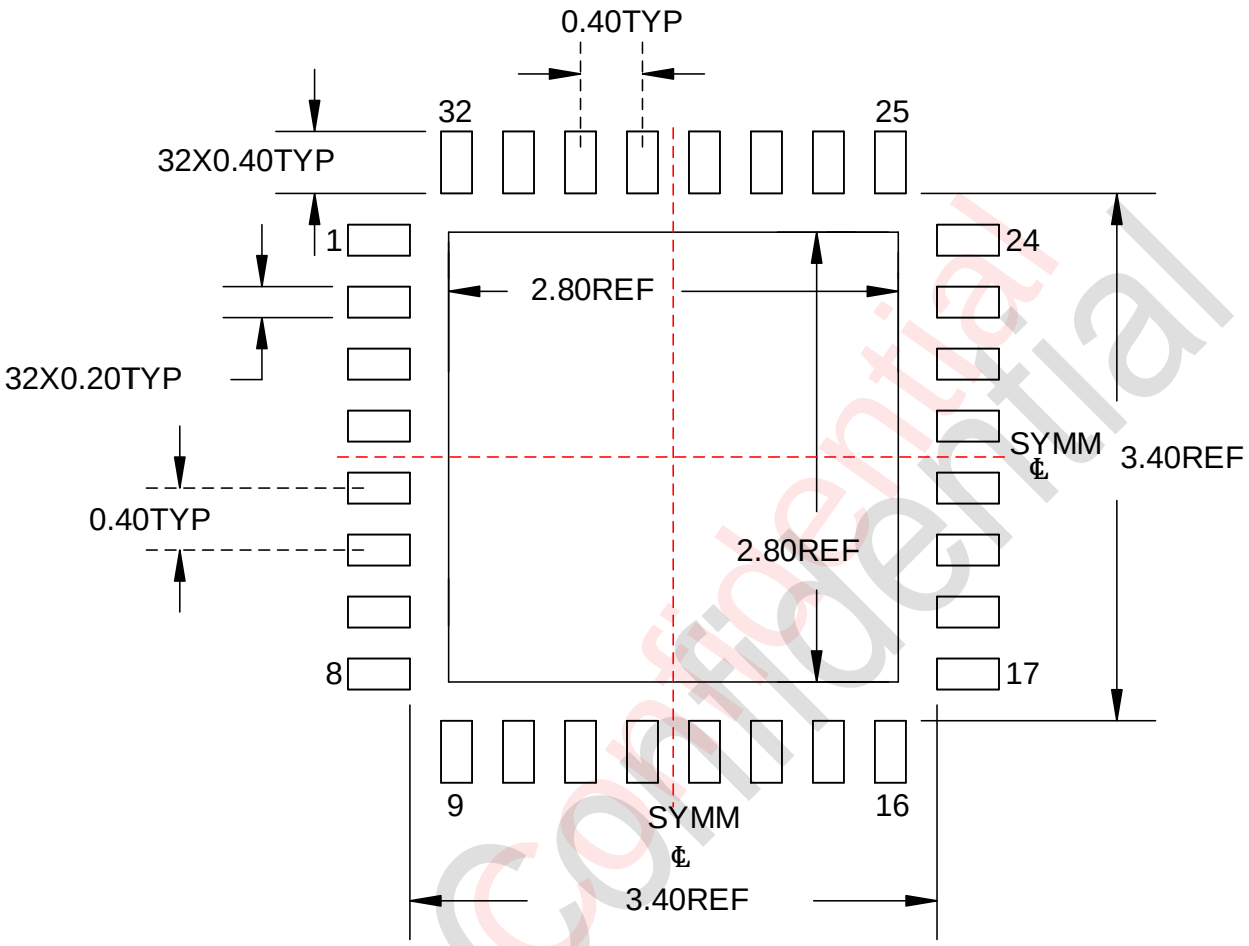
Side View

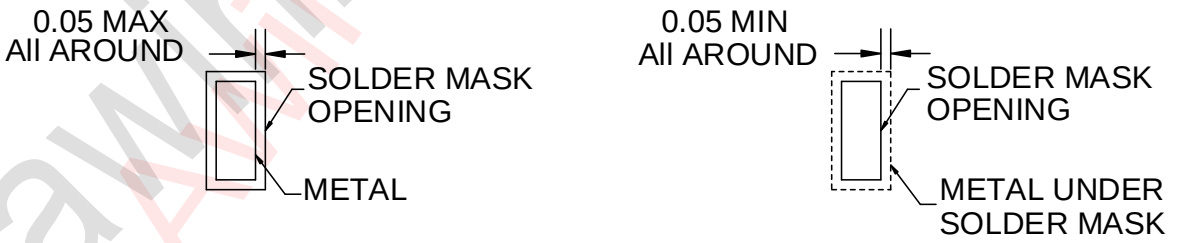


Bottom View

Unit:mm

Land Pattern Data





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Changed Record
V1.0	Nov. 2024	Officially released
V1.1	Apr. 2025	1、 Updated register detailed description； 2、 Updated Note；
V1.2	Jun. 2025	Updated description

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