12V Dual N-Channel MOSFET

Features

- Low source-source on resistance
- $R_{SS(ON)}$ Typ.= 2.20mΩ (V_{GS}= 4.5V)
- Common-Drain type
- ESD Diode-Protected Gate
- 2kV ESD HBM
- Pb-Free, Halogen Free and RoHS compliance

Applications

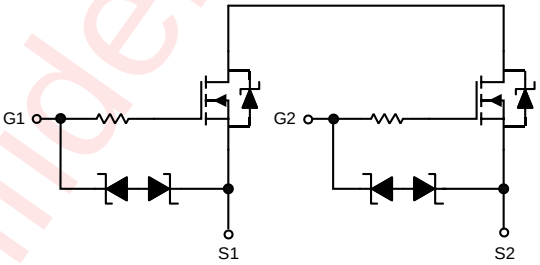
- WLCSP 2.98X1.49 - 10L

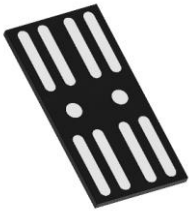
Applications

- Battery protection switch
- Mobile device battery charging and discharging

General Description

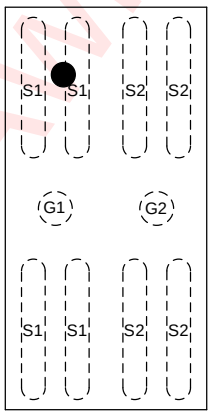
V_{SS}	$R_{SS(ON)}$ Max.
12V	2.95 mΩ @ V_{GS}= 4.5V
	3.35 mΩ @ V_{GS}= 3.8V
	4.20 mΩ @ V_{GS}= 3.1V
	6.10 mΩ @ V_{GS}= 2.5V



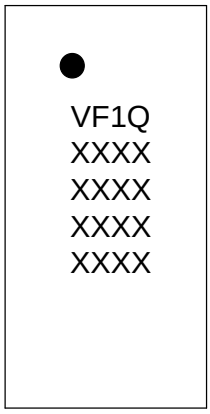


Pin Configuration and Top Mark

AW401005QCSR
(Top View)



AW401005QCSR Marking
(Top View)



VF1Q---AW401005QCSR
XXXX/XXXX/XXXX/XXXX---Production tracing code

Ordering Information

Part Number	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW401005QCSR	WLCSP 2.98X1.49 - 10L	VF1Q	MSL1	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE 1)

T_A= 25°C unless otherwise noted

Symbol	Parameter	Maximum	Unit
V_{SS}	Source-Source Voltage	12	V
V_{GS}	Gate-Source Voltage	±8	V
I_S	Source Current (DC) (NOTE 2)	23	A
I_{SM}	Source Current (Pulse) (NOTE 3)	92	A
P_D	Power Dissipation (NOTE 2)	2.3	W
T_J	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{ESD}	Human Body Model (NOTE 5)	±2	kV

Thermal Information

Symbol	Parameter	Condition	Value	Unit
$R_{\theta JA}$	Maximum Junction to Ambient (NOTE 2,4)	Steady-State	52.9	°C/W

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Mounted on FR-4 material with 1inch^2, 2oz. Copper.

NOTE3: PW < 10μs pulses, duty cycle 1% max.

NOTE4: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE5: HBM Standards: ESDA/JEDEC JS-001-2017.

Electrical Characteristics

T_J= 25°C for typical values (unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
STATIC PARAMETERS						
BV_{SSS}	Source - Source Breakdown Voltage	I_S= 1mA, V_{GS}= 0V(Test Circuit 1)	12	-	-	V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}= 12V, V_{GS}= 0V(Test Circuit 1)	-	-	100	nA
I_{GSS}	Gate Leakage Current	V_{SS}= 0V, V_{GS}= ±8V(Test Circuit 2)	-	-	±10	μA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{SS}= V_{GS}, I_S= 250μA(Test Circuit 3)	0.5	0.85	1.4	V
$R_{SS(ON)}$	Static Source to Source On-Resistance	V_{GS}= 4.5V, I_S= 6A(Test Circuit 4)	1.55	2.20	2.95	mΩ
		V_{GS}= 3.8V, I_S= 6A(Test Circuit 4)	1.60	2.50	3.35	mΩ
		V_{GS}= 3.1V, I_S= 6A(Test Circuit 4)	1.70	2.80	4.20	mΩ
		V_{GS}= 2.5V, I_S= 6A(Test Circuit 4)	1.90	3.60	6.10	mΩ
V_{FSS}	Forward Source to Source Voltage	I_S= 6A, V_{GS}= 0V(Test Circuit 5)	-	0.7	1.2	V
DYNAMIC PARAMETERS						
R_g	Series Gate Resistance	f= 1MHz	-	310	-	Ω
C_{iss}	Input Capacitance	V_{GS}= 0V, V_{SS}= 10V, f= 1MHz	-	2376	-	pF
C_{oss}	Output Capacitance		-	484	-	pF
C_{rss}	Reverse Transfer Capacitance		-	265	-	pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}= 0 to 4V, V_{SS}= 6V, I_S= 6A(Test Circuit 6)	-	30.6	-	nC
Q_{gs}	Gate Source Charge		-	5.6	-	nC
Q_{gd}	Gate Drain Charge		-	8.2	-	nC
$Q_{g(th)}$	Gate Charge at $V_{GS(TH)}$		-	2.9	-	nC
$t_{d(on)}$	Turn - On Delay Time	V_{GS}= 0 to 4V, V_{SS}= 6V, R_G= 3Ω, I_S= 6A(Test Circuit 7)	-	561	-	ns
t_r	Turn - On Rise Time		-	1058	-	ns
$t_{d(off)}$	Turn - Off Delay Time	V_{GS}= 4 to 0 V, V_{SS}= 6V, R_G= 3Ω, I_S= 6A(Test Circuit 7)	-	1612	-	ns
t_f	Turn - Off Fall Time		-	1854	-	ns

Typical Electrical and Thermal Characteristics

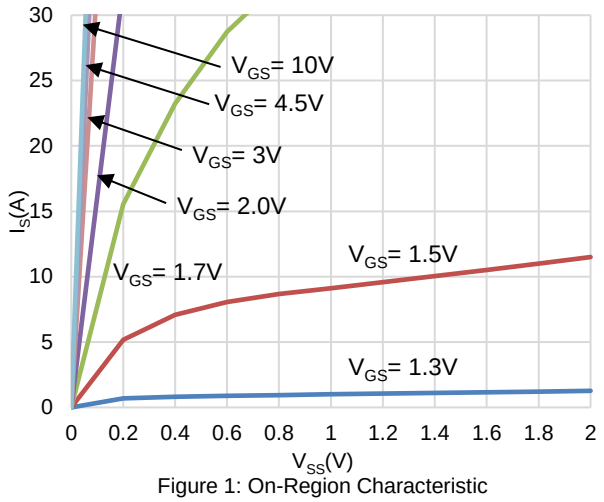


Figure 1: On-Region Characteristic

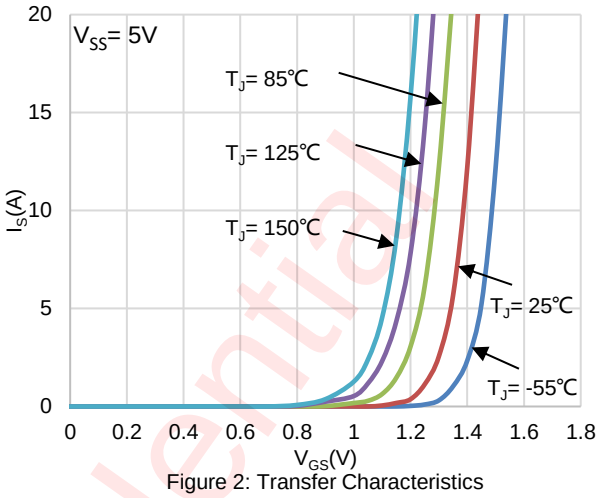


Figure 2: Transfer Characteristics

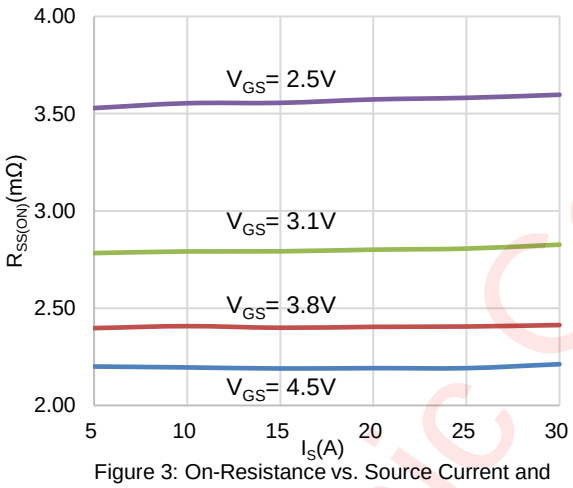


Figure 3: On-Resistance vs. Source Current and Gate Voltage

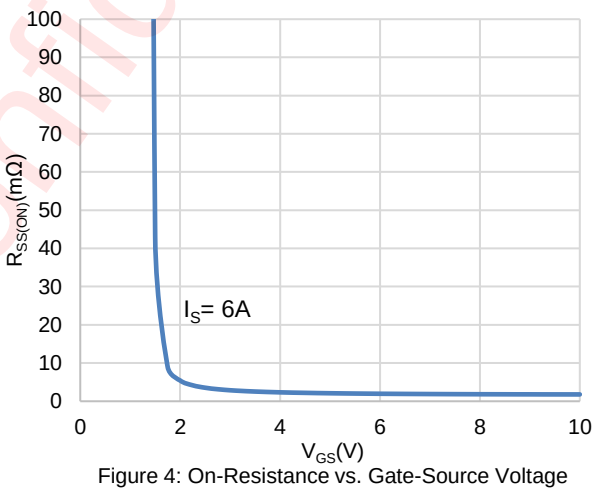


Figure 4: On-Resistance vs. Gate-Source Voltage

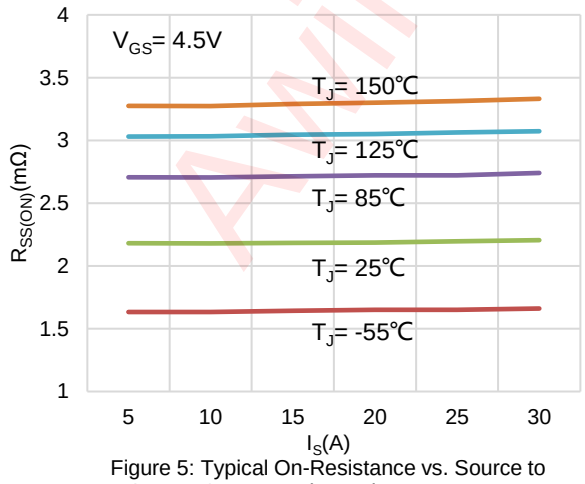


Figure 5: Typical On-Resistance vs. Source to Source Current and Junction Temperature

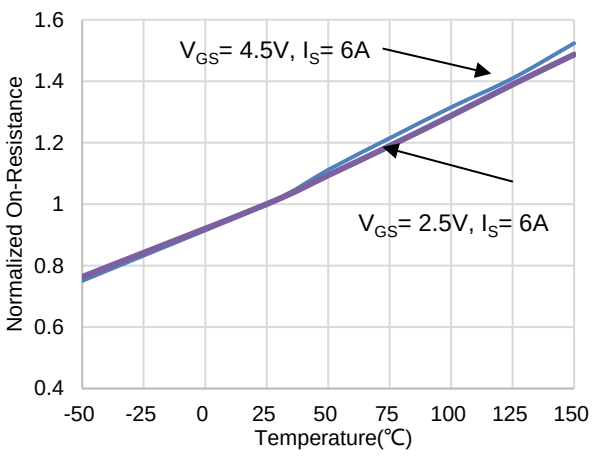


Figure 6: On-Resistance vs. Junction Temperature

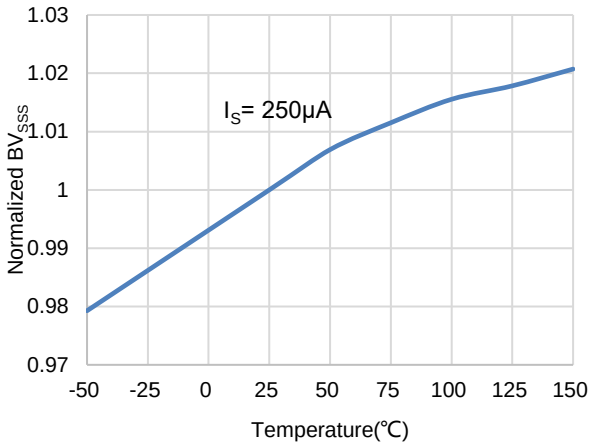


Figure 7: Source to Source Breakdown Voltage vs. Junction Temperature

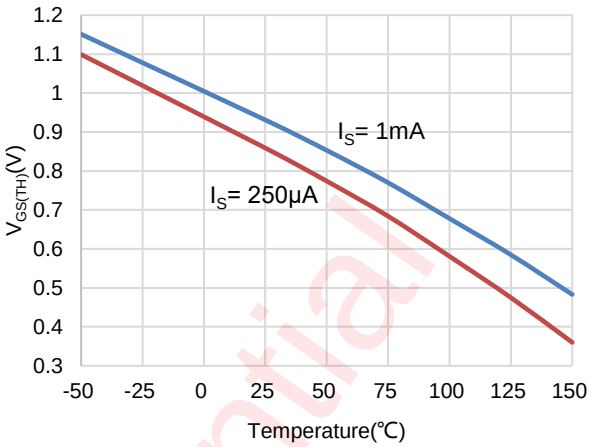


Figure 8: Gate Threshold Variation vs. Junction Temperature

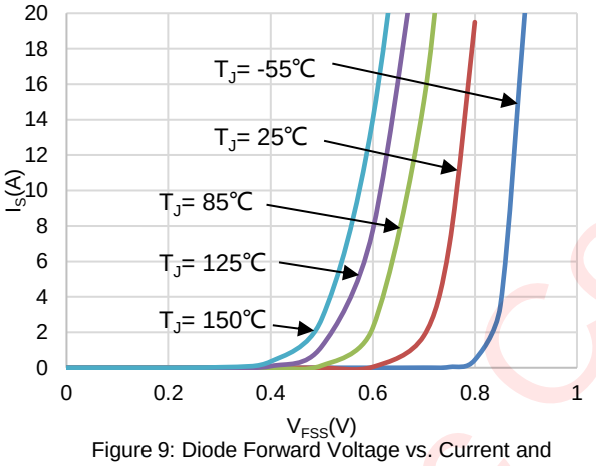


Figure 9: Diode Forward Voltage vs. Current and Temperature

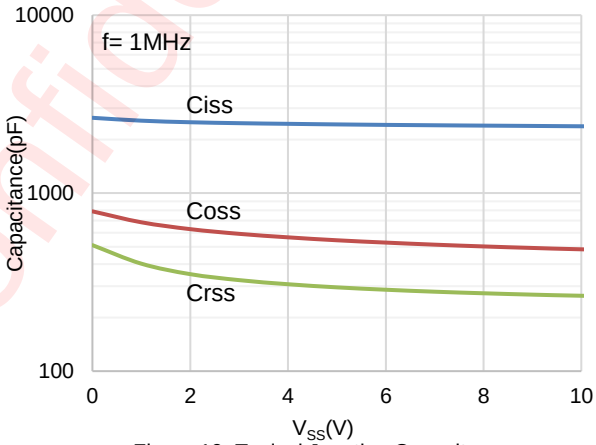


Figure 10: Typical Junction Capacitance

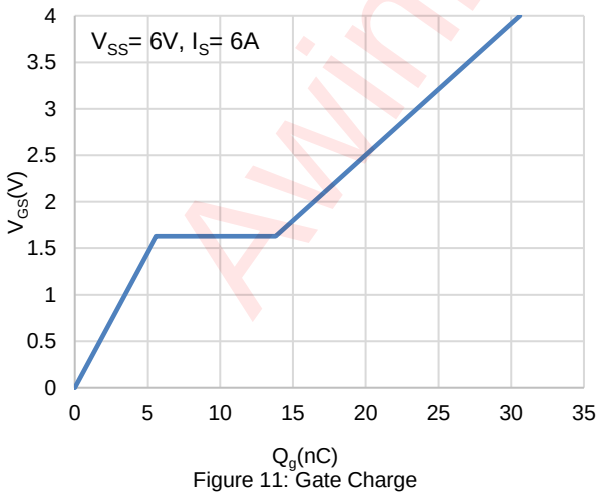


Figure 11: Gate Charge

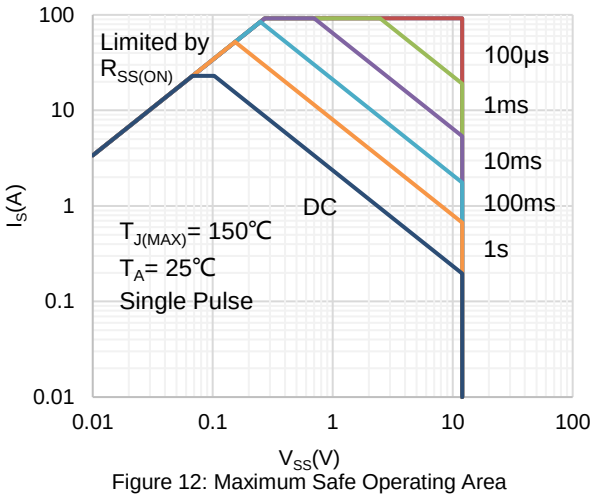


Figure 12: Maximum Safe Operating Area

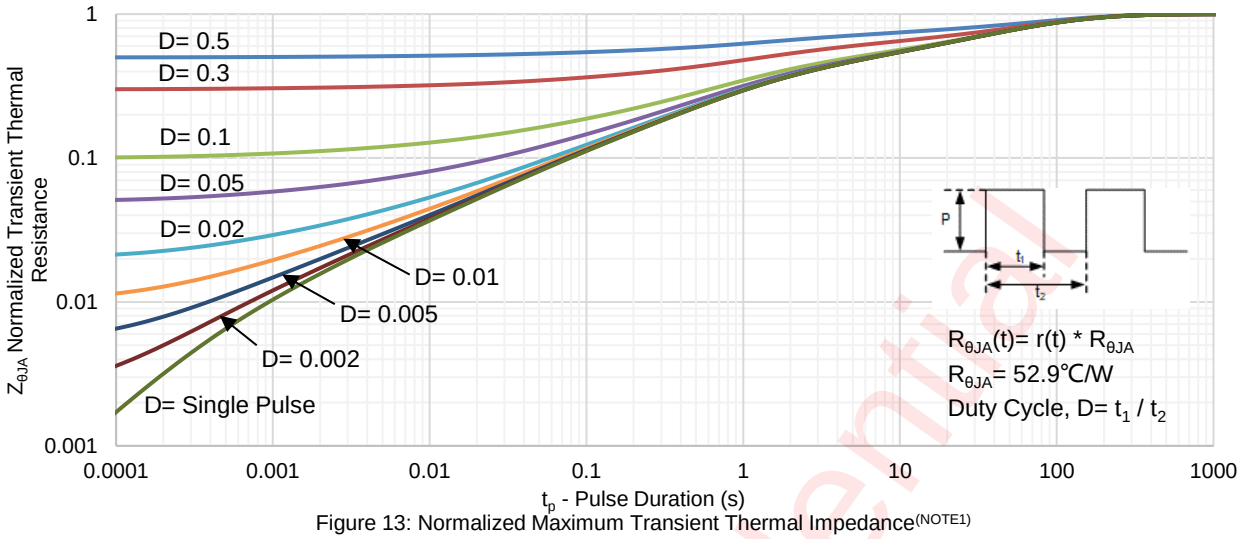
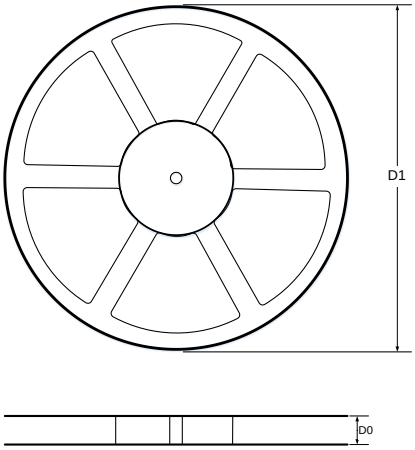


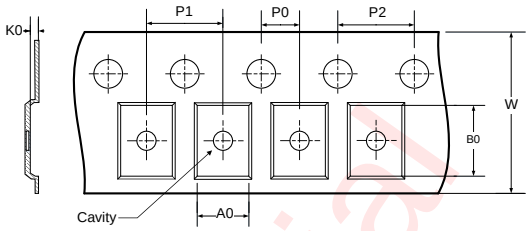
Figure 13: Normalized Maximum Transient Thermal Impedance(NOTE1)

Tape And Reel Information

REEL DIMENSIONS

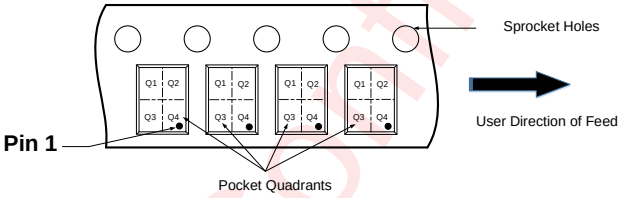


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



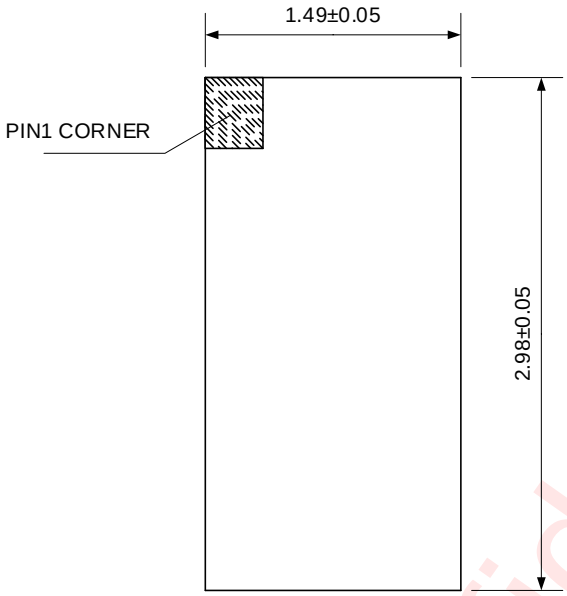
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

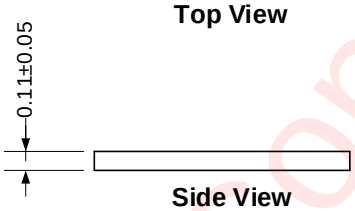
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	12	1.61	3.1	0.22	2	4	4	12	Q4

All dimensions are nominal

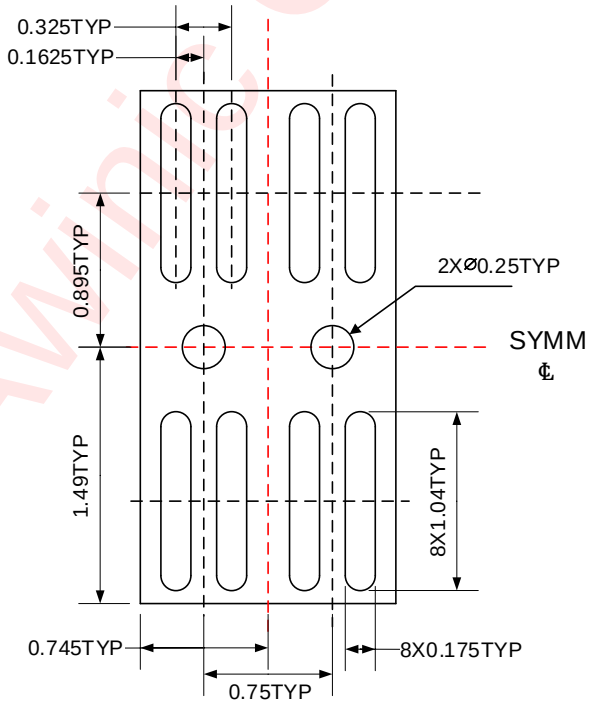
Package Description



Top View



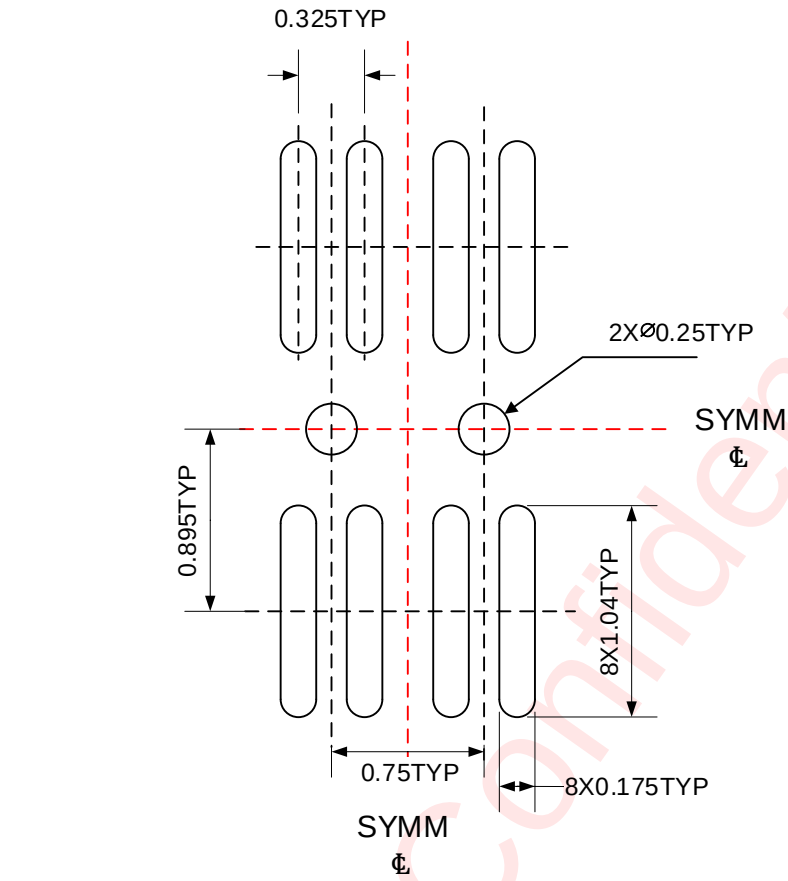
Side View

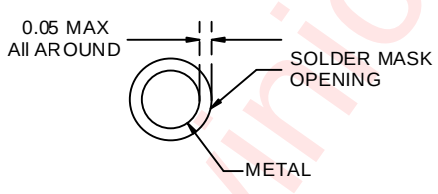


Bottom View

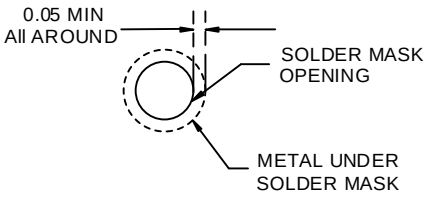
Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED



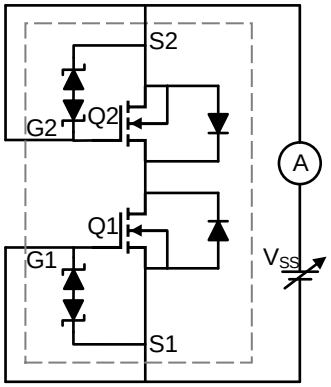
SOLDER MASK DEFINED

Unit: mm

Test Circuits

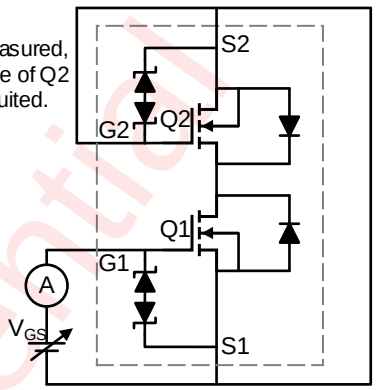
Q1 and Q2 are both measured. The test circuits are example of measuring Q1.

Test Circuit 1
BV_{SSS}/I_{SSS}



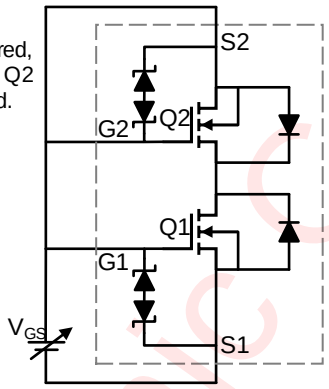
Test Circuit 2
I_{GSS}

When Q1 is measured, Gate and Source of Q2 are short-circuited.

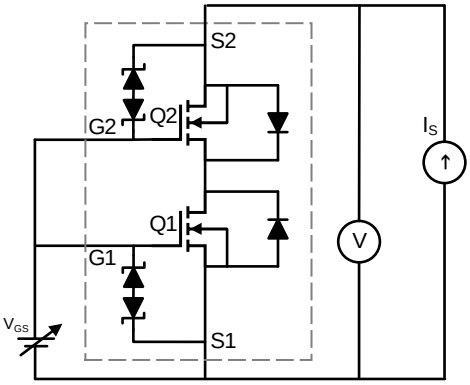


Test Circuit 3
$V_{GS(TH)}$

When Q1 is measured, Gate and Source of Q2 are short-circuited.

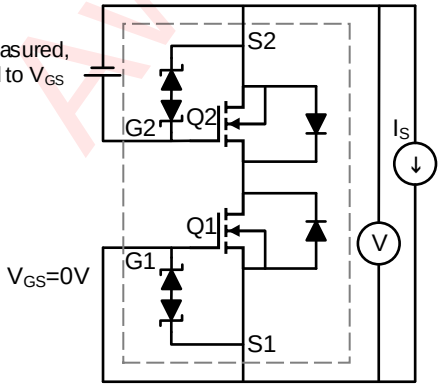


Test Circuit 4
$R_{SS(ON)}$



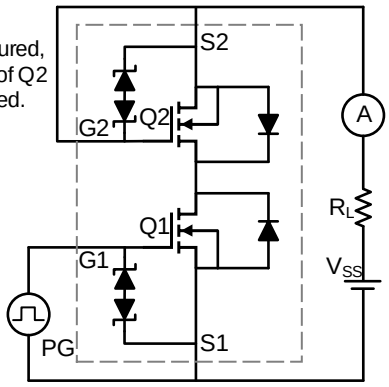
Test Circuit 5
V_{FSS}

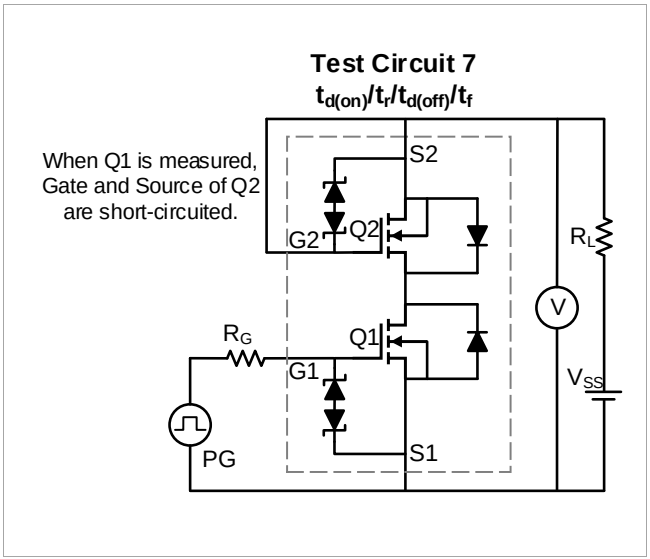
When Q1 is measured, +4.5V is added to V_{GS} of Q2.



Test Circuit 6
$Q_g/Q_{gs}/Q_{gd}/Q_{g(th)}$

When Q1 is measured, Gate and Source of Q2 are short-circuited.





Revision History

Version	Date	Change Record
V1.0	Feb. 2023	Officially released
V1.1	May. 2023	1. Updated the value of I_S from 7A to 6A in V_{FSS} Conditions. (P3) 2. Updated the Tape And Reel Information. (P6) 3. Added the test circuits. (P9-P10)
V1.2	Jun. 2023	Updated the value of V_{SS} from 9.6V to 12V in I_{SSS} Conditions. (P3)
V1.3	Nov. 2025	Updated the maximum value of I_{SSS} from 1μA to 100nA. (P3)

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