30V P-Channel Enhancement-Mode MOSFET

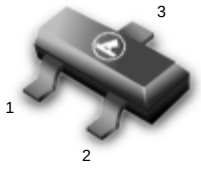
LP2305LT1G
S-LP2305LT1G

V_{DS}= -30V

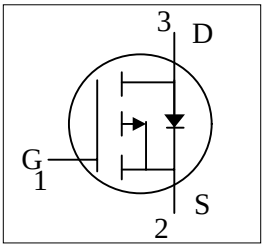
$R_{DS(ON)}$, V_{gs}@-10V, I_{ds}@-4.2A = 70mΩ

$R_{DS(ON)}$, V_{gs}@-4.5V, I_{ds}@-4.0A = 85 mΩ

$R_{DS(ON)}$, V_{gs}@-2.5V, I_{ds}@-1.0A = 130mΩ



SOT– 23 (TO–236AB)



FEATURES

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

ORDERING INFORMATION

Device	Marking	Shipping
LP2305LT1G S-LP2305LT1G	P05	3000/Tape&Reel
LP2305LT3G S-LP2305LT3G	P05	10000/Tape&Reel

MAXIMUM RATINGS AND THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	**Symbol**	**Limit**	**Unit**
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±12	
Continuous Drain Current	I_D	-4.2	A
Pulsed Drain Current [1)]	I_{DM}	-30	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Total Power Dissipation	P_D	1.4	W
Junction-to-Ambient Thermal Resistance (PCB mounted) [2)]	$R_{\theta JA}$	140	°C/W

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature
2. 1-in 2oz Cu PCB board

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static [2]						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-30			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -4.2A		53.0	70.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -4A		64.0	85.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -2.5V, I_D =-1A		86.0	130.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	-0.7		-1.3	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0V			± 100	nA
Forward Transconductance	g_{fs}	V_{DS} = -5V, I_D = -5A	7	11		S
Dynamic[3]						
Total Gate Charge	Q_g	V_{DS} = -15V, I_D = -4A V_{GS} = -4.5V		6.36		nC
Gate-Source Charge	Q_{gs}			1.79		
Gate-Drain Charge	Q_{gd}			1.42		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V, RL= 3.6Ω I_D = -1A, V_{GEN} = -10V R_G = 6Ω		11.36		ns
Turn-On Rise Time	t_r			2.32		
Turn-Off Delay Time	$t_{d(off)}$			34.88		
Turn-Off Fall Time	t_f			3.52		
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V f = 1.0 MHz		826.18		pF
Output Capacitance	C_{oss}			90.74		
Reverse Transfer Capacitance	C_{rss}			53.18		
Source-Drain Diode						
Max. Diode Forward Current	I_S				-2.2	A
Diode Forward Voltage	V_{SD}	I_S = -1.0A, V_{GS} = 0V			-1	V

Note: 1. Pulse test: pulse width <= 300us, duty cycle<= 2%

2. Static parameters are based on package level with recommended wire-bonding

3. Guaranteed by design; not subject to production testing

LP2305LT1G , S-LP2305LT1G

TYPICAL ELECTRICAL CHARACTERISTICS

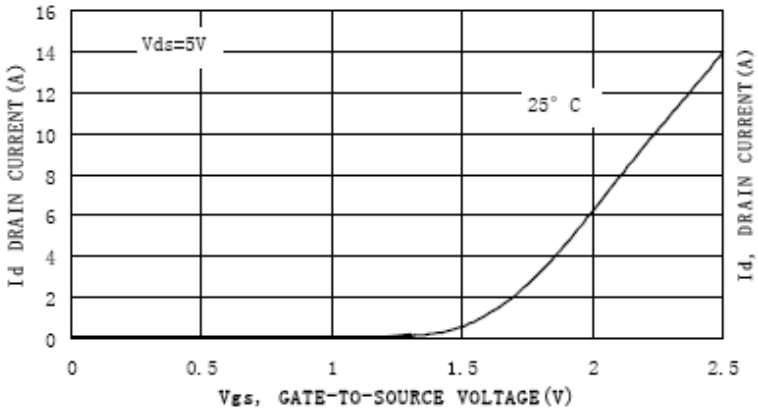


Figure 1. Transfer Characteristics

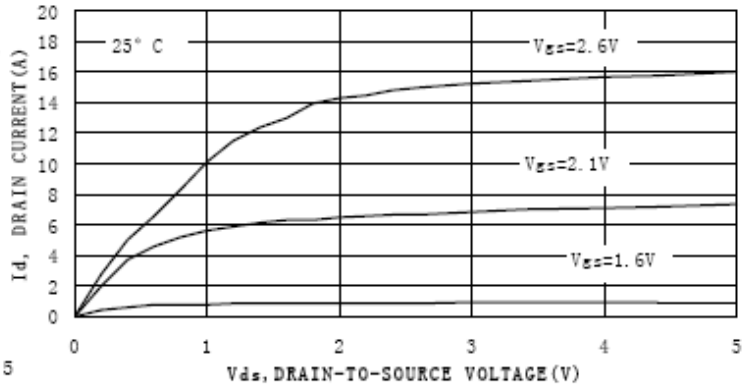


Figure 2. On–Region Characteristics

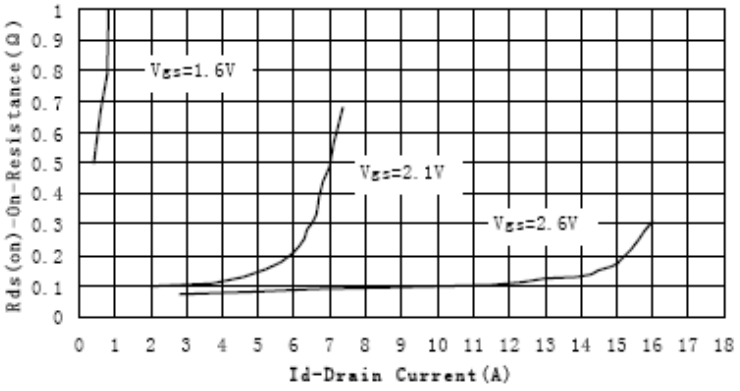


Figure 3. On–Resistance versus Drain Current

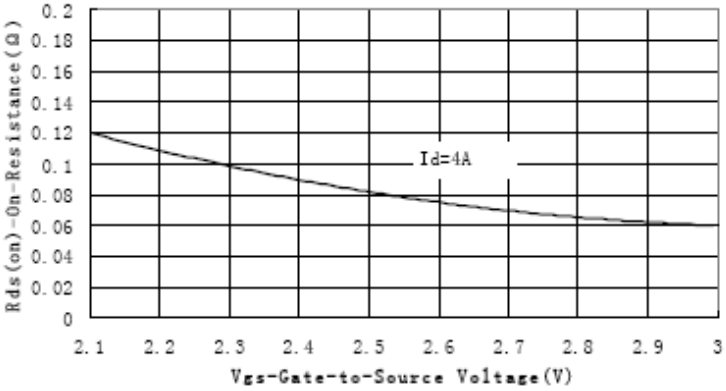
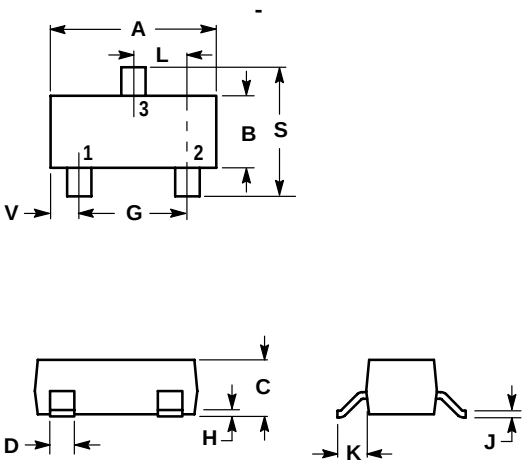


Figure 4. On-Resistance vs. Gate-to-Source Voltage

LP2305LT1G , S-LP2305LT1G

SOT–23



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60