

1A Low-Dropout Linear Regulator

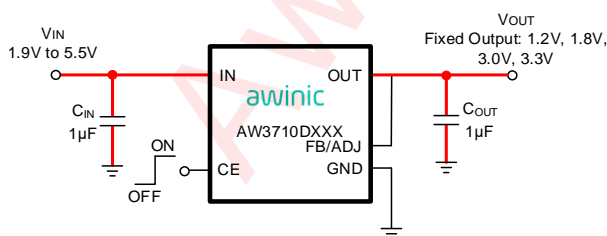
Features

- Input voltage range: 1.9V to 5.5V
- Fixed outputs of 1.2V, 1.8V, 3.0V, 3.3V
- Rated output current: 1A
- Quiescent current: typical 85 μ A
- Typical 0.3 μ A shutdown current
- Typical 155mV dropout voltage at 1A load , $V_{OUT}=3.3V$
- Power supply rejection ratio: typical 82dB ($I_{OUT}=30mA$, $f_{req}=1kHz$)
- Noise: typical 26 μ Vrms ($I_{OUT}=30mA$, $BW=10Hz$ to 100kHz)
- Built-in output short protection: typical 130mA when output short to ground
- Output auto discharge function
- SOT89 4.5mmX4.5mm-5L package

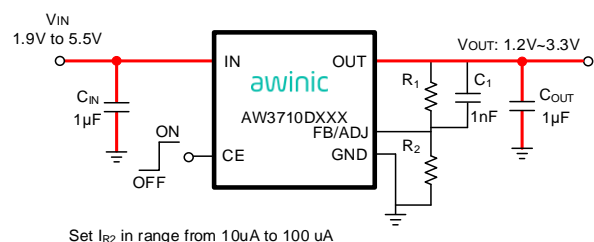
Applications

Battery-powered equipment
Smart phone
Digital camera
STB

Typical Application Circuit



Fixed Output Voltage Application



Adjustable Output Voltage Application

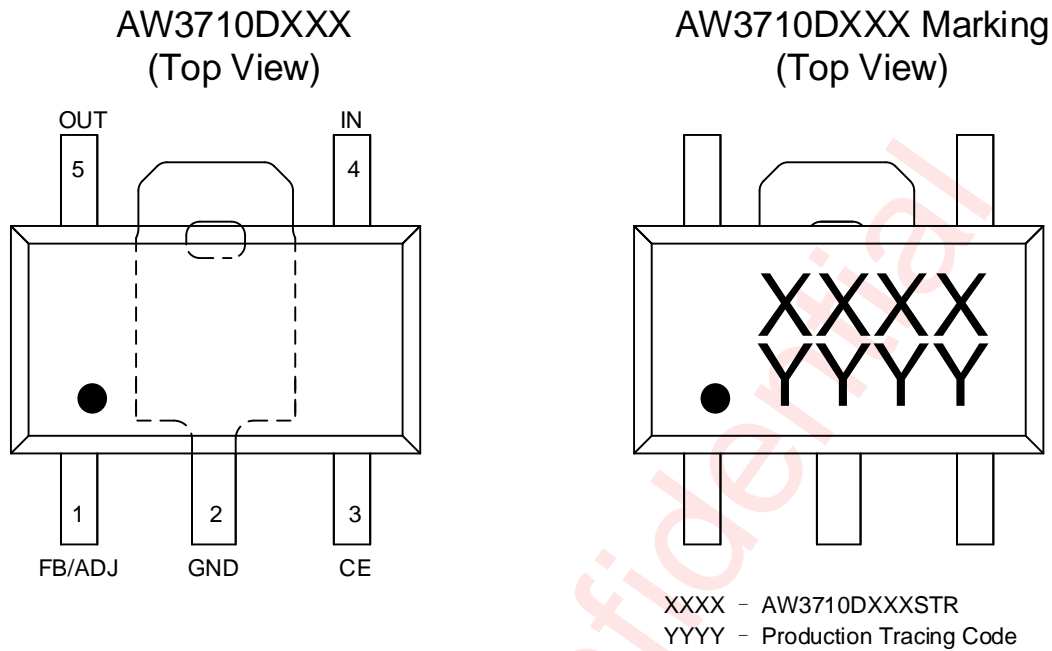
General Description

AW3710DXXX is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW3710DXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged. Meanwhile AW3710DXXX integrates a reverse current protection circuit.

AW3710DXXX is designed to work with a 1 μ F or more input ceramic capacitor and a 1 μ F or more output ceramic capacitor. The low power dissipation and good dynamic response make AW3710DXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

Pin Configuration and Top Mark



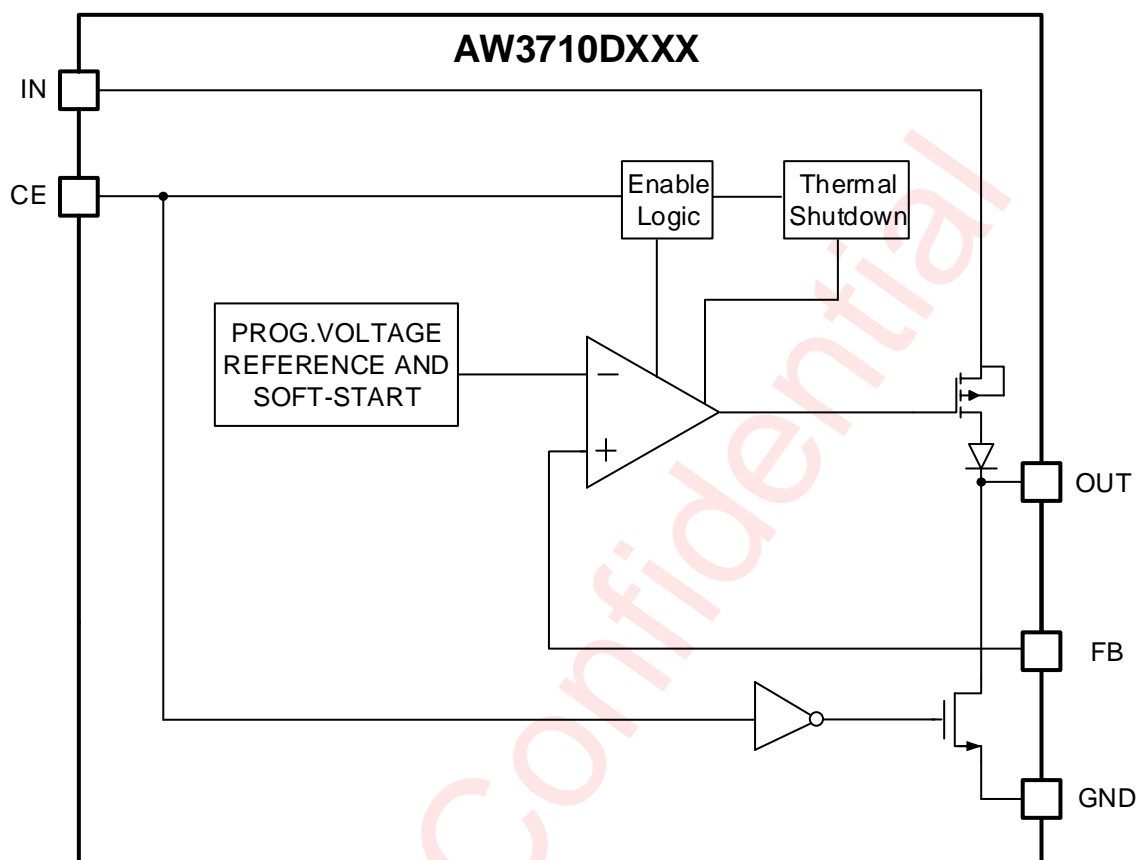
Pin Definition

No.	NAME	DESCRIPTION
1	FB/ADJ	Feedback /adjustable pin (connect this pin directly to the OUT pin or to the resistor divider)
2	GND	Ground.
3	CE	Chip enable pin. Built-in pull-down resistor. (High Active)
4	IN	Input supply pin. Put a 1 μ F or more bypass capacitor at the power supply.
5	OUT	Regulated output voltage pin. Put a 1 μ F or more ceramic capacitor at the output pin.

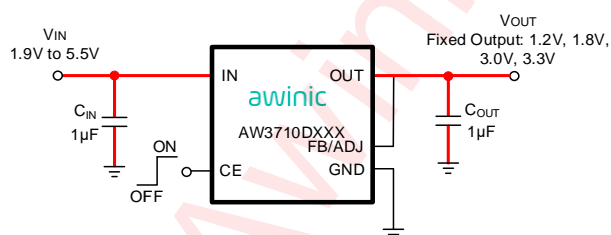
Device Comparison Table

Part Number	V _{OUT(SET)}	Rated Current	CE Active	Auto Discharge
AW3710D120STR	1.2V or ADJ	1A	High	YES
AW3710D180STR	1.8V	1A	High	YES
AW3710D300STR	3.0V	1A	High	YES
AW3710D330STR	3.3V	1A	High	YES

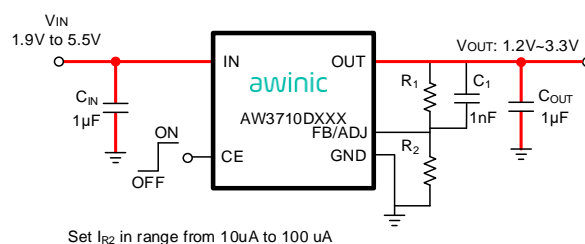
Functional Block Diagram



Typical Application Circuits



Fixed Output Voltage Application



Adjustable Output Voltage Application

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be $1\mu\text{F}$ or more.

The input and output capacitor must be located a distance of not more than 1 cm.

$$V_{OUT_ADJ} = V_{OUT_SET} \left(1 + \frac{R_1}{R_2} \right), \text{ Set } I_{R1}, I_{R2} \text{ in range from } 10\mu\text{A} \text{ to } 100\mu\text{A} \text{ for better performance.}$$

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW3710D120 STR	-40°C~85°C	SOT89 4.5mmX4.5 mm-5L	L7ZZ	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW3710D180 STR	-40°C ~ 85°C	SOT89 4.5mmX4.5 mm-5L	QJ1W	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW3710D300 STR	-40°C ~ 85°C	SOT89 4.5mmX4.5 mm-5L	R50F	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW3710D330 STR	-40°C ~ 85°C	SOT89 4.5mmX4.5 mm-5L	U3LJ	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
Input voltage range V_{BUS}	-0.3V to 6.5V
Enable control voltage range	-0.3V to 6.5V
Output voltage range	-0.3V to 6.5V
Junction-to-ambient thermal resistance θ_{JA} ^(NOTE2)	44.1°C/W
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD	
HBM (Human body model) ^(NOTE3)	±2kV
CDM(Charged device model) ^(NOTE4)	±1.5kV
Latch-Up	
Latch-Up ^(NOTE5)	+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ANSI/ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: JEDEC EIA/JESD22-C101F .

NOTE5: Test Condition: JEDEC STANDARD NO.78E SEPTEMBER 2016 .

Electrical Characteristics

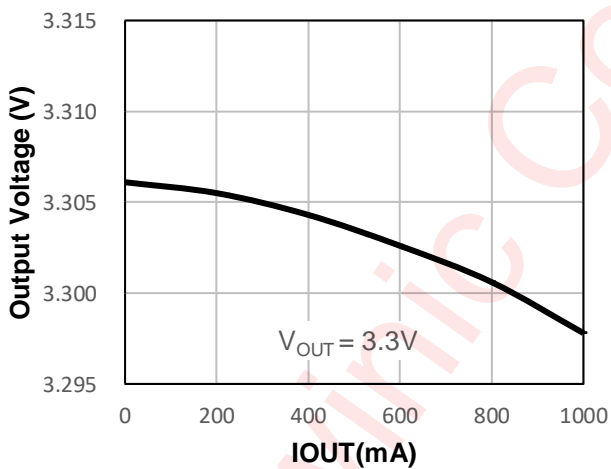
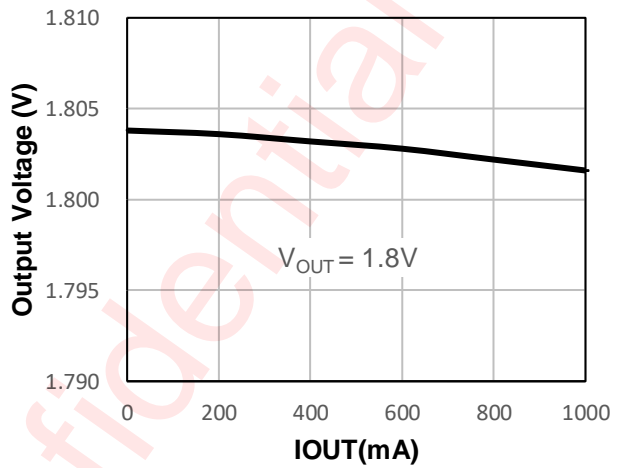
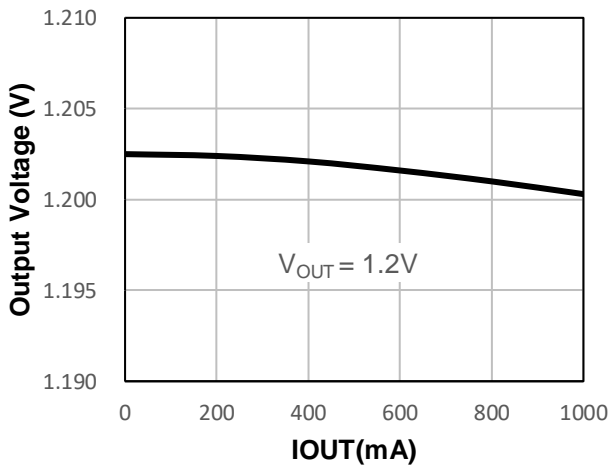
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		1.9		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy		-2.5		2.5	%
$LOAD_{Reg}$	Load Regulation	$1mA \leq I_{OUT} \leq 1A$		1	40	mV
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}+0.5V \leq V_{IN} \leq 5.5V$		1	5	mV
$V_{dropout}$	Dropout Voltage	$I_{OUT}=1A$, $V_{OUT(SET)}=1.8V$		240		mV
		$I_{OUT}=1A$, $V_{OUT(SET)}=3.3V$		155		mV
I_{SD}	Shutdown Current	$V_{CE}<0.4V$		0.3	1	μA
I_Q	Quiescent Current	$I_{OUT}=0mA$		85	133	μA
V_{CEH}	CE Input Voltage "H"	$-40^\circ C \leq T_A \leq 85^\circ C$	1.1			V
V_{CEL}	CE Input Voltage "L"	$-40^\circ C \leq T_A \leq 85^\circ C$			0.4	V
PSRR		$I_{OUT}=30mA$, $f=1kHz$		82		dB
V_N	Output Voltage Noise	$I_{OUT}=30mA$, $BW=10Hz$ to $100kHz$		26		μV_{rms}
I_{CL}	Output Current Limit		1			A
I_{SC}	Short Current Limit	$V_{OUT}=0V$		130		mA
VTC	Output Voltage Temperature Coefficient	$-40^\circ C \leq T_A \leq 85^\circ C$		± 80		ppm/ $^\circ C$
R_{DISC}	Auto Discharge Resistance	$V_{CE}<0.4V$, $I_{OUT}=0mA$		66		Ω
R_{CE}	CE Pull Down Resistance			2.2		M Ω
T_{SDH}		Temperature Rising		155		$^\circ C$
T_{SDL}		Temperature Falling		110		$^\circ C$
I_{REV}	Reverse Current	$V_{OUT(SET)}=1.2V$, $V_{OUT}=V_{OUT(SET)}+1.0V$ $0 \leq V_{IN} \leq V_{OUT}$		0.2		μA
V_{REV_DET}	Detection Offset Voltage in Reverse Current Protection Mode	$V_{OUT} \geq 0.7V$, $0 \leq V_{IN} \leq 5.5$ $V_{REV_DET} = V_{OUT} - V_{IN}$		30		mV
V_{REV_REL}	Release Offset Voltage in Reverse Current Protection Mode			20		mV

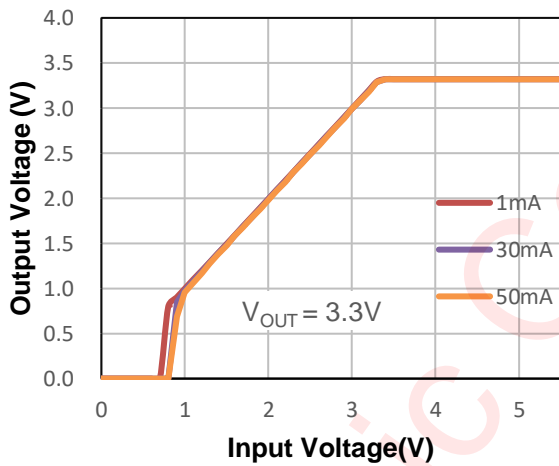
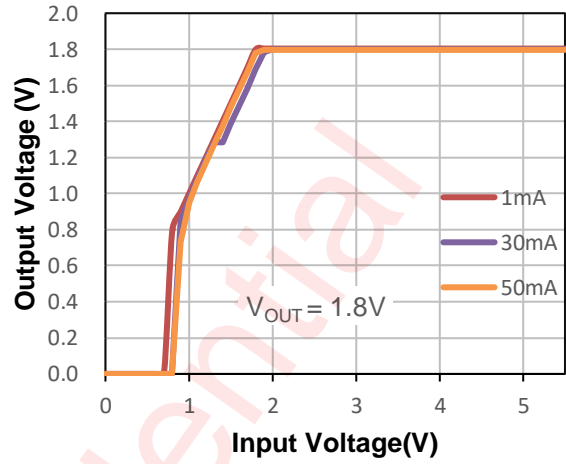
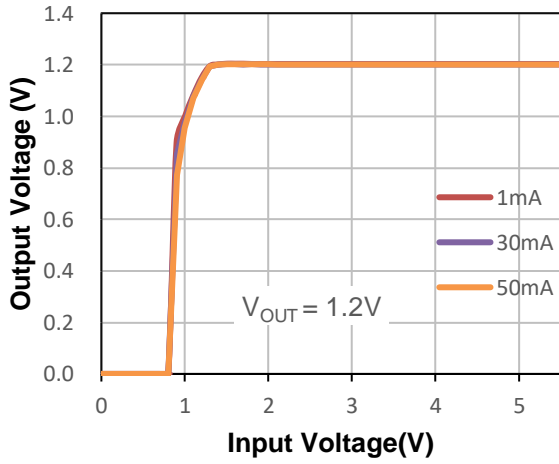
Typical Characteristics

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1.1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, In Typical Application Circuit, unless other noted.

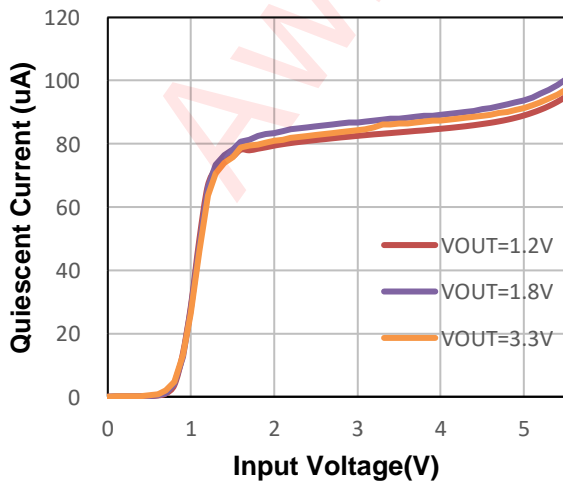
1) Output Voltage vs. Output Current ($C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$)

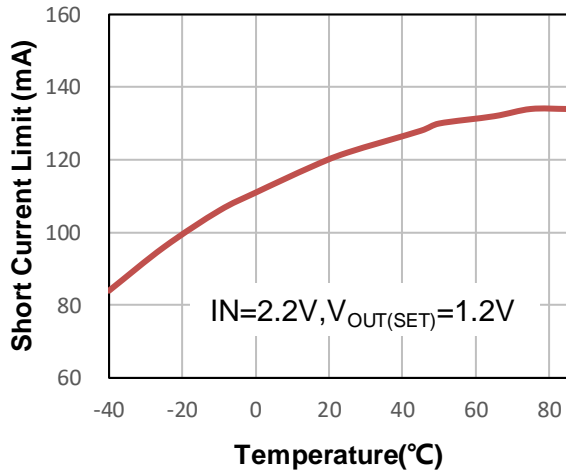
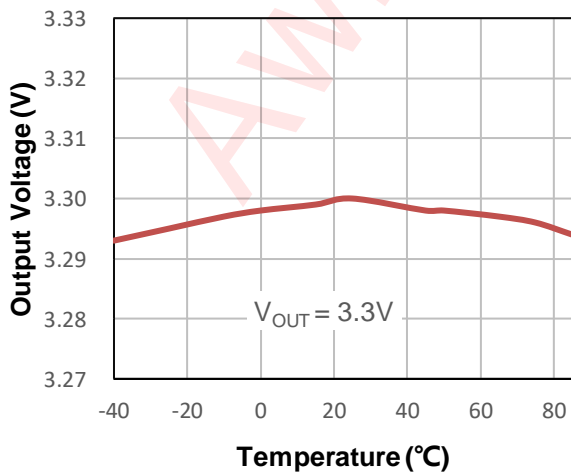
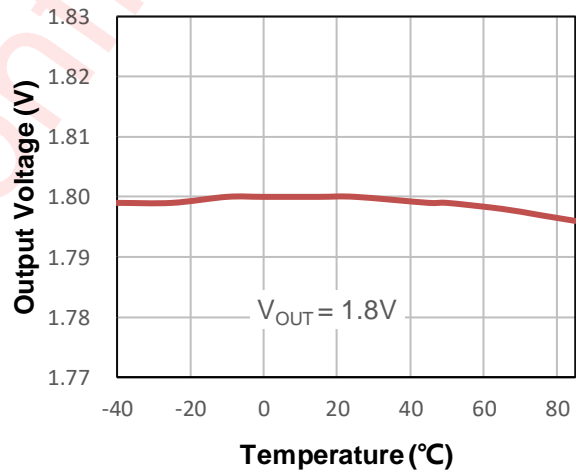
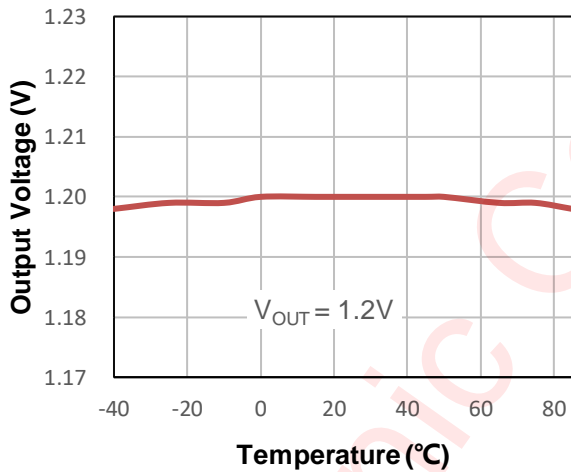


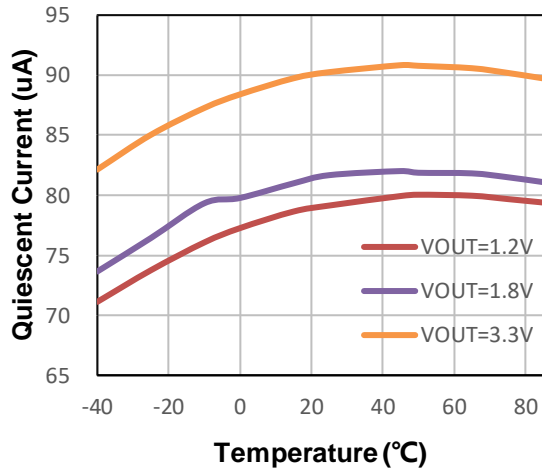
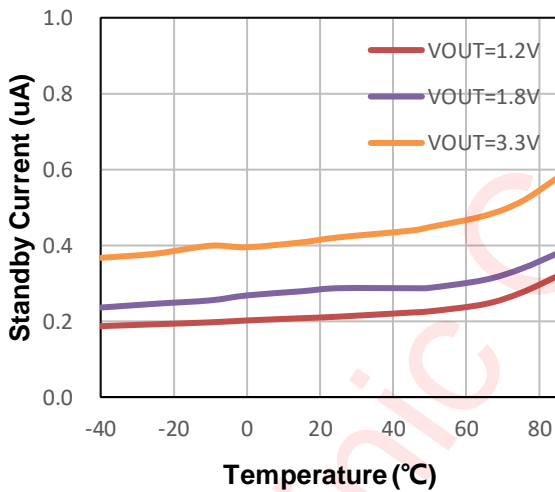
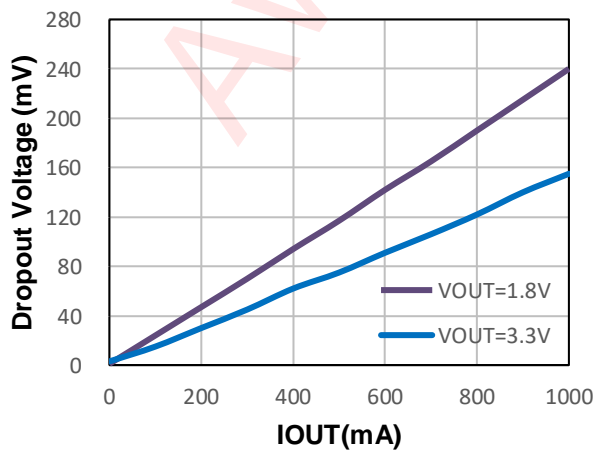
2) Output Voltage vs. Input Voltage ($C_{IN}=C_{OUT}=1\mu F, T_A=25^\circ C$)



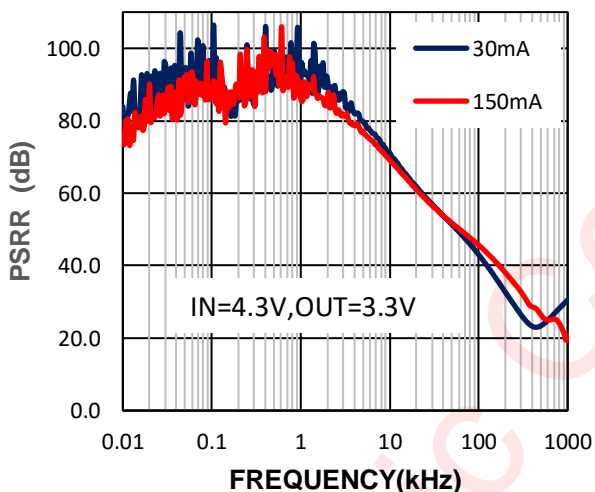
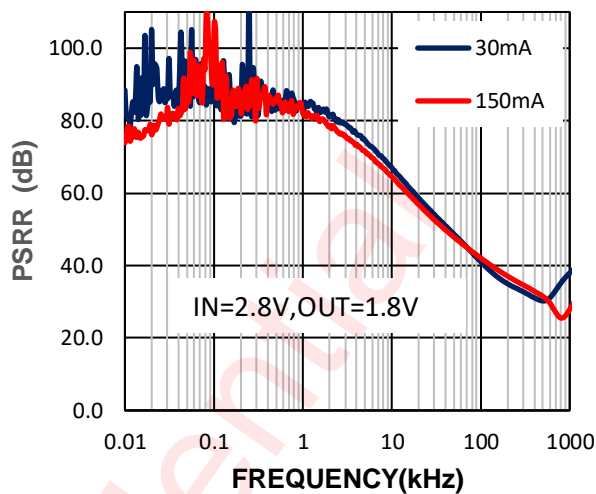
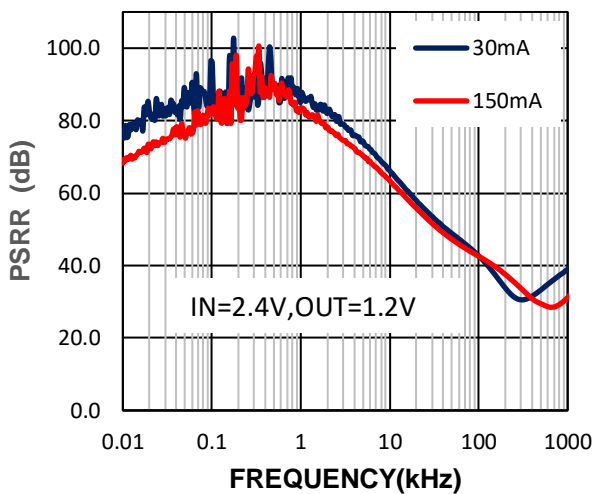
3) Quiescent Current vs. Input Voltage ($C_{IN}=C_{OUT}=1\mu F, T_A=25^\circ C$)



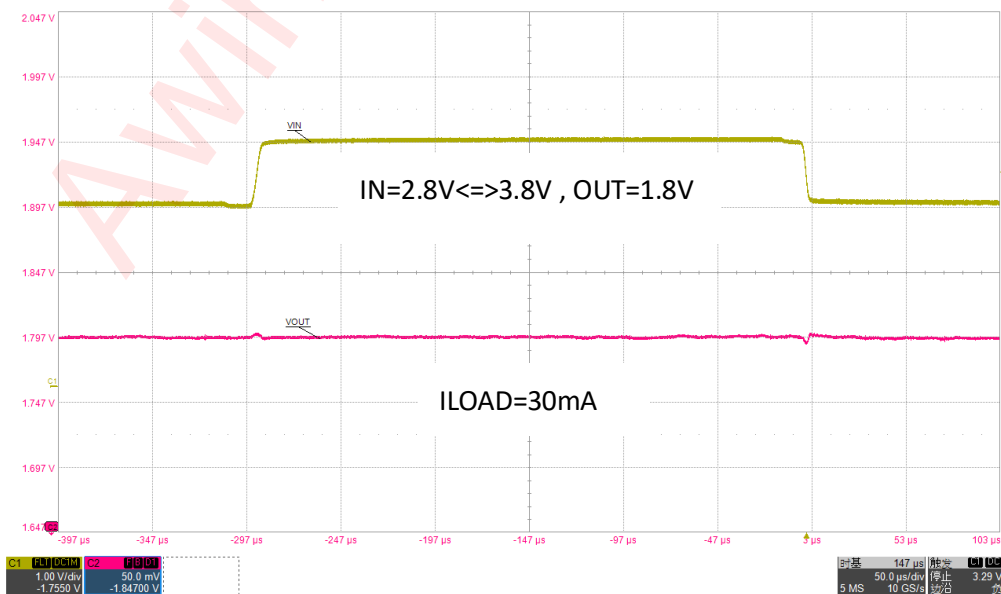
4) Short Current Limit vs. Temperature ($C_{IN}=C_{OUT}=1\mu F$)5) Output Voltage vs. Temperature ($C_{IN}=C_{OUT}=1\mu F$, $I_{OUT}=1mA$)

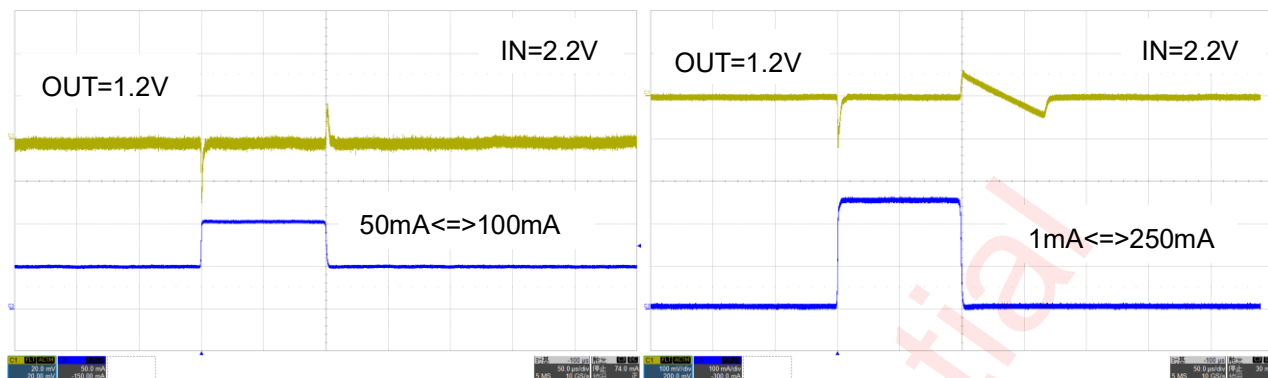
6) Quiescent Current vs. Temperature ($C_{IN}=C_{OUT}=1\mu F$)7) Standby Current vs. Temperature ($C_{IN}=C_{OUT}=1\mu F$)8) Dropout Voltage vs. Output Current ($C_{IN}=C_{OUT}=1\mu F, T_A=25^\circ C$)

9) Ripple Rejection vs. Frequency ($C_{IN}=0.1\mu F, C_{OUT}=1\mu F, T_A=25^\circ C$)



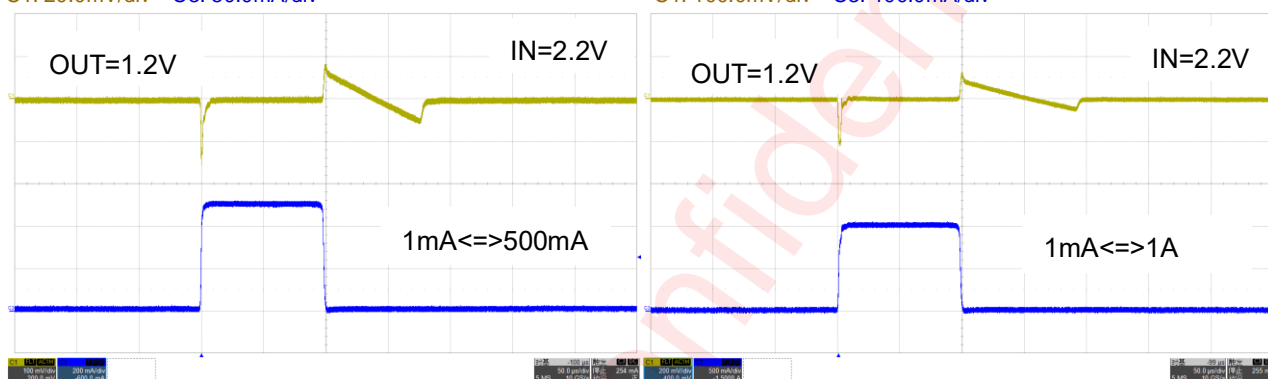
10) Line Transient ($C_{IN}=C_{OUT}=1\mu F, t_r = t_f = 10\mu s, T_A=25^\circ C$)



11) Load Transient ($C_{IN}=C_{OUT}=1\mu F$, $t_r=t_f=1\mu s$, $T_A=25^\circ C$)

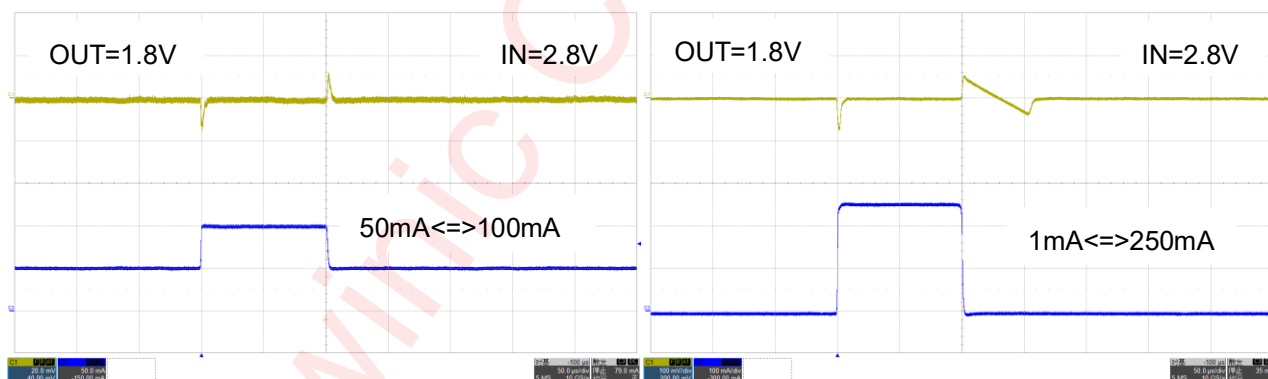
C1: 20.0mV/div C3: 50.0mA/div

C1: 100.0mV/div C3: 100.0mA/div



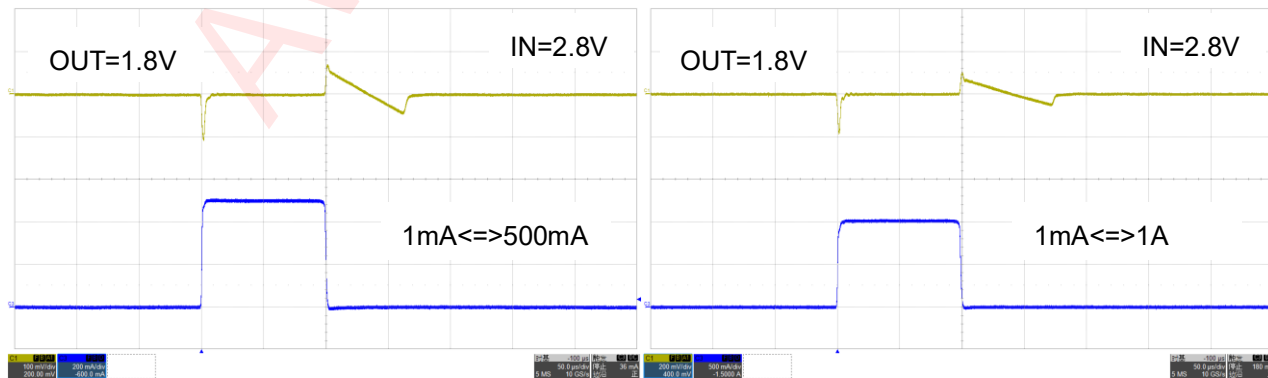
C1: 100.0mV/div C3: 200.0mA/div

C1: 200.0mV/div C3: 500.0mA/div



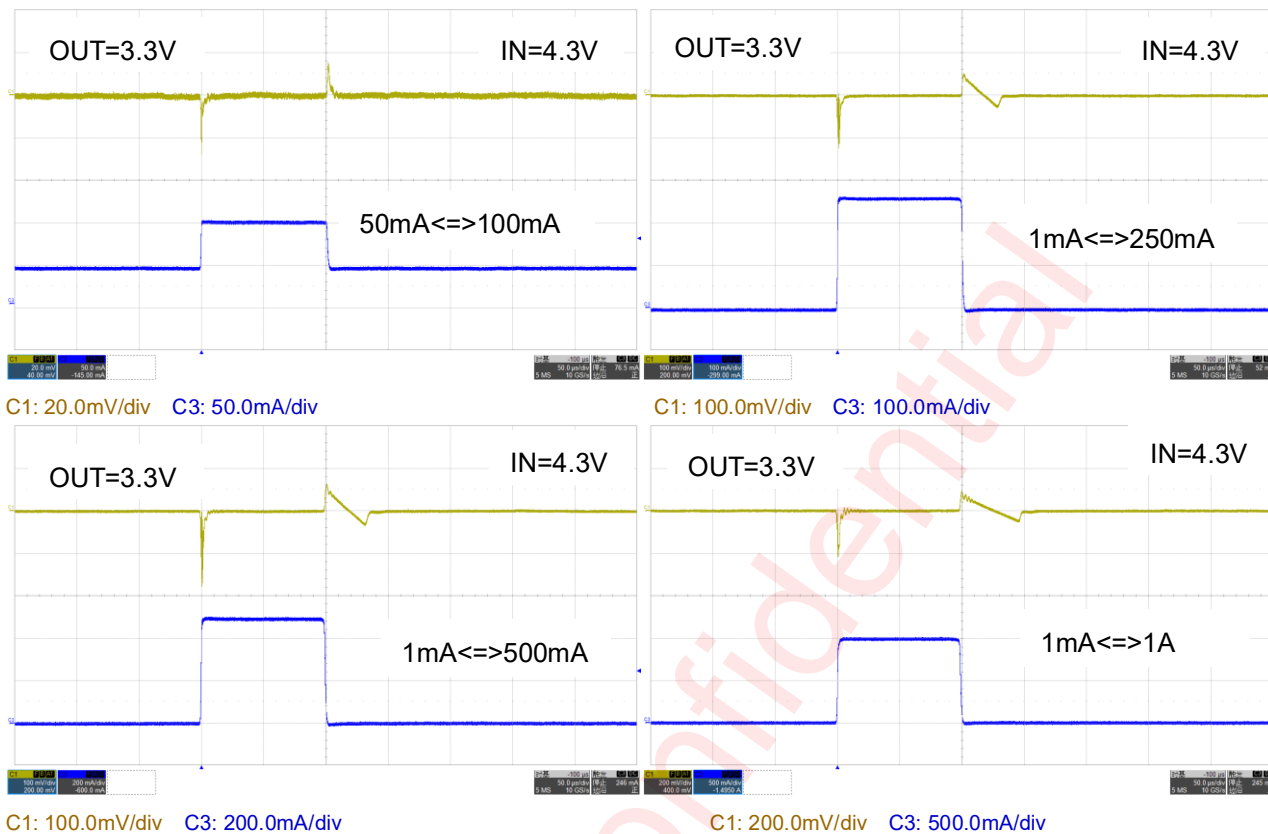
C1: 20.0mV/div C3: 50.0mA/div

C1: 100.0mV/div C3: 100.0mA/div

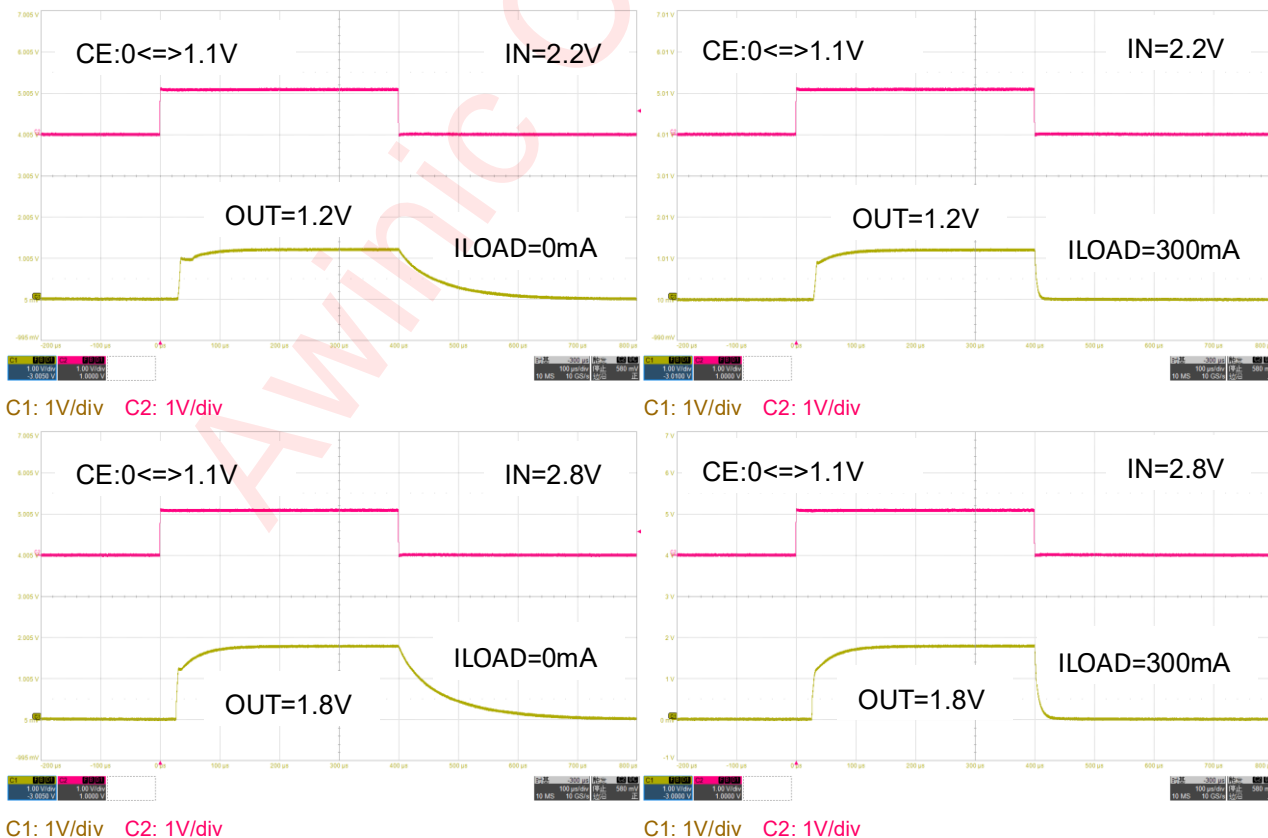


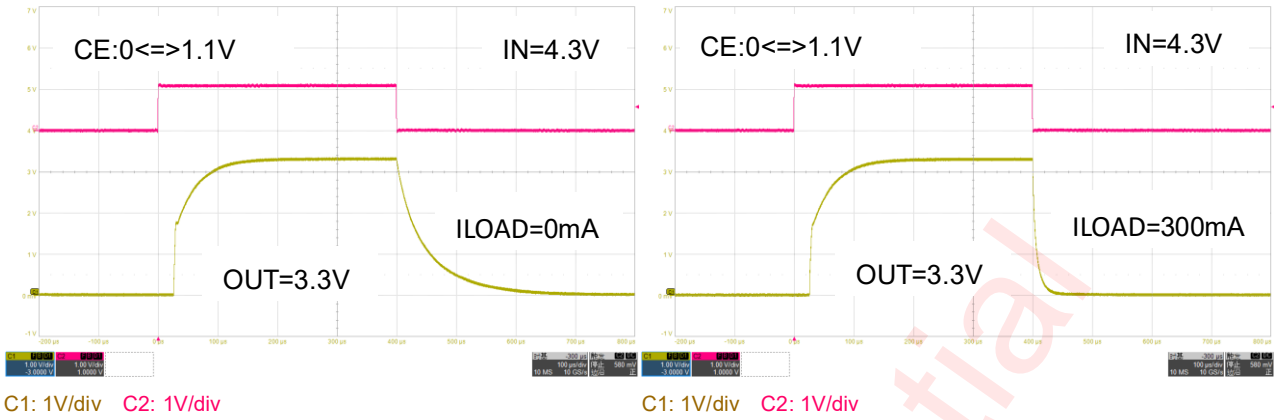
C1: 100.0mV/div C3: 200.0mA/div

C1: 200.0mV/div C3: 500.0mA/div



12) Turn-on/off Waveform by CE Pin signal ($C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$)





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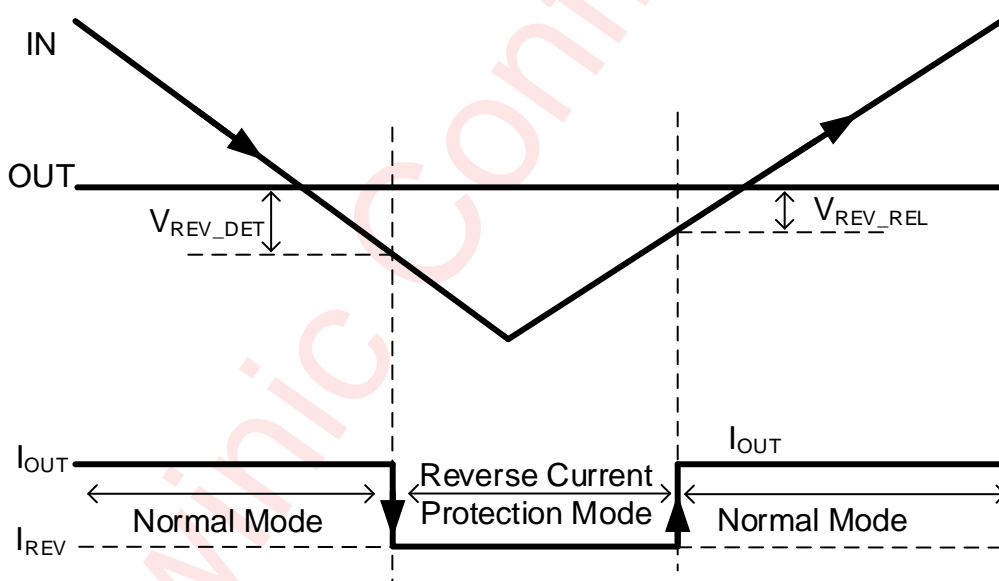
Detailed Functional Description

AW3710DXXX is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate.

Reverse Current Protection Circuit

Usually, the LDO using PMOS output transistor contains a parasitic diode between VIN pin and VOUT pin. Therefore, if VOUT is higher than VIN, the parasitic diode becomes forward direction. As a result, the current flows from VOUT pin to VIN pin. The AW3710DXXX integrates a reverse current protection circuit, which stops the reverse current from VOUT pin to VIN pin when Vout becomes higher than VIN.

Following figure shows the principle of each mode. When giving the OUT pin a constant voltage and decreasing the IN voltage. When the IN voltage become lower than $OUT - V_{REV_DET}$, the reverse current protection starts to function to stop the load current. By increasing the IN voltage higher than $OUT - V_{REV_REL}$, the protection mode will be released to let the load current to flow.



Enable Operation

AW3710DXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.4V, AW3710DXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is open making output discharge through a 66Ω resistor to Ground. In disable state, AW3710DXXX only consumes a typical 0.3uA current.

If the voltage of CE pin is more than 1.1V, AW3710DXXX is guaranteed to be enabled. In this state, the auto discharge MOSFET is closed, and AW3710DXXX regulates output voltage to the designed value of voltage.

A 2.2MΩ resistor to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW3710DXXX integrates output current limit function, protecting IC from excessive current. When the load is excessively heavy, AW3710DXXX limits the current flowing through the IC to a typical 1.5A current. This value is specially designed, so that IC is protected properly and the output capability of 1A is not influenced either.

Meanwhile, AW3710DXXX integrates fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW3710DXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 155°C, AW3710DXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 110°C. At this moment, the over-temperature protection-state is released, IC resumes to work again. The hysteresis avoids IC's turning off and on frequently around the Thermal Shutdown threshold.

Auto Discharge

AW3710DXXX makes output voltage decrease quickly when in disable state or thermal shutdown state, benefit from integrating auto discharge function.

Application Information

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW3710DXXX advises to use a 1 μ F or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW3710DXXX advises to use a 1 μ F or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μ F
	CL05A105K05NNNC	16V, X5R, 0402	Samsung	1	
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	
	CL05A105K05NNNC	16V, X5R, 0402	Samsung	1	
	GRM155R61A225KE95	10V, X5R, 0402	MURATA	2.2	

Output Voltage

FB/ADJ pin could be connected to the output pin directly to compensate voltage drop across the internal bond wiring and PCB traces or to the middle point of the output resistor divider to adjust the output voltage. The output voltage of the circuit is simply the same as the nominal output voltage of the LDO while FB/ADJ connected to the output pin. When connected to the resistor divider the output voltage is the nominal output voltage multiplied by the resistors divider ratio, see following equation.

$$V_{\text{OUT_ADJ}} = V_{\text{OUT_SET}} \left(1 + \frac{R1}{R2} \right)$$

Where:

- $V_{\text{OUT_ADJ}}$ is output voltage of the circuit with resistor divider
- $V_{\text{OUT_SET}}$ is the LDO's nominal output voltage

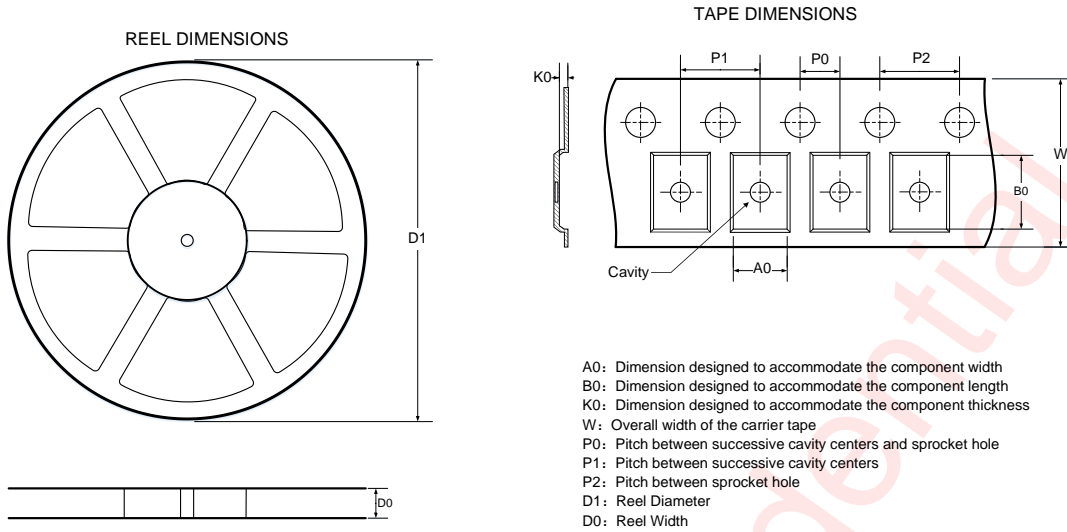
Chose the R1 and R2 values to have their currents IR1 and IR2 in range from 10 to 100 μA for good stability and fast transient response. The capacitor C1 = 1 nF improves the stability and transient response as well.

PCB Layout Consideration

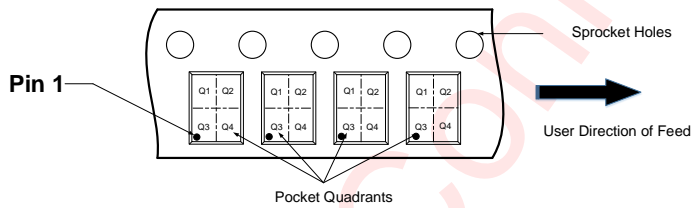
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW3710DXXX should be obeyed:

1. All peripheral components should be placed as close as possible to the device with shortest-distance wirings. Connect an input capacitor (CIN) between the VIN and GND pins with shortest-distance wiring. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, ensure the wirings are sufficiently robust make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of CIN or COUT and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference. If the impedance of wiring between the VIN VOUT and GND pins is high, it may cause noise pickup or unstable operation.
4. Connect an output capacitor (COUT) between the VOUT and GND pins with shortest-distance wiring.
5. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.9	4.9	1.8	2	8	4	12	Q3

All dimensions are nominal

Revision History

Version	Date	Change Record
V1.0	May 2019	Officially released
V1.1	Oct 2020	Update Output Voltage vs. Input Voltage curve.
V1.2	Feb.2025	Reduce V_{OUT} of 1.5V/2.5V/2.8V.(P1-4) Update Electrical Characteristics.(P6)

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