23V Digital Input, High Efficiency Class-D Audio Amplifier with PSM

Features

- **Key Features**
  - 23V supply for Class-D Output Stage
  - PSM Multi-Level Supply Architecture
  - PTC External Boost Control Algorithm
  - Ultrasonic Output Support up to 40kHz
- **Output Power**
  - 30W@4Ω, 18V, THD+N<1%
- **High-efficiency Class-D Amplifier PSM ON**
  - 81% at 0.5W,4Ω, PVDDH=18V, PVDDL=5V
  - 84% at 1W,4Ω, PVDDH=18V, PVDDL=5V
- **High-efficiency Class-D Amplifier PSM OFF**
  - 80% at 1W, 4Ω, PVDDH=18V, PVDDL=5V
  - 89% at 10W, 4Ω, PVDDH=18V, PVDDL=5V
  - 90% at 20W, 4Ω, PVDDH=18V, PVDDL=5V
- **Interface and Control**
  - I2S/TDM:8 Channels of 32 bits up to 96ksps
  - Data Width: 16, 20, 24, 32 bits
  - 32kHz to 192kHz Sample Rates
- **Protection and EMI:**
  - IV-Sense for Speaker Protection
  - Over Power and Low Battery Protection
  - PVDDH/PVDDL Supply Tracking Limiters
  - Thermal and Over Current Protections
  - Thermal Foldback
- **Power Supplies**
  - PVDDH: 3V~23V
  - PVDDL: 2.7V~5.5V
  - AVDD: 1.8V
  - IOVDD: 1.8V/3.3V
- **Integrated Self-Protection**
  - Over-Current Protection (OCP)
  - Over-Temperature Protection (OTP)
  - Over / Under-Voltage Lock-out (OVLO/UVLO)
  - Cycle by Cycle (CBC)
  - DC-detect and short-circuit protection
- FCQFN 3.5mmX4mm-30L Package

Applications

- Laptop and Desktop Computers
- Smart Speakers
- Tablets and Handhelds
- Wireless Speakers

Description

The AW85281 is a mono, digital input Class-D audio amplifier optimized for efficiently driving high peak power into loudspeakers. The Class-D amplifier is capable of delivering 30W of continuous power into a 4Ω load with less than 1% THD+N at a supply voltage of 18V. The broad voltage input range and the high output power makes this amplifier versatile enough to work with battery or line powered systems.

The integrated speaker voltage and current sense provides for real-time monitoring of loudspeakers.

PSM power architecture improves amplifier efficiency by internally selection the supplies for optimal headroom. Brownout prevention scheme with adjustable threshold allows reducing the gain in signal path when the supply drops.

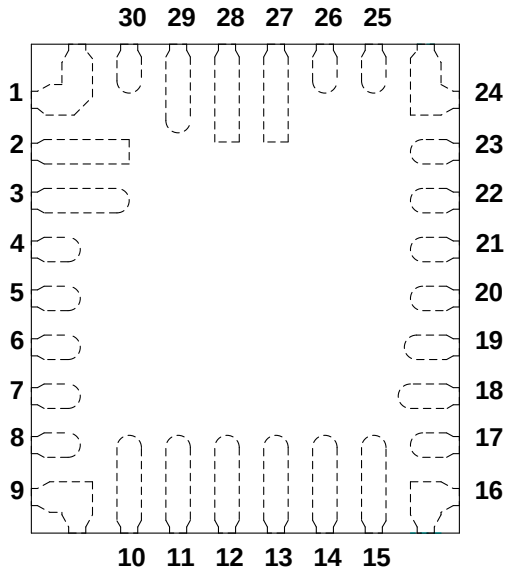
The PTC algorithm allows user to optimize efficiency and improve battery life by controlling the external power supply.

Up to eight AW85281 devices can share a common bus via I2S/TDM and I2C interfaces.

AW85281 is available in a 30 pin FCQFN 3.5mmX4mm-30L Package for a compact PCB footprint.

Pin Configuration and Top Mark

AW85281FCR
(Top View)



AW85281FCR Marking
(Top View)

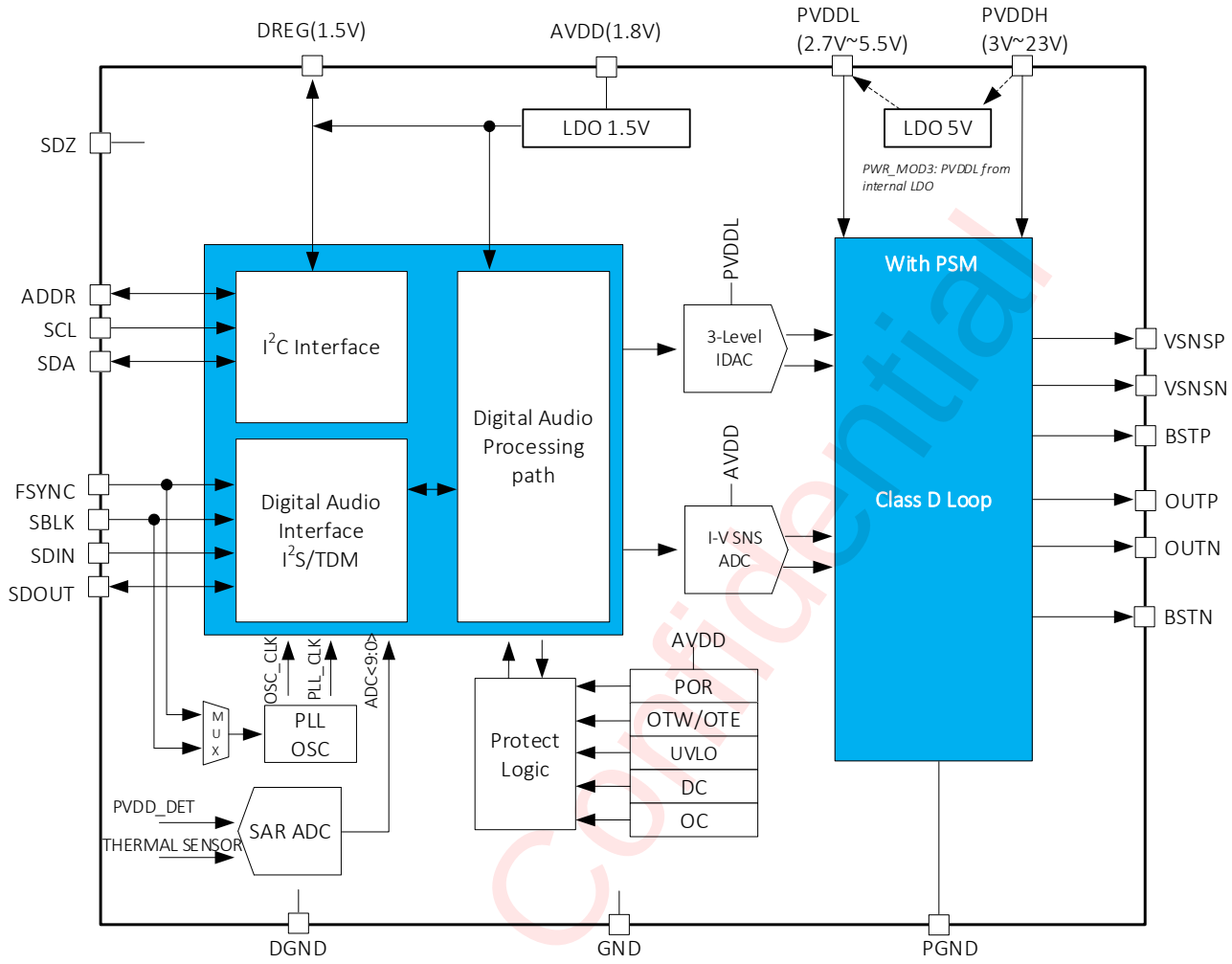
NGYZ—AW85281FCR
XXXX/XXXX—Production Tracing Code

Pin Description

Pin No	Pin Name	Description
1	VSNSN	Voltage sense negative input
2	PGND	Class-D amplifier ground
3	OUTP	Class-D amplifier positive output
4	BSTP	Class-D amplifier positive output
5	VSNSP	Voltage sense positive input
6	MUTEN	MUTE pin
7	GND	Analog ground
8, 9, 16, 17, 26	NC	Not used
10	DREG	Digital core regulator output
11	PWM_CTRL	Control pin for external boost converter
12	SDOUT	Audio serial data output
13	SDIN	Audio serial data input
14	FSYNC	Audio serial frame clock
15	SBCLK	Audio serial bit clock
18	SCL	I2C clock
19	SDA	I2C data
20	IOVDD	Digital IO supply
21	IRQZ	Interrupt pin, active low with open drain

Pin No	Pin Name	Description
22	SDZ	Hardware shutdown, active low
23	ADDR	Address detect pin
24	AVDD	Analog power
25	DGND	Device substrate ground
27	PVDDL	Low-side class-D power stage
28	PVDDH	High-side class-D power stage
29	OUTN	Class-D amplifier negative output
30	BSTN	Class-D negative bootstrap

Functional Block Diagram



Typical Application Circuit

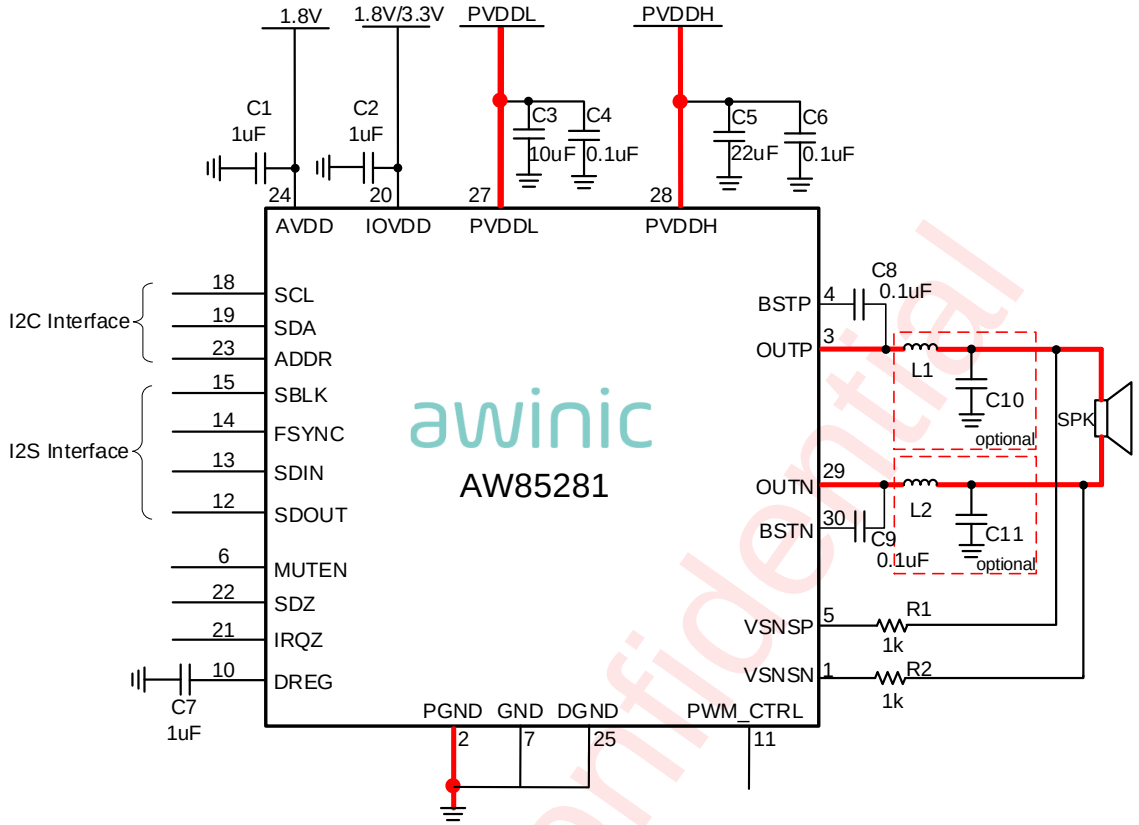


Figure 1 AW85281 Typical Application Circuit

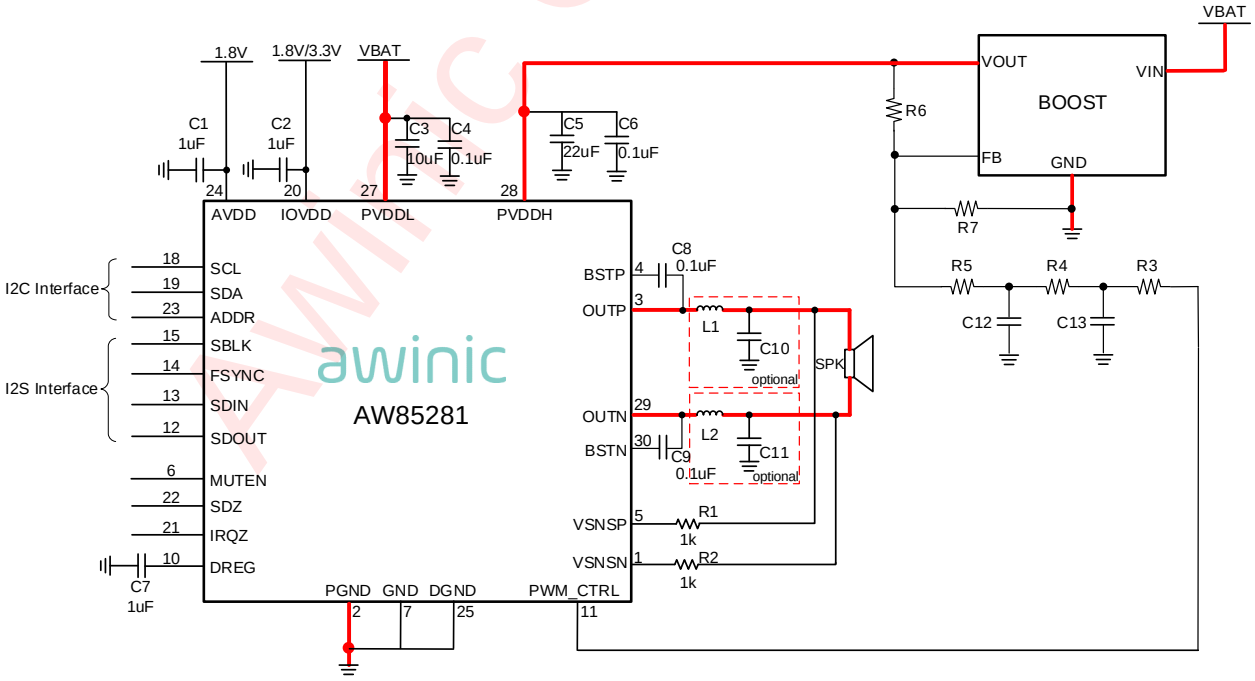


Figure 2 AW85281 Application Circuit – External Boost Control

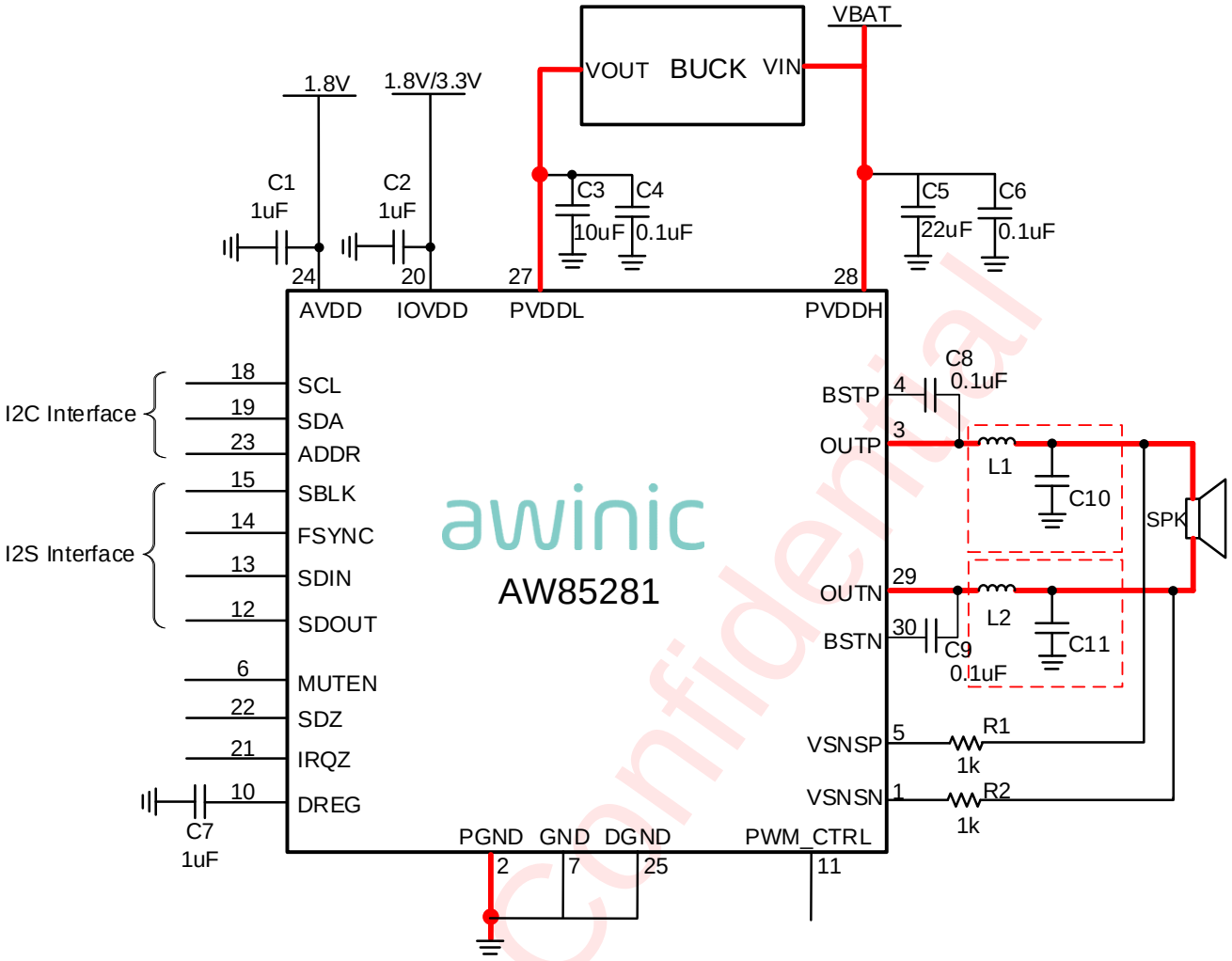


Figure 3 AW85281 Application Circuit – External Buck Circuit

***Notes**: Traces carry high current are marked in red in the above figure*

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW85281FCR	-40°C~105°C	FCQFN 3.5X4-30L	NGYZ	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{PVDDL}		-0.3V to 6V
Supply voltage range V_{PVDDH}		-0.3V to 26V
Digital I/O voltage range V_{IOVDD}		-0.3V to 5V
Analog voltage range V_{AVDD}		-0.3V to 2V
Digital core regulator output voltage range V_{DREG}		-0.3V to 1.65V
IO voltage1	SBCLK, FSYNC, SDIN, SDOUT, IRQZ, SDA, SCL, PWM_CTRL, SDZ	-0.3V to 5V
IO voltage2	MUTEN, ADDR	-0.3V to 2V
Junction-to-ambient thermal resistance θ_{JA}		45.7°C/W
Junction-to-board thermal resistance θ_{JB}		5.36°C/W
Junction-to-case thermal resistance θ_{JC}		31.92°C/W
Junction-to-top characterization parameter ψ_{JT}		1.5°C/W
Junction-to-board characterization parameter ψ_{JB}		5.34°C/W
Ambient Temperature Range		-40°C to 105°C
Operating junction temperature T_J		-40°C to 150°C
Storage temperature T_{STG}		-65°C to 150°C
ESD Rating (NOTE 2)		
HBM (human body model)		±2kV
CDM (charged-device model)		±500V
Latch-Up		
Test Condition：JESD78F		+IT：200mA -IT：-200mA

***NOTE1**: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

***NOTE2**: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001*

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{AVDD}	Analog power supply	1.62	1.8	1.98	V
V_{IOVDD}	Digital IO supply	3	3.3	3.63	V
		1.62	1.8	1.98	V
V_{PVDDL}	Input voltage(functional) (NOTE 1)	2.7		5.5	V
	Input voltage(performance)	3.5		5.5	V
V_{PVDDH}	Input voltage(functional) (NOTE 1)	3		23	V
	Input voltage(performance)	4.5		23	
R_{SPK}	Speaker impedance	3.2	4		Ω

NOTE1: Device will remain functional but performance will degrade.

Electrical Characteristics

Test condition: T_A = 25°C, PVDDH = 18V, PVDDL = 3.8V, AVDD = 1.8V, IOVDD = 1.8V, R_L = 4Ω + 33μH, fin = 1kHz, f_s = 48kHz, Gain = 23dBV, SDZ = 1, Power Mode 1(PSM enabled), unless otherwise noted.

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
Digital Logical Interface						
VIH	Logic input high level	SBLK、FSYNC、SDIN、SCL、SDA	0.7xIOVDD			V
VIL	Logic input low level				0.3xIOVDD	
VIH(SDZ)	Logic input high level	SDZ	0.7xIOVDD			V
VIL(SDZ)	Logic input low level	SDZ			0.3xIOVDD	
VOH	Logic output high level		0.7xIOVDD			V
VOL	Logic output low level				0.3xIOVDD	V
IIH	Input logic-high leakage for digital inputs	All digital pins; Input = Supply Rail.	-1		1	uA
IIL	Input logic-high leakage for digital inputs	All digital pins; Input = GND.	-1		1	uA
IO	Output Current Strength	Measured at 0.4V below supply and 0.4V above GND.		8		mA

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
Class-D Amplifier performance						
P_O	Peak Output Power	THD+N = 1%		30		W
THD+N	Total armonic distortion	P_O = 1W, fin = 1kHz		-80		dB
IMD	Inter-Modulation Distortion	ITU-R, 19kHz / 20kHz, 1:1:12.5W		-84		dB
DNR	Dynamic range	A-weighting, -60dBFS, PWR_MODE1		109		dB
		A-weighting, -60dBFS, PWR_MODE2		109		
		A-weighting, -60dBFS, PWR_MODE0		107		
SNR	Signal to Noise Ratio	A-Weighted, Referenced to 1% THD+N Output Level		110		dB
		A-Weighted, Referenced to 1% THD+N Output Level, PWR_MODE2		110		
		A-Weighted, Referenced to 1 % THD+N Output Level, PWR_MODE0		106		
V_N	Idle-channel noise	A-weighting, 20~20kHz, PWR_MODE1		28		uV
		A-weighting, 20~20kHz, PWR_MODE2		28		
		A-weighting, 20~20kHz, PWR_MODE0		40		
η	System efficiency	P_O = 1W, PVDDL = 5V, PWR_MODE1		84		%
		P_O = 1W, PVDDL = 5V, PWR_MODE0		80		
		P_O = 3W, PVDDL = 5V		87		
		P_O = 8W, PVDDL = 5V		89		
F_{PWM}	Class-D PWM Switching Frequency	Average frequency in Spread Spectrum Mode		384		kHz
		Fixed Frequency Mode, f_s = 44.1kHz and 88.2kHz		352.8		

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
		Fixed Frequency Mode, f_s = 48kHz and 96kHz		384		
V_{OS}	Output Offset Voltage	Idle Mode	-1.5		1.5	mV
	Mute attenuation	Device in Software Shutdown or Muted in normal operation		108		dB
PSRR	PSRR on PVDDH	PVDDH = 18V + 200mVpp & 217Hz		87		dB
		PVDDH = 18V + 200mVpp & 1kHz		85		
	PSRR on PVDDL	PVDDL = 5V + 200mVpp & 217Hz		86		
		PVDDL = 5V + 200mVpp & 1kHz		82		
	PSRR on AVDD	AVDD = 1.8V + 200mVpp & 217Hz		90		
		AVDD = 1.8V + 200mVpp & 1kHz		90		
	Turn ON Time from Release of Software Shutdown	No Volume Ramping		0.5		ms
		Volume Ramping		10.5		
	Turn OFF Time From Assertion of Software Shutdown to Amp Hi-Z	No Volume Ramping		0.1		
		Volume Ramping		10.5		
Die Temperature Sensor						
	Minimum Temperature Measurement Range			-40		°C
	Maximum Temperature Measurement Range			150		°C
	Die Temperature Resolution			1		°C
	Die Temperature Accuracy		-5		5	°C
Voltage Monitor						
	PVDDH	Minimum Level		3		V

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
	Measurement Range	Maximum Level		23		
	PVDDH Resolution			27		mV
	PVDDL Measurement Range	Minimum Level		2.7		V
		Maximum Level		5.5		
	PVDDL Resolution			20		mV
TDM Serial Audio Port						
	Minimum PCM Sample Rates and FSYNC Input Frequency			32		kHz
	Maximum PCM Sample kHz Rates and FSYNC Input Frequency			192		
	Minimum SBCLK Input Frequency	I2S/TDM Operation		0.512		MHz
	Maximum SBCLK Input Frequency	I2S/TDM Operation		24.576		
	SBCLK Maximum Input Jitter	RMS Jitter below 40kHz that can be tolerated without performance degradation		0.5		ns
		RMS Jitter above 40kHz that can be tolerated without performance degradation		1		
	Minimum SBCLK Cycles per FSYNC in I2S and TDM Modes	Other Values: 24, 32, 48, 64, 96, 125, 128, 192, 250, 256, 384, 500		16		
	Maximum SBCLK Cycles per FSYNC in I2S and TDM Modes	Other Values: 24, 32, 48, 64, 96, 125, 128, 192, 250, 256, 384, 500		512		
PCM Playback Characteristics fs ≤ 48kHz						
f_S	Minimum Sample Rate			32		kHz
	Maximum Sample Rate			48		
	Passband Frequency Meeting Ripple			0.443		f_S
	Passband Ripple	20Hz to LPF cutoff frequency	-0.5		0.5	dB
	Stop Band	≥ 0.55f_S		60		dB

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
	Attenuation	≥ 1f_S		65		
PCM Playback Characteristics fs ＞ 48kHz						
f_S	Minimum Sample Rate			88.2		kHz
	Maximum Sample Rate			192		
	Passband Ripple	DC to LPF cutoff frequency	-0.5		0.5	dB
	Stop Band Attenuation	≥ 0.56f_S		60		dB
		≥ 1f_S		65		
Speaker Voltage Sense						
	Resolution			16		Bits
VFS_VSNS	Full scale input voltage			30.67		V_{PK}
DNR	Dynamic Range	Un-weighted, relative to 0 dBFS		-80		dB
THD+N	Total Harmonic Distortion and Noise	P_O = 1W		-61		dB
	Frequency Response	20Hz – 20kHz	-0.15		0.15	dB
Speaker Current Sense						
	Resolution			16		Bits
IFS_ISNS	Full scale input current	Measured @-6dBFS, re-scale to 0dBFS		10		A
DNR	Dynamic Range	Un-weighted, relative to 0 dBFS		-70		dB
THD+N	Total Harmonic Distortion and Noise	P_O = 1W		-54		dB
Speaker Voltage/current Sense Ratio						
	Gain Linearity	P_O ≥ 40mW to 0.1% THD+N, using a 35Hz -40dBFS pilot tone, PWR_MODE0	-1		1	%
	Gain Linearity	P_O ≥ 80mW to 0.1% THD+N, using a 40Hz -40dBFS pilot tone, PWR_MODE1	-2		2	%
PROTECTION CIRCUITRY						

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
	Thermal Shutdown Temperature				150	°C
	Output Over Current Limit on PVDDH	Output to Output, Output to GND or Output to PVDDH Short	5.5	6.5		A
	Output Over Current Limit on PVDDL	Output to Output, Output to GND or Output to PVDDL Short	1.8	2.5		A
	PVDDL Undervoltage Lockout Threshold	UVLO is asserted		2.01		V
		UVLO is de-asserted		2.17		
	PVDDH Undervoltage Lockout Threshold	UVLO is asserted		2.45		V
		UVLO is de-asserted		3.08		
	AVDD Undervoltage Lockout Threshold	UVLO is asserted		1.44		V
		UVLO is de-asserted		1.51		
	IOVDD Undervoltage Lockout Threshold	UVLO is asserted		1.18		V
		UVLO is de-asserted		1.26		
	PVDDL Internal LDO Undervoltage Lockout Threshold	UVLO is asserted		4.1		V
CLASSH CONTROLLER						
	Look Ahead Time	Sampling Rates 48kHz and 96kHz			4	ms
Beep Pin Generator						
fin	SDZ Pin	Input PWM signal frequency	25.6		192	kHz
Typical Current Consumption						
	Hardware shutdown	SDZ = 0, PVDDH		0.02	1	uA
		SDZ = 0, PVDDL		0.02	1	
		SDZ = 0, AVDD		0.09	1	
		SDZ = 0, IOVDD		0.002	1	
	Software	SDZ = 1, All clocks		0.04	1	uA

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
	shutdown	stoped, PVDDH				
		SDZ = 1, All clocks stoped, PVDDL		0.75	2	
		SDZ = 1, All clocks stoped, AVDD	5	12	25	
		SDZ = 1, All clocks stoped, IOVDD		0.4	1	
	Noise gate	f_s = 48kHz, PVDDH		0.02	0.1	mA
		f_s = 48kHz, PVDDL		0.08	0.15	
		f_s = 48kHz, AVDD	2	4.9	8	
		f_s = 48kHz, IOVDD		0.005	0.01	
	Idle mode-PWR_MODE1	f_s = 48kHz, PVDDH		0.07	0.15	mA
		f_s = 48kHz, PVDDL	2	4	6.5	
		f_s = 48kHz, AVDD, IV sense open	3	7	12	
		f_s = 48kHz, AVDD, IV sense close	2	5	9	
		f_s = 48kHz, IOVDD		0.005	0.01	
	Idle Mode - PWR_MODE2	f_s = 48kHz, PVDDH	2	5	8	mA
		f_s = 48kHz, AVDD, IV Sense = Enabled	3	7	12	
		f_s = 48kHz, AVDD, IV Sense = Disabled	2	5	9	
		f_s = 48kHz, IOVDD		0.005	0.01	
	Idle Mode - PWR_MODE0	f_s = 48kHz, PVDDH	3	6	8	mA
		f_s = 48kHz, PVDDL	2	4	7	
		f_s = 48kHz, AVDD, IV Sense = Enabled	3	7	12	
		f_s = 48kHz, AVDD, IV Sense = Disabled	2	5	9	
		f_s = 48kHz, IOVDD		0.005	0.01	

I2C INTERFACE TIMING

Parameter			Fast mode			Fast mode Plus			UNIT
No.	Sym	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.26			μs
7	$t_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			0.26			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	The Bus idle time START state to STOP state	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	10			10			ns

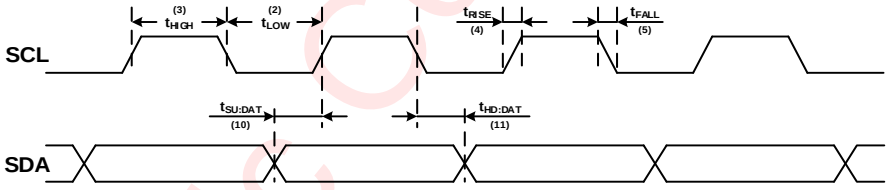


Figure 5 SCL and SDA timing relationships in the data transmission process

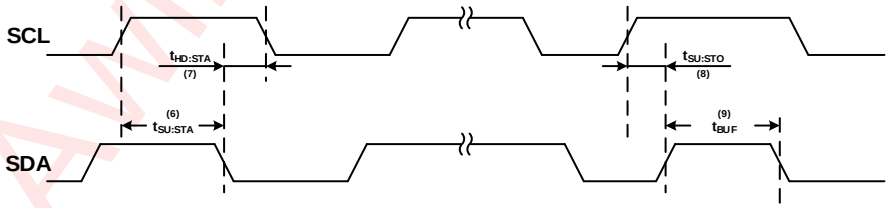


Figure 6 The timing relationship between START and STOP state

DIGITAL AUDIO INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin LRCLK	32		192	kHz
f_{bck}	Bit clock frequency, on pin SCLK	16*fs		24.576M (NOTE1)	Hz
t_{su}	LRCLK, SDIN Setup time to SCLK	10			ns
t_h	LRCLK, SDIN hold time to SCLK	10			ns
t_d	GPIO2 output delay time to SCLK			30 (NOTE2)	ns

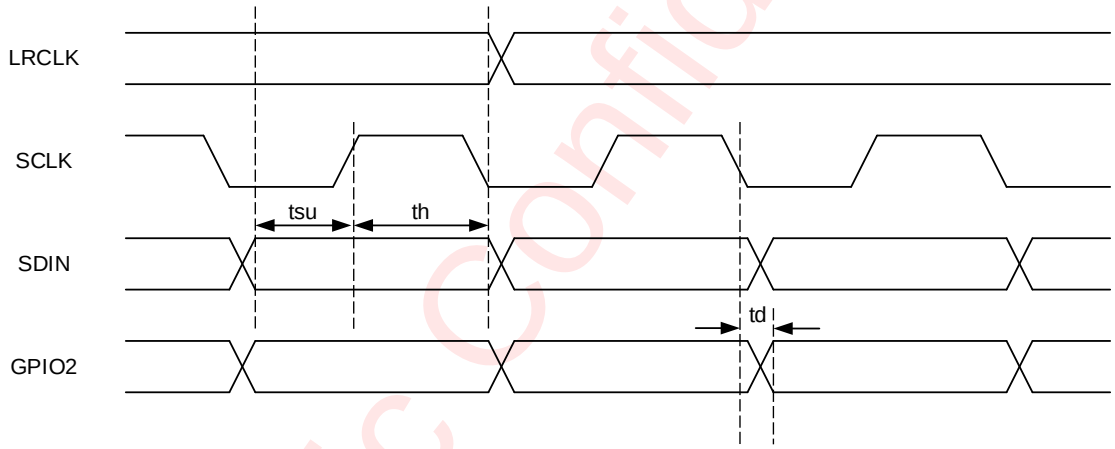


Figure 1 Digital Audio Interface Timing

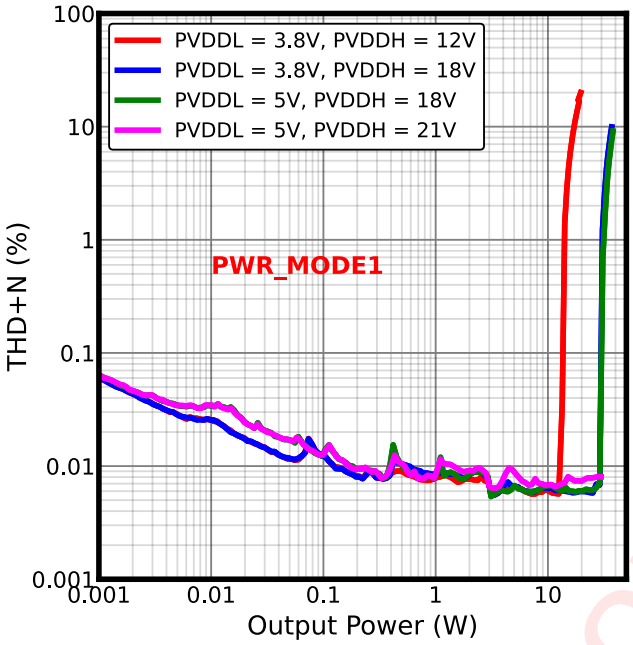
***NOTE1**: The digital audio interface support up to 16 slots（32-bit） at a 32/44.1/48 kHz sample rate 8 slots（32-bit）at a 88.2/96 kHz and 4slots (32-bit) at a 192kHz sample rate*

***NOTE2**: Calculating t_d based on 32ns in 8-parallel PA applications. When PA count ≥6, enable I2S_DRV_STREN register to boost driver current for preventing waveform distortion.*

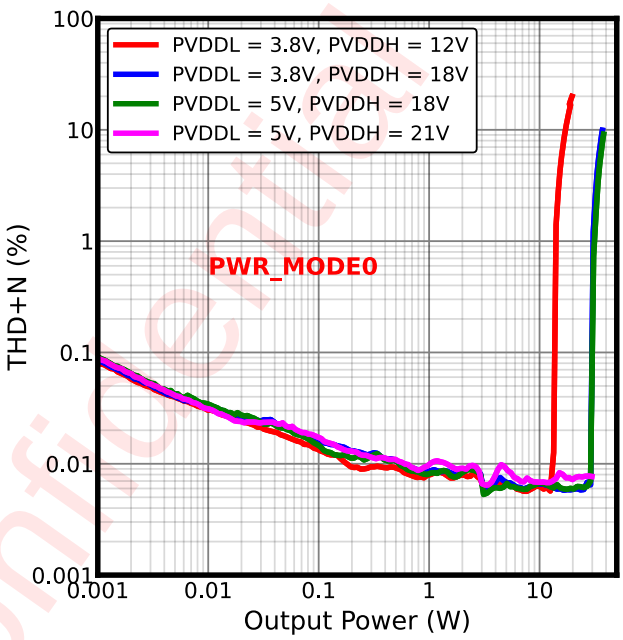
Typical Characteristics Curves

Test condition: TA = 25°C, AVDD=1.8V, IOVDD=1.8V, f_s = 48kHz, F_{PWM} = 384kHz, fin = 1kHz, R_L = 4Ω + 33μH, unless otherwise noted.

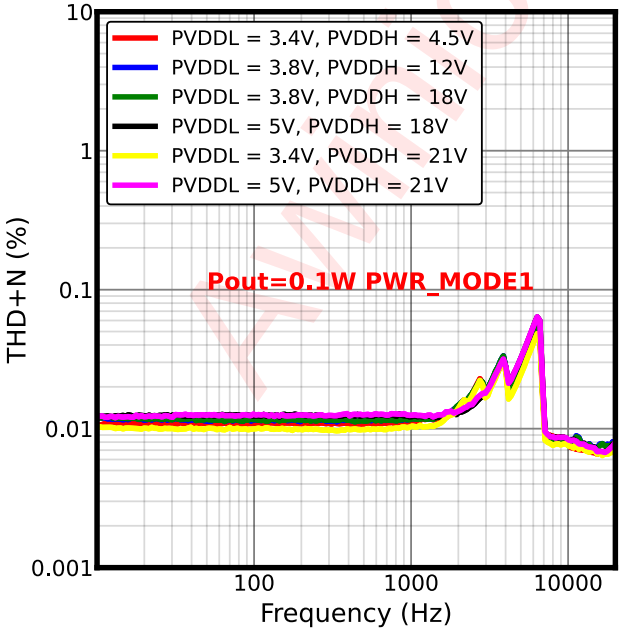
THD+N VS. Output Power



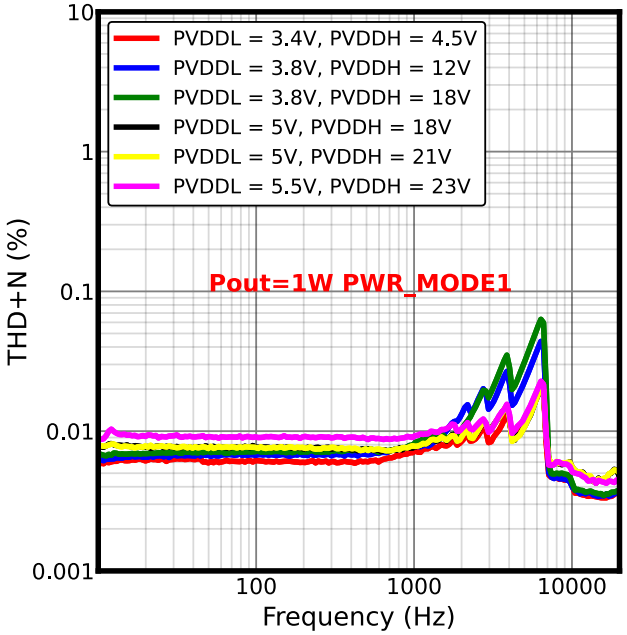
THD+N VS. Output Power



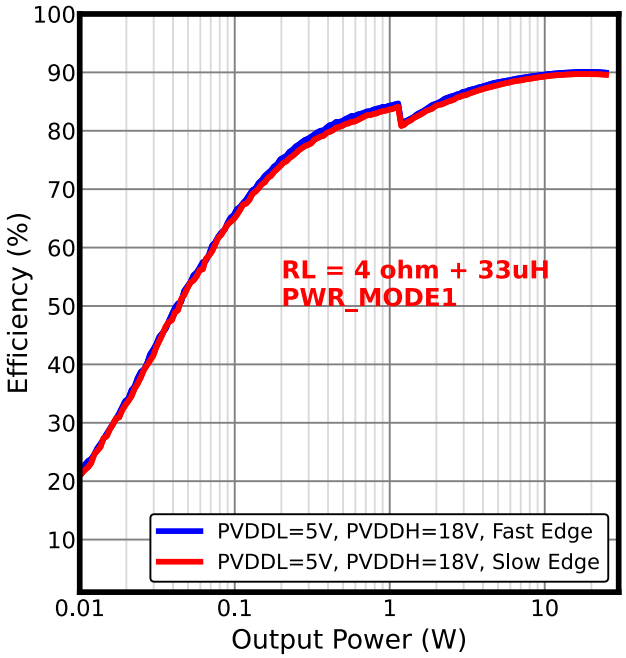
THD+N VS. Frequency



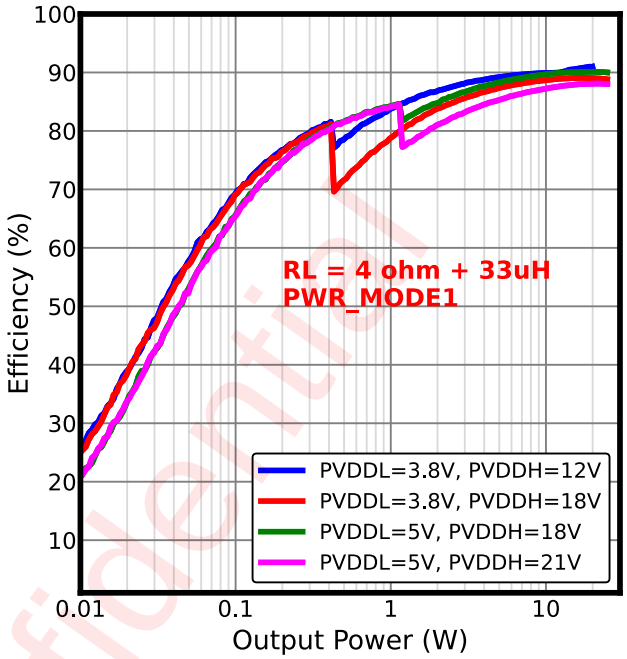
THD+N VS. Frequency



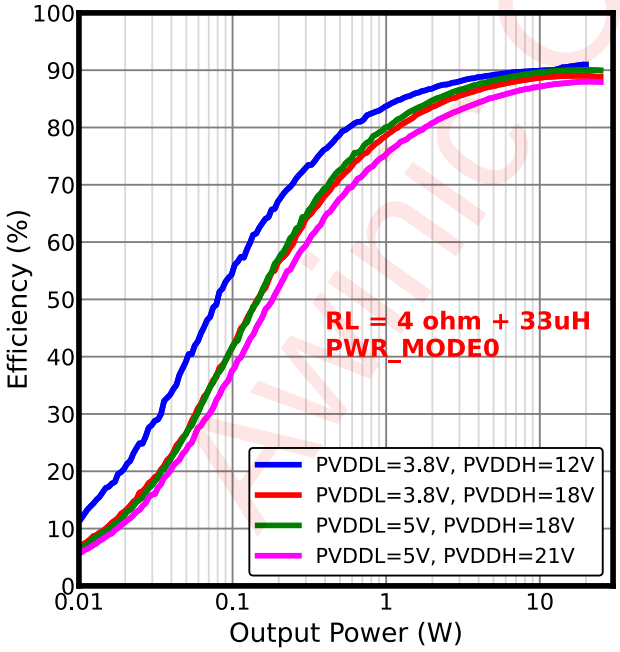
Efficiency VS. Output Power



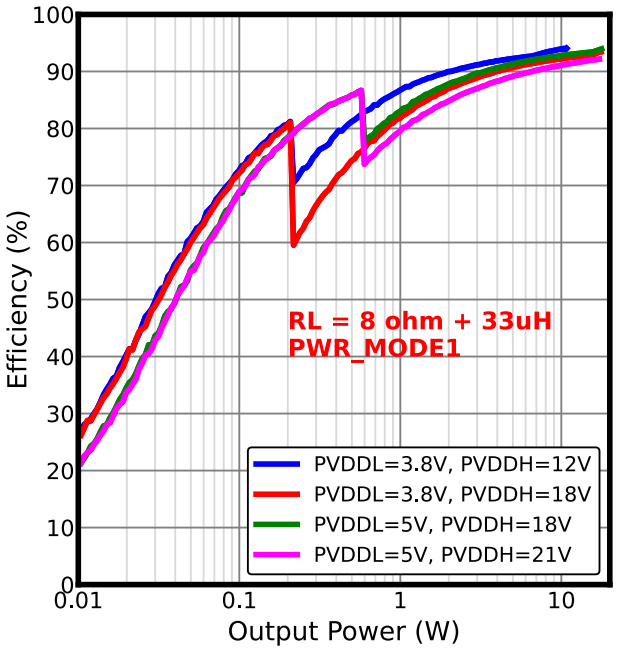
Efficiency VS. Output Power



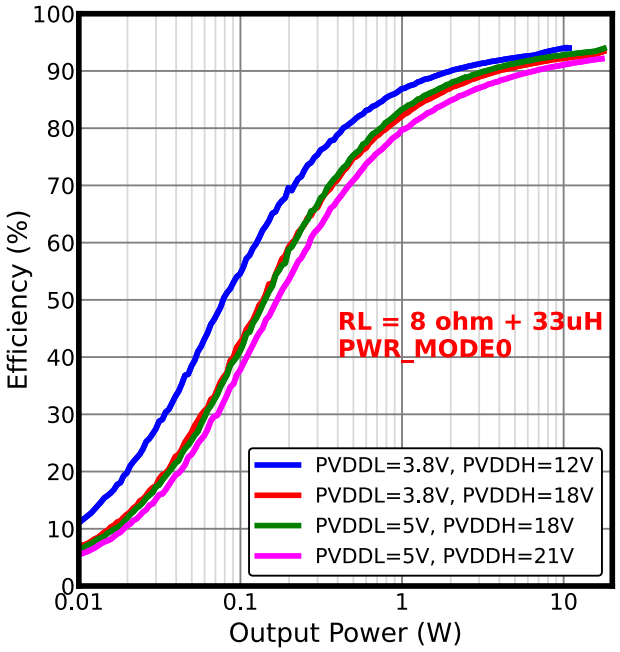
Efficiency VS. Output Power



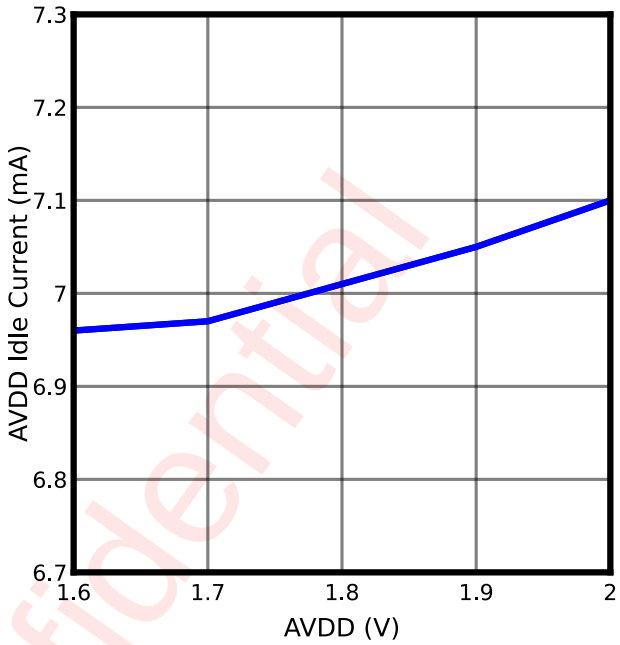
Efficiency VS. Output Power



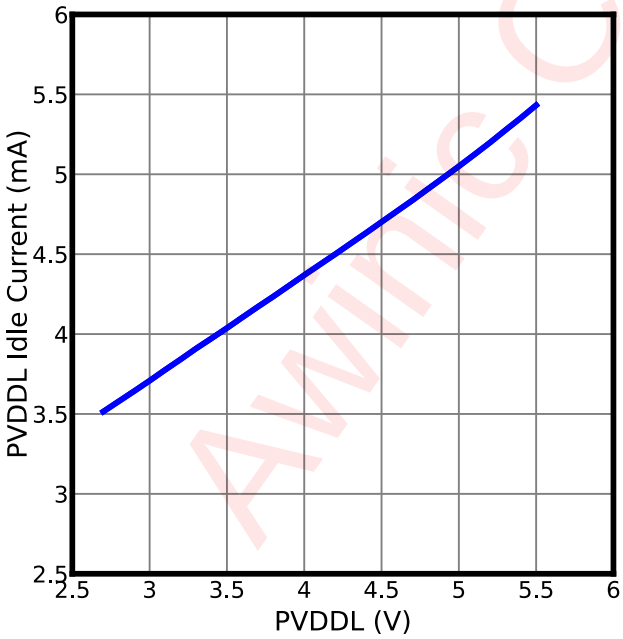
Efficiency VS. Output Power



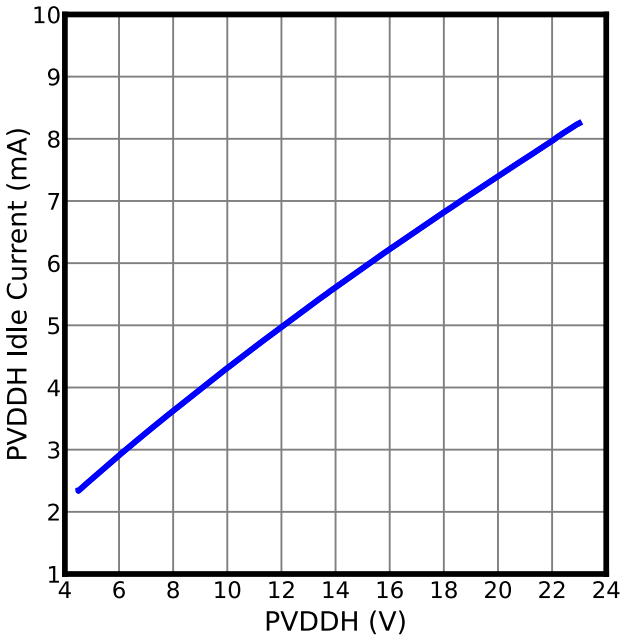
AVDD Idle Current VS. AVDD



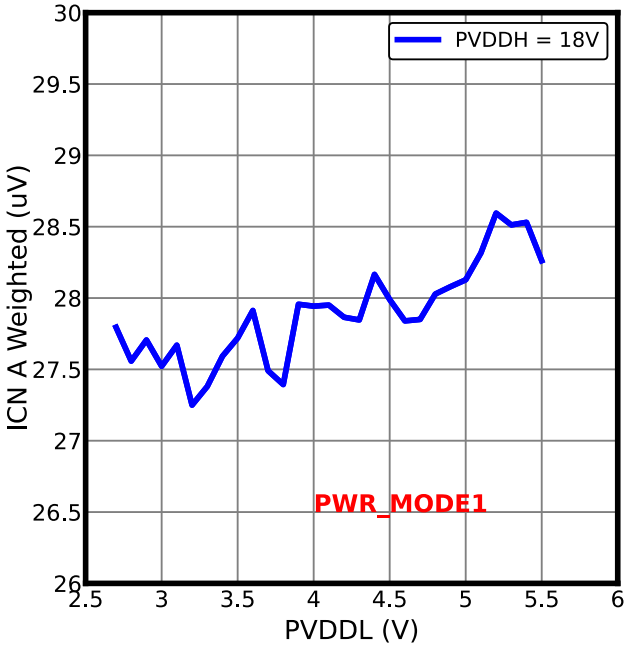
PVDDL Idle Current VS. PVDDL



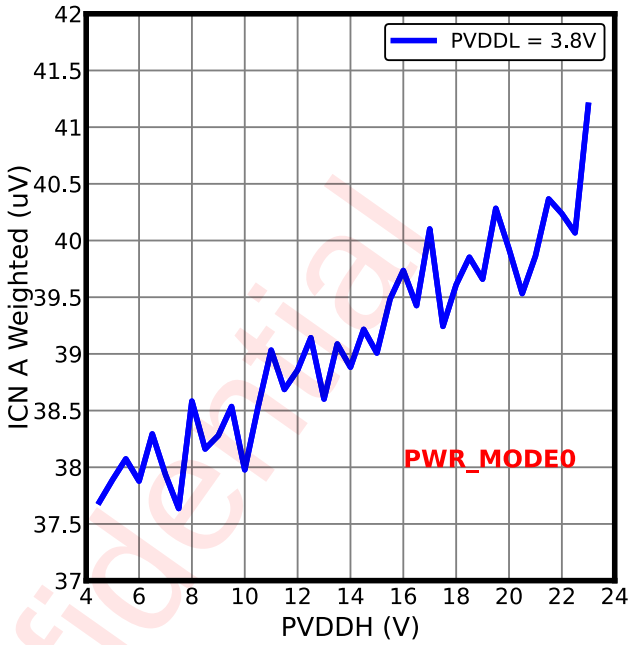
PVDDDH Idle Current VS. PVDDH



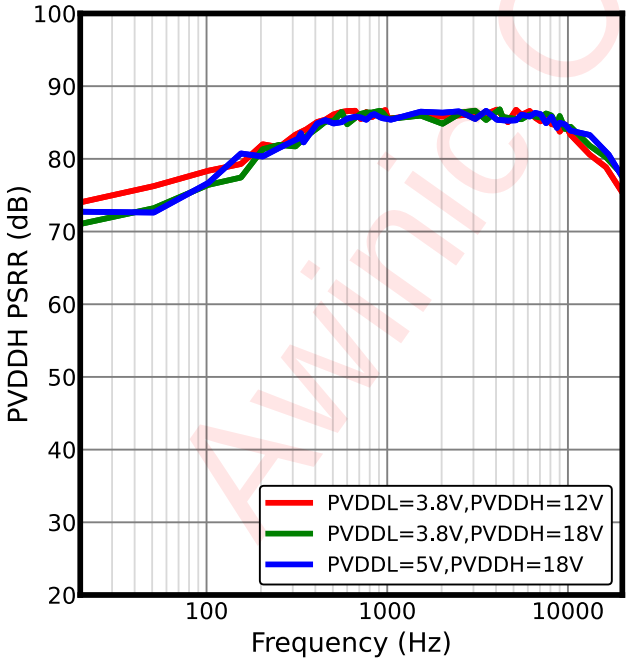
ICN A-Weighted VS. PVDDL



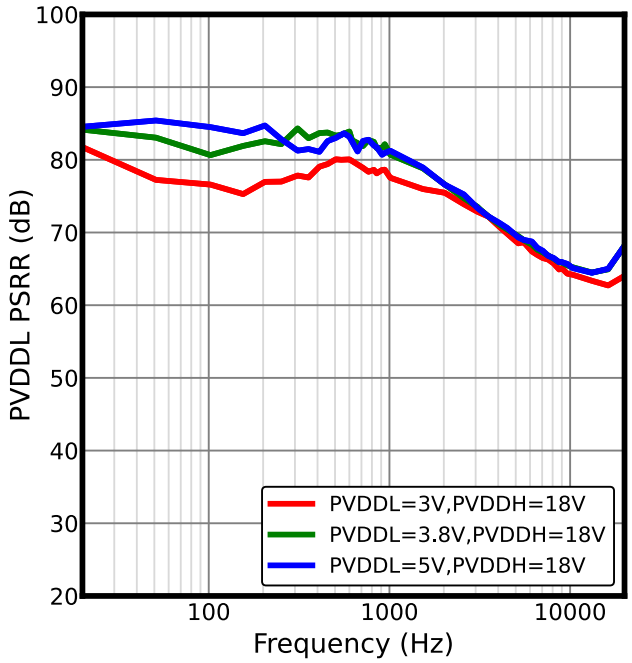
ICN A-Weighted VS. PVDDH



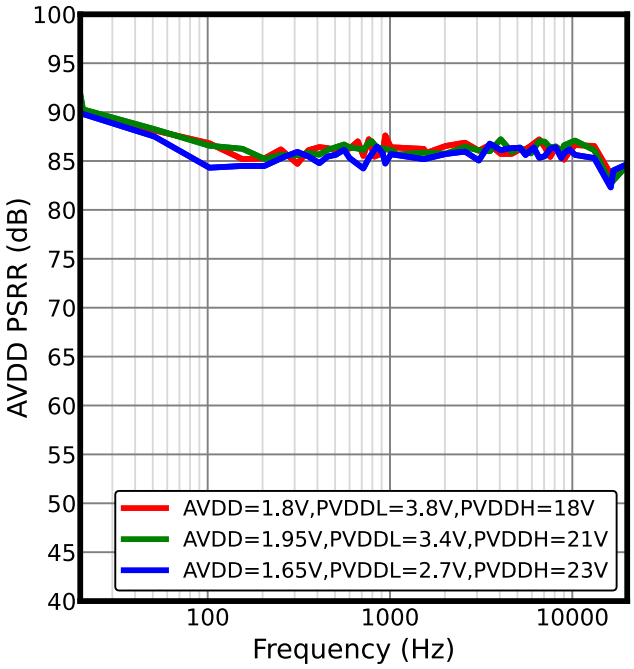
PVDDH PSRR VS. Frequency



PVDDL PSRR VS. Frequency



AVDD PSRR VS. Frequency



Detailed Functional Description

OPERATION MODE

POWER-DOWN MODE

In this mode, all circuits inside this device will be shutdown except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

By default, when SDZ pin goes low, the device will force a power-down mode after a timeout set by the configurable shutdown timer (register bits SDZ_DEG_TTH). If SDZ is asserted low while audio is playing, the device will ramp down volume of the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into power-down mode. The volume ramp down can be controlled using SDZ_VOL_RAMP register bits. The device can also be configured for forced power-down mode and in this case it will not attempt to gracefully disable the audio channel. The power-down mode can be controlled using SDZ_MODE register bits.

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK and SDZ pin is HIGH. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to stand-by mode when the device is no needed to work.

CONFIG MODE

The device switches to OFF mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 1;

In this mode the internal bias, OSC and PLL modules will start to work.

OPERATING MODE

The device is fully operational in this mode. Amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.

This device power up sequence is illustrated in the following figure :

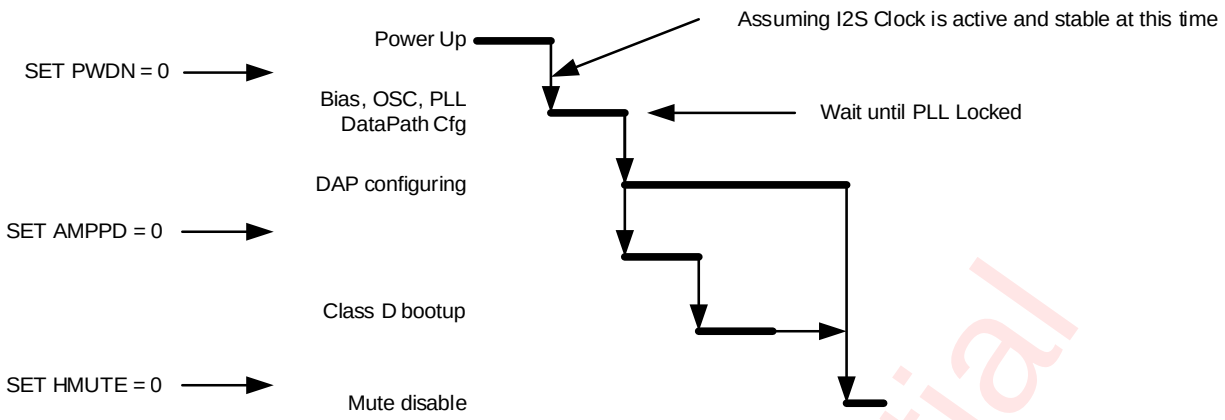
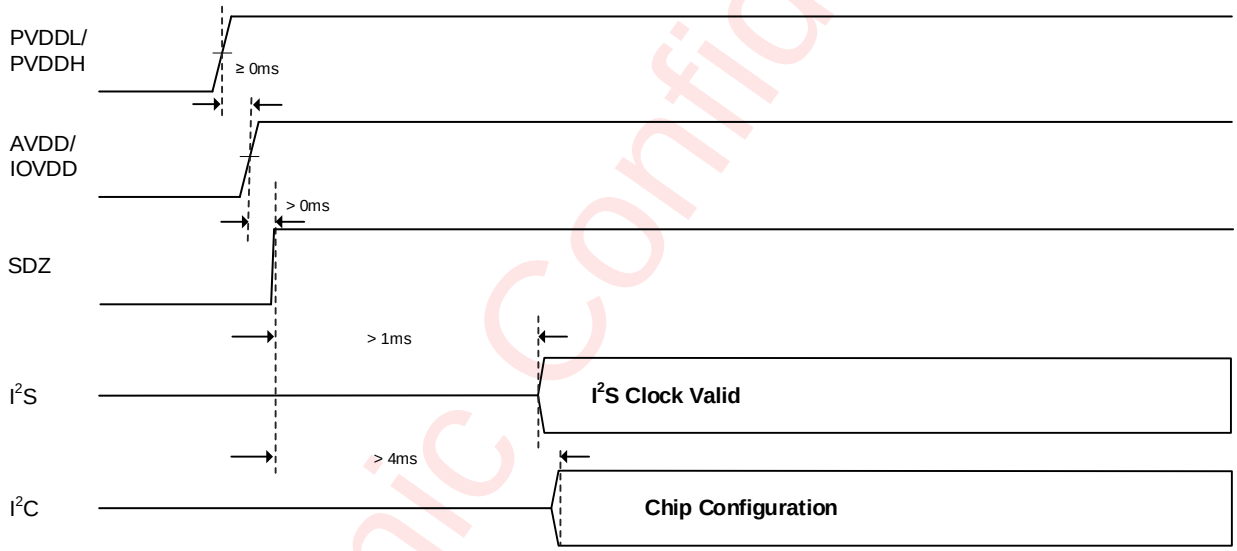


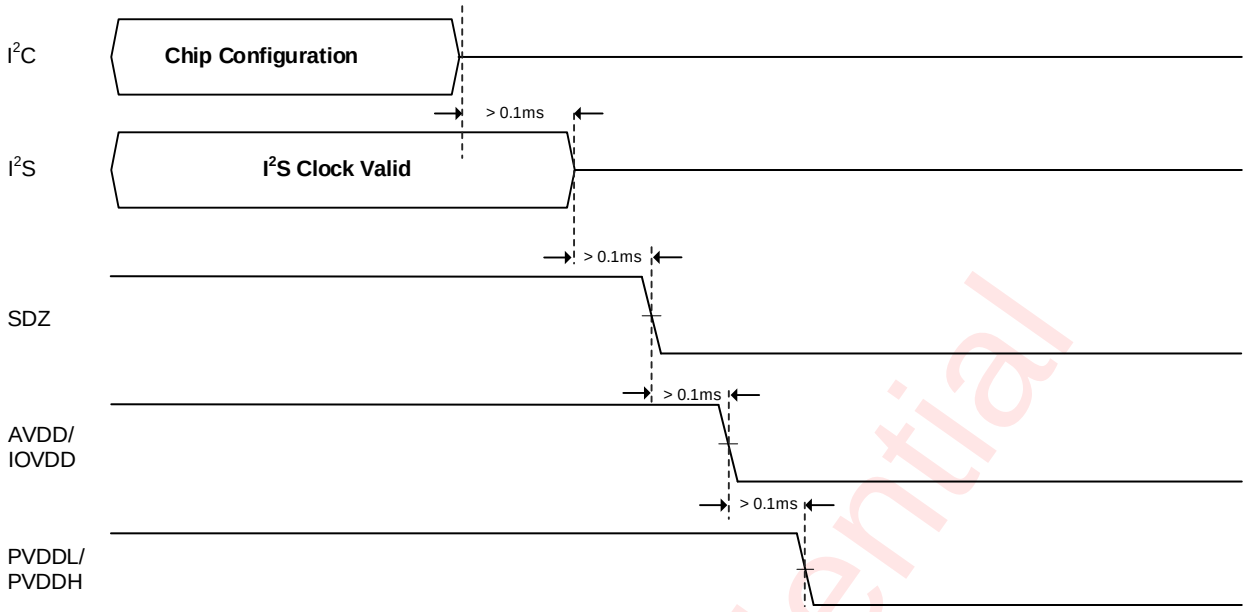
Figure 2 Power up sequence

Power up sequence considering I²S, I²C timing shows as below（NOTE1）:



***NOTE1**: SDZ must not be pulled high until AVDD is fully established.*

Power down sequence considering I²S, I²C timing shows as below:



BEEP MODE

Through applying pulses on the SDZ pin, the beep generation can happen when the device is in standby, config or operating mode. This beep generator produces a simple audio tone (beep) that is transmitted directly to amplifier output, which have a frequency of the input pulse frequency divided 64.

A deglitch timer will hold-off the shut-down functionality until the tone has finished and the deglitch timer has expired in which case the pin will revert to controlling the hardware shutdown of the device.

The output power of the beep signal is controlled by the duty cycle of the input signal as show in the table below.

Load (Ω)	Duty Cycle (%)	Output Power (W)
8	20 - 30	0.2
8	45 - 55	0.4
8	70 - 80	0.8

SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL I/O STATUS

The state of each digital input and output are shown in below table. After power on, the input signal pin SCLK, LRCLK, SDIN are set to high impedance by default. If I2STXEN is enabled, SDOUT is actively driven when outputting data otherwise it is high impedance by default.

Table 1 Digital I/O status description

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
ADDR	Input	Weak pull down

Digital I/O	Type	Description (Default State)
SCLK	Input	Hi-Z
LRCLK	Input	Hi-Z
SDIN	Input	Hi-Z
SDOUT	Output	Hi-Z

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- SCLK
- LRCLK
- SDIN
- SDOUT

Two-slot I²S and 1/2/4/6/8/16-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock LRCLK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 32kHz, 44.1kHz, 48kHz, 96kHz and 192kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock SCLK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL4.I2SBCK. The frequency of SCLK can be calculated according to the following equation:

SCLK frequency = ***SampleRate*** * ***SlotLength*** * ***SlotNumber***

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of Sclk clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 1/2/4/6/8/16-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL). The frequency of word select signal should be larger than 32kHz when it is used as the reference clock of PLL.

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL.

Table 2 Supported I²S interface parameters

Interface format(MSB first)	Data width	Sclk frequency
Standard I²S	16b/20b/24b/32b	32fs/48fs/64fs
Left-justified	16b/20b/24b/32b	32fs/48fs/64fs

Interface format(MSB first)	Data width	Sclk frequency
Right-justified	16b/20b/24b/32b	32fs /48fs/64fs

The output port SDOUT, can be enabled or disabled via bit SYSCTRL3.I2STXEN. The unused slots can be set to Hi-z or normal working, which is controlled by I2SCTRL3.DOHZ.

STANDARD I²S MODE

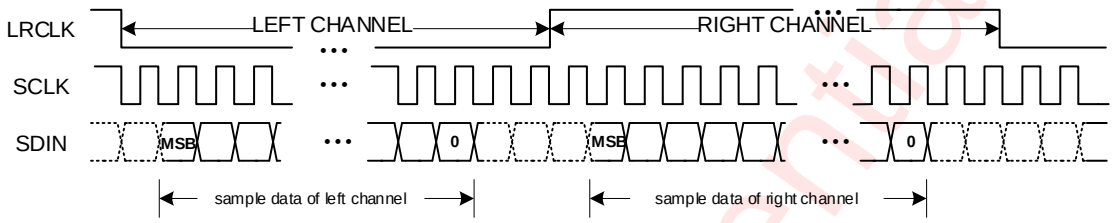


Figure 3 I²S Timing for Standard I²S Mode

- When LRCLK=0 indicating the left channel data, and LRCLK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

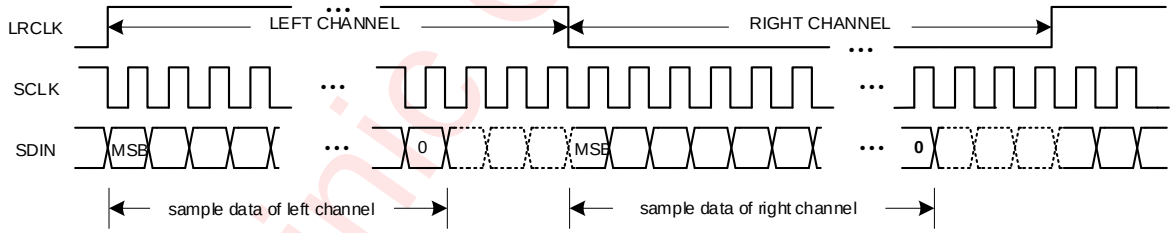


Figure 4 I²S Timing for Left-Justified Mode

- When LRCLK=1 indicating the left channel data, and LRCLK=0 indicating the right channel data.
- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

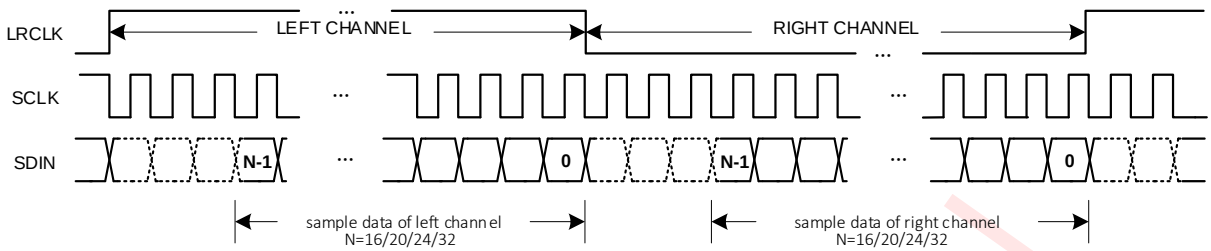


Figure 5 I²S Timing for Right-Justified Mode

- When LRCLK is high indicating the left channel data, and LRCLK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 1/2/4/6/8/16-slot is supported in TDM mode, while 2-slot is supported in I²S mode

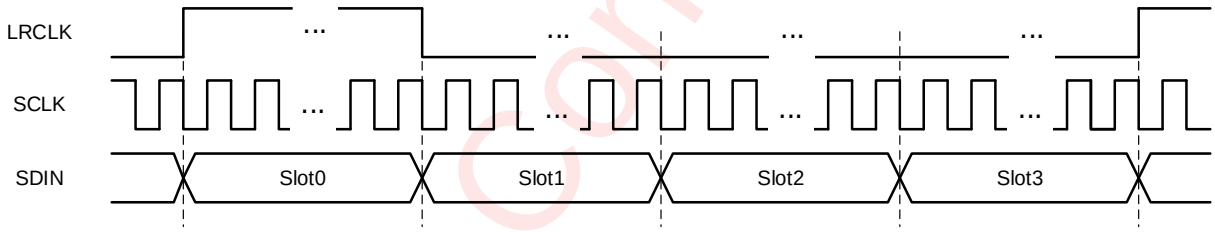


Figure 6 TDM Timing

Note: The high level pulse width of LRCLK signal can be one slot time or one period of SCLK.

ULTRASONIC APPLICATION

The device offers two modes for ultrasonic application via TDM/I²S running at 96kHz or 192kHz:

TDM Mode: Ultrasonic signal and audio signal could be sent into different slots of TDM/I²S separately, and then be mixed in the device.

Mixed Mode: Ultrasonic signal could be mixed with audio signal, and then be sent into one slot of TDM/I²S. In this mode, the frequency of ultrasonic signal should be larger than 25kHz.

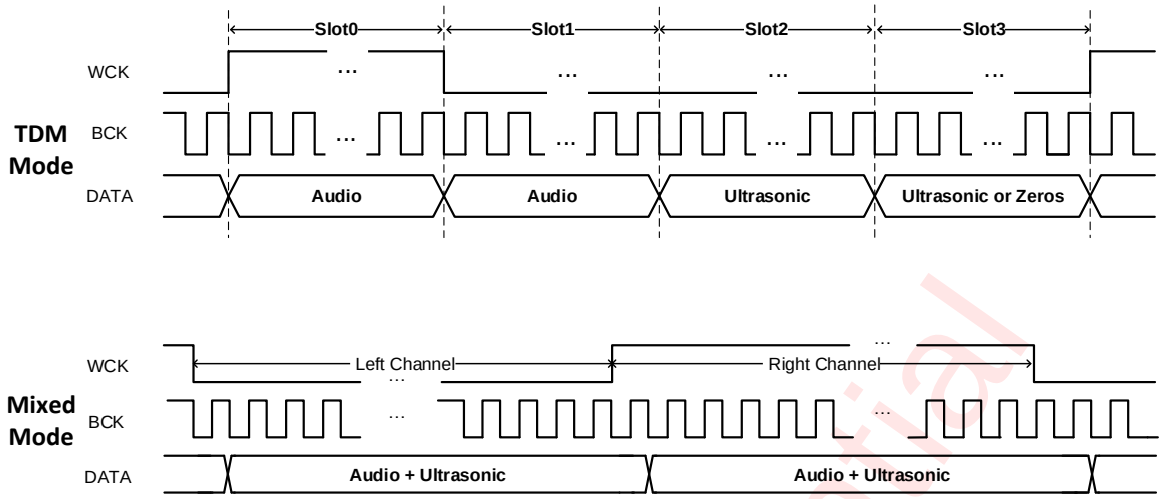


Figure 7 Ultrasonic Application for Two PA

DIGITAL AUDIO PROCESSING

This device incorporates one programmable Digital Audio Processor (DAP) block. It provides the algorithm for audio signal processing and speaker protection. The following functions are available in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the Digital Audio Processor (DAP) is illustrated in the following figure.

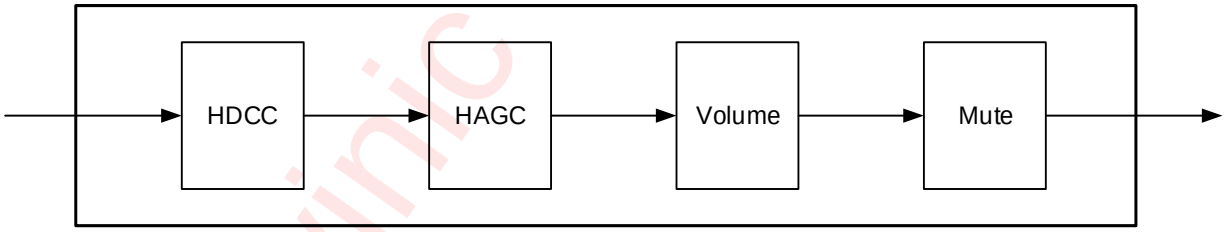


Figure 8 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker in the actual audio application, the overload signal can cause damage to the speaker if there is no output power control. The audio power amplifier with HAGC can protect the speaker effectively. When the output power is not exceeds the setting threshold, the

HAGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the HAGC module will reduce the internal gain of amplifier and restrict the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0dB to -96dB with 0.094dB/step.

MUTE

This module performs mute control for the audio stream. When setting DACCFG6.FADE_EN to 1, if mute is asserted, volume of the Class-D amplifier will be ramped down to a mute state, if mute is de-asserted, the device will ramp volume back to the programmed digital setting.

DEVICE FUNCTIONAL MODES

PVDDL SUPPLY

The AW85281 can operate with or without a PVDDL supply. When configured without a PVDDL supply, the PVDDH voltage will be used with an internal LDO to generate this supply voltage. A 1uF decoupling capacitor is needed. In this case, CDS_MODE[1:0] bit should be set to 11 and LDO5V_EN=1, LDO_5V_EN_PVDDL=1 before transitioning from Software Shutdown mode.

POWER SAVING MODE

This feature is enabled by setting CDS_MODE[1:0] bits to 2'b00 when both PVDDH and PVDDL are supplied to the device. When PVDDL is the power supply of class-D output, it is in Power Saving Mode (PSM). The main purpose of PSM is to improve the efficiency when the output power is low. There are two options of power switch threshold can be configured, one is a constant input threshold, the other is a hysteresis threshold relative to the PVDDL voltage.

If not configured to PSM mode the device will use only the selected supply for Class-D output even if clipping would otherwise occur. The device can operate using only PVDDH to supply Class-D output. In this configuration the PVDDL can be provided from external supply (register bit LDO5V_EN=0, LDO_5V_EN_PVDDL=0) or generated by an internal LDO (register bit LDO5V_EN=1, LDO_5V_EN_PVDDL=1). In this case CDS_MODE[1:0] bits should be set to 2'b10. The AW85281 PSM with low power on PVDDL can be used to switch to the PVDDL rail only at very low power when close to idle. This will reduce the Class-D output swing when near idle and limit the current requirements of the PVDDL supply. Set the CDS_MODE[7:6] register to 2'b11 for this mode.

NOISE GATE MODE

The noise gate functionality allows the amplifier to stop switching in order to reduce power consumption during passages of ultra-low input signal, When the input audio signal keep smaller than the noise gate threshold for more than deglitch time, the amplifier enters noise-gated condition, then the amplifier's output (OUTP/OUTN) switching is disabled and the Class-D is powered down. This eliminates the power consumption of the output switching, produces a state of very low idle noise and idle current. When exiting the noise-gated condition, the simplifier immediately resumes normal operation.

OUTPUT SLEW RATE CONTROL

The output slew rate can be programmed using register bits GDTX_EDGE[4:3] , register 0x53 .

By default, if PVDDH supply is below 20V. the output slew rate will be at a fast rate (GDTX_EDGE[4:3]=10), dependant on supply and load. If PVDDH goes above 20V the slew rate will be automatically change to a slower rate.

Optionally, to improve EMI performance, user can set the slew rate to a slower rate for the entire range of PVDDH supply by setting the bits GDTX_EDGE[4:3] to 2'b11.

SAR ADC

A SAR ADC monitors PVDDH voltage, PVDDL voltage, die temperature and Power MOS temperature. The results of these conversions are available via register readback (PVDDH [9:0], PVDDL[9:0], TEMP1[9:0] and TEMP2[9:0] register bits).

PVDDH and PVDDL voltage conversions are also used by the limiter and brown out prevention blocks.

The ADC runs at a fixed 192kHz/96kHz/48kHz sample rate with a conversion time of 5.2 μs/10.4us/20.8us. Every temperature is sampled once every 4th SAR conversions, when Tsensor worked in mode0. And when Tsensor worked in mode1, the two temperatures are sampled once every 8th SAR conversions.

PVDDH and PVDDL voltages, die temperature and Power MOS temperature are calculated using equations from Registers 0x23, 0x22, 0x21 and 0x24. The register bits content should always be read from MSB to LSB.

CURRENT AND VOLTAGE (IV) SENSE

The AW85281 provides speaker voltage and current sense measurements for real time monitoring of loudspeaker behavior. The VSNSP and VSNSN pins should be connected after any ferrite bead filter (or directly to the OUTP and OUTN connections if no EMI filter is used). The V-Sense connections eliminate voltage drop error due to packaging, PCB interconnect or ferrite bead filter resistance. It should be noted that any interconnect resistance after the VSNS terminals will not be corrected for, so it is advised to connect the sense connections as close to the load as possible.

The voltage and current sense internal ADCs have a DC blocking filter. This filter cut-off frequency can be adjusted, or the filter can be bypassed.

I-Sense and V-Sense blocks can be powered up by setting the EN_ISENSE[0X2A, bit3] and EN_VSENSE[0X2A, bit1] register bits to low.

ULTRASONIC

The AW85281 has a dedicated power mode (PWR_MODE3) to play ultasound in advance ultrasonic applications like presence detection, gesture recognition, etc.

In PWR_MODE3 mode of operation the output stage of Class-D will be supplied by external PVDDL rail.

POWER TRACKING CONTROL

The dynamic range of audio signals is large, and in order to ensure that the output is not distorted, the power supply voltage needs to cover the maximum output voltage of the audio. In most cases, using a fixed maximum output voltage of the audio for power supply is inefficient and causes a lot of heat loss. AW85281 can dynamically

track the envelope of audio signals, analyze and obtain the minimum undistorted power supply voltage, and transmit PWM control signals to external DC-DC converters through GPIO pins to regulate the power supply voltage. The entire system always directly matches the requirements of audio signals, rather than just maintaining the voltage required for maximum power usage. The power loss in the system is reduced, and the efficiency is significantly improved.

The PTC function will detect the input audio signal in advance, and the advance amount is controlled by PTC_CFG0 bit [1:4]. When the audio signal decreases, the PVDD will not immediately decrease, but will remain for a period of time named PTC_TIME (PTC_CFG [5:7]), and the speed of PVDD reduction can be controlled by setting PTC_STEP (VPC_CFG1 bit [9:11]). At the same time, the PTC function can be selected from two modes, with Advanced mode providing PVDD closer to the signal distortion limit, while Normal mode is relatively conservative.

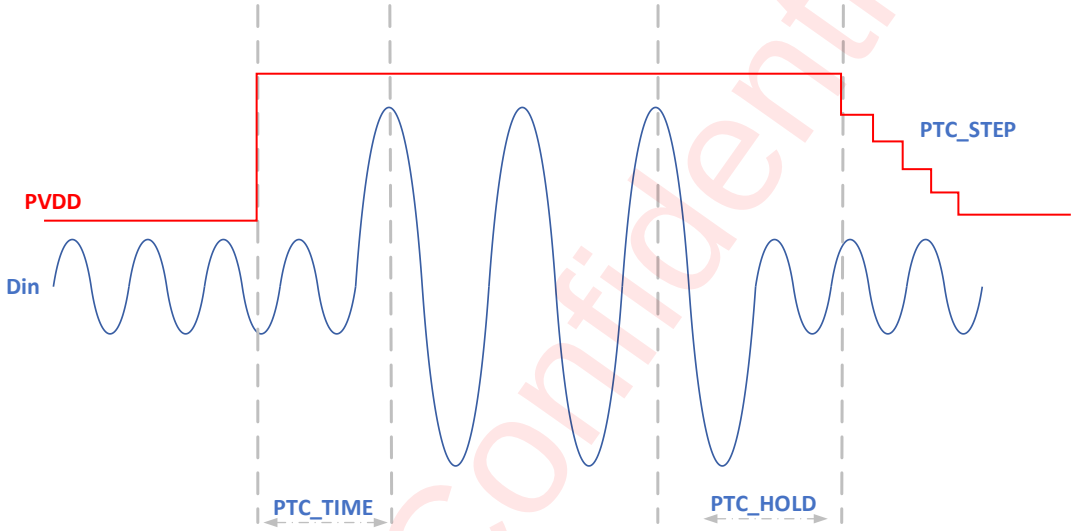


Figure 1 Power Tracking Supply

AUTO VOLTAGE MONITOR

When the supply voltage changes due to sudden transients and declining battery life, the AVM automatically optimizes the signal amplitude to avoid distortion.

DEVICE PROTECTION MECHANISMS

Over current Protection (OCP)

For PVDDL supply below 3.4 V the power FETs can go into saturation at higher load currents which could result in device damage due to the FETs connected to PVDDH going into thermal runaway. To prevent the damage the OCP limit is adjusted based on PVDDL level measured by the internal SAR ADC. Lower PVDDL level will correspond to lower OC limit setting.

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the CLASSD Amplifier outputs enter high impedance immediately if the peak current increases to large enough. The Amplifier shutdown speed depends on some factors, such as the impedance of the short circuit,

PVDD supply voltage, and PWM switching frequency. The host can restart the Amplifier via config I2C.The OCP event will be indicated on the fault pin, and the I2C register saves a fault record. If the output current is strong enough to exceed the peak current threshold but not severe enough to trigger the OCP, the peak current limiter works to prevent excess current from damaging the device, and the output returns to normal operate state while the short is removed.

DC Detect (DC)

If the AW85281 device detects the DC offset of the output voltage, if the different output exceed 1.9V for a long time, the device be judged as an DC error, the FAULT Pin is pulled low and the CLASSD outputs transition to high impedance, signifying a fault. The host can restart the Amplifier via config I2C.

Over Voltage Protection (OVP)

The circuit has integrated the over voltage protection control loop. When the output voltage PVDDL/PVDDH is above the threshold, the CLASSD Amplifier will stop working, until the voltage of PVDDL/PVDDH going down and under the normal fixed working voltage.

Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when PVDDL/PVDDH/IOVDD/AVDD under voltage occurs, and the interrupt bits will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected under-voltage event has taken place.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). The protection mechanism is based on two thresholds TEMP1 and TEMP2. When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 140°C), the output stages will start to operate normally again.

Thermal Foldback (TFB)

The device has automatic output power attenuation mechanism when the junction temperature exceeds the configured threshold (default = 100°C). When it happens, the internal gain of amplifier will be reduced automatically to a setting threshold, to prevent the device from shutting down due to over-temperature. When the junction temperature drops below the preset temperature low threshold (less than 95°C), the attenuation will start to releasing.

POWER SUPPLY RECOMMENDATIONS

The power sequence between the supply rails can be applied in any order as long as SDZ pin is held low. Once all supplies are stable the SDZ pin can be set high to initialize the part. After a hardware or software reset additional commands to the device should be delayed for at least 1 ms to allow the OTP memory to load.

When PVDDL is internally generated it is recommended that the device enters Software Shutdown mode before entering Hardware Shutdown mode. This ensures that PVDDL pin is discharged using the internal 5 kOhms pull down resistor (not present in Hardware Shutdown mode).

The AW85281 can operate with both PVDDL and PVDDH as supplies or with only PVDDH or PVDDL as supply. The table below shows different power supply modes of operation depending on the user need.

When PVDDL is external (PWR_MODE0, PWR_MODE1), if PVDDH falls below (PVDDL + 2.3V) level, the PSM will stop switching between supplies and will remain on the PVDDH supply. In PWR_MODE2 user needs to ensure that PVDDH supply level is at least 2.3V above the PVDDL voltage generated internally in order to take advantage of PSM mode of operation. To enable voltage protection the under voltage threshold of PVDDH

supply should be set above 7.1V by using register bits PVDD_UV_TH [15:11]. This will ensure that, with an internally generated PVDDL of 4.8V, PVDDH supply is at least 2.3V higher than PVDDL.

Table 3 Device Configuration and Power Supply Modes

Supply Power Mode	Output Switching Mode	Supply Condition	PVDDL Mode	Device Configuration	Use Case and Device Functionality
PWR_MODE0	High Power on PVDDH	PVDDH>PVDDL	External	CDS_MODE[1:0]=10	PVDDH is the only supply used to deliver output power.
PWR_MODE1	PSM - High Power on PVDDL	PVDDH>PVDDL	External	CDS_MODE[1:0]=00	PVDDL is used to deliver output power based on level and headroom configured. When audio signal crosses a programmed threshold Class-D output is switched over PVDDH.
PWR_MODE2	PSM - Low Power on PVDDL	PVDDH>PVDDL	Internal	CDS_MODE[1:0]=11 LDO5V_EN=1 LDO_5V_PVDDL=1	PVDDH is the only supply. PVDDL is delivered by an internal LDO and used to supply at signals close to idle channel levels. When audio signal levels crosses -100dBFS (default), Class-D output switches to PVDDH.
PWR_MODE3	PVDDL	PVDDL	External	CDS_MODE[1:0]=01	The device can be forced to work out of a low power rail mode of operation. For example this can be used for a low power ultrasonic chirp when audio is not played.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~4.7kΩ and the typical value is 2.2kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I2C device address (7-bit) can be set using the ADDR pin according to the following table: The ADDR pin configures the three LSB bits of the following 7-bit binary address A6-A0 of 111xxx0. The permitted I2C addresses are 0x70(7-bit) through 0x7E(7-bit).

Table 4 Address Selection

ADDR	Address(7-bit)
Short to GND	0x70
470Ω to GND	0x72
470Ω to AVDD	0x74
2.2kΩ to GND	0x76
2.2kΩ to AVDD	0x78
10kΩ to GND	0x7A
10kΩ to AVDD	0x7C

Short to AVDD	0x7E

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

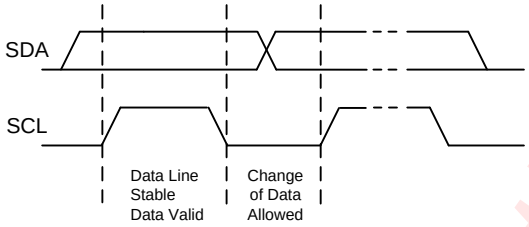


Figure 2 Data Validation Diagram

I²C START/STOP

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

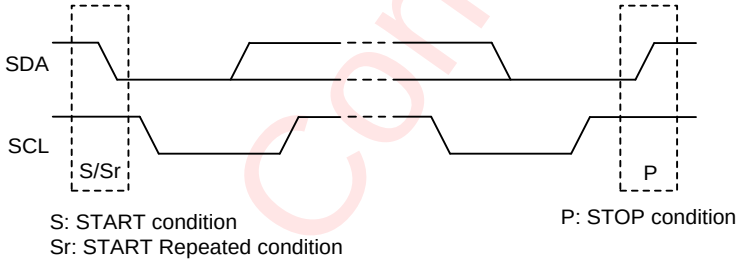


Figure 3 I²C Start/Stop Condition Timing

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

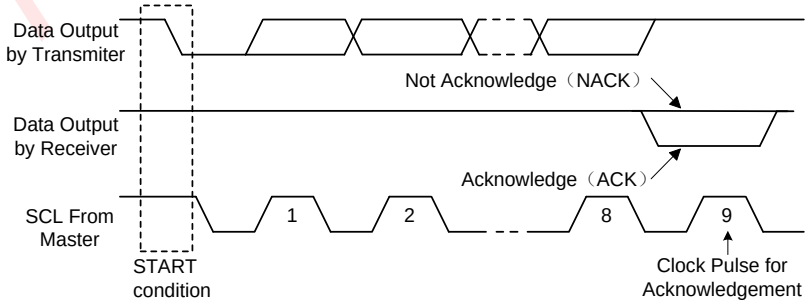


Figure 4 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master sends high data byte of 16-bit data to be written to the addressed register.

g) Slave sends acknowledge signal.

h) Master sends low data byte of 16-bit data to be written to the addressed register.

i) Slave sends acknowledge signal.

j) If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g).

k) Master generates STOP condition to indicate write cycle end.

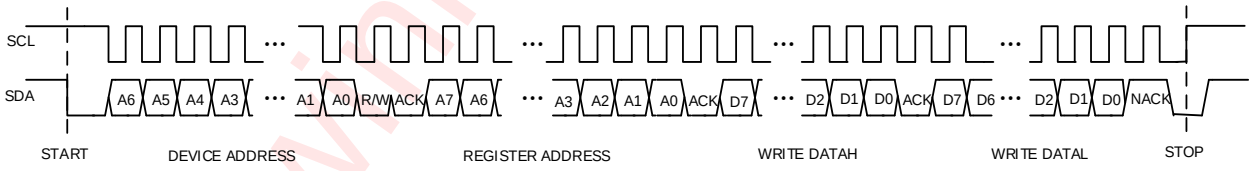


Figure 5 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit).

e) Slave sends acknowledge signal.

f) Master generates STOP condition followed with START condition or REPEAT START condition.

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends read high data byte of 16-bit data from addressed register.

j) Master sends acknowledge signal.

k) Slave sends read low data byte of 16-bit data from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m) If the master device generates STOP condition, the read cycle is ended.

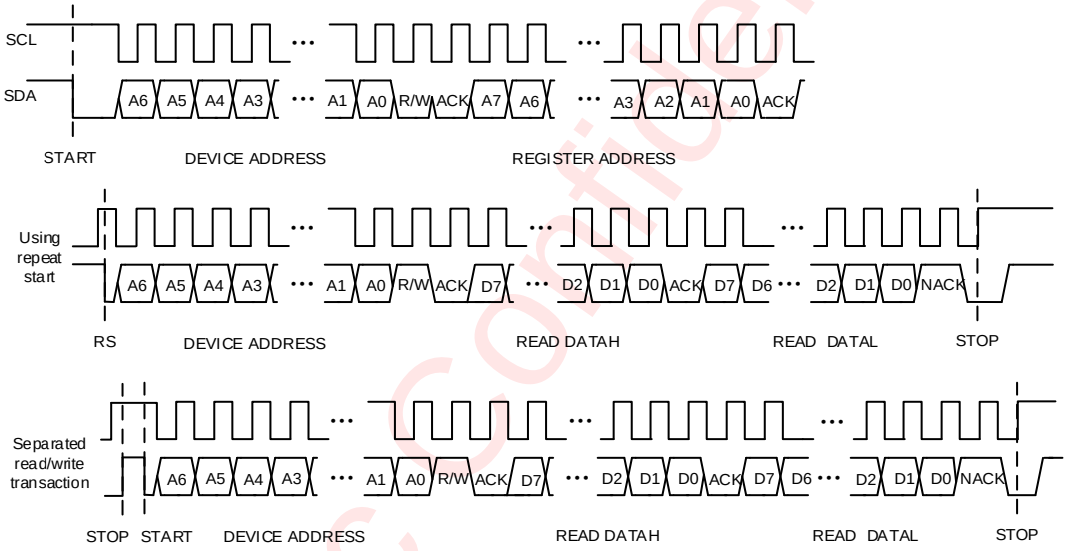


Figure 6 I²C Read Byte Cycle

Register Configuration

Register List

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	ID	RO	IDCODE																0x2321
0x01	SYSST	RO		UVLS			RAMP_ERRS			OVPS			NOCLKS	CLKS	OCDS	DCS	OTHS	PLLS	0x0000
0x02	SYSINT	RC		UVLI			RAMP_ERRI			OVPI			NOCLKI	CLKI	OCDI	DCI	OTHI	PLLI	0x0000
0x03	SYSINTM	RW		UVLM			RAMP_ERRM			OVPM			NOCLKM	CLKM	OCDM	DCM	OTHM	PLLM	0xFFFF
0x04	SYSCTRL	RW	I2C_WEN		I2SEN	SET_GAIN					ULS_HMUTE	HAGCE	HDCCE	HMUTE	IPLL		AMPPD	PWDN	0XA0A4
0x05	SYSCTRL2	RW	GPIO_MUTE	INPLEV		IRQZ_PU	SDZ_VOL_RAMP	VOL_RAMP	VOL										0x0800
0x06	SYSCTRL3	RW								SDZ_DEG_TTH		SDZ_MODE		RMSE	I2SRXEN	I2STXEN	CDS_MODE		0XE60C
0x07	I2SCTRL1	RW	CFSEL				CHSEL		I2SMD		I2SFS		I2S_TXEDGE	I2S_DRV_STREN	I2SSR				0x64C8
0x08	I2SCTRL2	RW	FSYNC_TYPE	SLOT_NUM			I2S_TX_SLOTVLD				I2S_RXR_SLOTVLD				I2S_RXL_SLOTVLD				0x0010

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x09	*I2SCTRL 3*	***RW***	IV2CH	I2SDOSEL	DOHZ	I2SCHS									I2S_RXULS_SLOTVLD				0x2001
0x0A	*I2SCTRL 4*	***RW***	I2SBCK					I2S_SHIFTS					WSINV	BCKINV	TDM_ULS_EN				0xF800
0x0B	*DACCFG 1*	***RW***	RVTH								AVTH								0x2A2D
0x0C	*DACCFG 2*	***RW***	ATTH																0x0964
0x0D	*DACCFG 3*	***RW***	RTTH																0x258F
0x0E	*DACCFG 4*	***RW***									HOLDTH								0x1C64
0x11	*DACCFG 6*	***RW***	FADE_EN	MUTE_SPEED															0x9A3B
0x15	*DACCFG 10*	***RW***								PSM_EN				AMPNG_EN					0x3F30
0x17	*DACCFG 12*	***RW***													PSM_DET				0x50FC
0x18	*DACCFG 13*	***RW***					ULS_VOL												0x0800
0x1A	*SYSCFG1*	***RW***	VOL_CDC_BYP																0x3731
0x1B	*SYSCFG2*	***RW***								PWM_CTRL_OEN							MUTE_IEN	MUTE_PAD_EN	0x6F00

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x1C	I2SCFG1	***RW***								GPIO_MUTE_SEL		SPIN_BYP	SPIN_STEP						0x00C0
0x1E	PTC	***RW***								PWM_SEL									0x6000
0x21	TEMP1	***RO***							TEMP1_DET										0x0032
0x22	PVDDL	***RO***							PVDDL_DET										0xC19C
0x23	PVDDH	***RO***							PVDDH_DET										0x0294
0x24	TEMP2	***RO***							TEMP2_DET										0x0032
0x29	TESTDET	***RO***	PVDDL_UVLO_DET	PVDDH_UVLO_DET	IOVDD_UVLO_DET	AVDD_UVLO_DET	A2D_OVP_PVDDH_MK	A2D_OVP_PVDDL_MK											0x0000
0x2A	IVSCTRL1	***RW***													EN_ISENSE		EN_VSENSE		0x207F
0x53	CDACTRL1	***RW***												GDTX_EDGE					0x3194
0x56	PRTCTRL2	***RW***		OT_TEMP2_TH				OT_TEMP1_TH		TF_TEMP2_TH			TF_TEMP1_TH		OT_EN		TFB_EN		0x2008
0x59	OCCTRL1	***RW***	OC_EN																0xE3C0
0x5B	CBCCTRL	***RW***																EN_CBC	0x2281

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x5F	RAMPGEN1	*RW*																RAMP_EN_SS	0x3000
0x60	RAMPGEN2	*RW*		RAMP_EN_SS_TRI												RAMP_EN_SS_RD			0x2879

Register Detailed Description

ID: (Address 00h)				
Bit	Symbol	R/W	Description	Default
15:0	IDCODE	RO	Chip ID (2321h) will be returned after read. All configuration registers will be reset to default value after 0x55aa is written	0x2321

YSST: (Address 01h)				
Bit	Symbol	R/W	Description	Default
15	Reserved	RO	Not used	0
14	UVLS	RO	VDD under voltage indicator 0: Normal 1: UVLO	0
13	Reserved	RO	Not used	0
12	Reserved	RO	Not used	0
11	RAMP_ERRS	RO	The indicat signal of RAMP_ERR	0
10	Reserved	RO	Not used	0
9	Reserved	RO	Not used	0
8	OVPS	RO	OVP status indicator 0: Normal 1: OVP	0
7	Reserved	RO	Not used	0
6	Reserved	RO	Not used	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0
4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCDS	RO	Over current status in amplifier 0: Normal 1: OC	0
2	DCS	RO	The indicat signal of DC 0: Normal 1: DC	0
1	OTHS	RO	Die Temperature is higher than 150℃ 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)				
Bit	Symbol	R/W	Description	Default
15	Reserved	RC	Not used	0
14	UVLI	RC	Interrupt indicator for Power On and UVLS	0

13	Reserved	RC	Not used	0
12	Reserved	RC	Not used	0
11	RAMP_ERRI	RC	Interrupt indicator for RAMP_ERR	0
10	Reserved	RC	Not used	0
9	Reserved	RC	Not used	0
8	OVPI	RC	Interrupt indicator for OVPS.	0
7	Reserved	RC	Not used	0
6	Reserved	RC	Not used	0
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCDI	RC	Interrupt indicator for OCDS	0
2	DCI	RC	Interrupt indicator for DC	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

SYSINTM: (Address 03h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	1
14	UVLM	RW	Interrupt mask for UVLI.	1
13	Reserved	RW	Not used	1
12	Reserved	RW	Not used	1
11	RAMP_ERRM	RW	Interrupt mask for RAMP_ERR	1
10	Reserved	RW	Not used	1
9	Reserved	RW	Not used	1
8	OVPM	RW	Interrupt mask for OVPI	1
7	Reserved	RW	Not used	1
6	Reserved	RW	Not used	1
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCDM	RW	Interrupt mask for OCDI.	1
2	DCM	RW	Interrupt mask for DC	1
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

SYSCTRL: (Address 04h)

Bit	Symbol	R/W	Description	Default
15:14	I2C_WEN	RW	I2C write enable 10: enable others: disable	10
13	I2SEN	RW	Disable/Enable whole I2S interface module 0: Disable 1: Enable	1
12:8	SET_GAIN	RW	AMP gain control, in unit of dBV 00000: 23 00001: 22.42 00010: 21.87 00011: 21.36 00100: 20.87	0

			00101: 20.41 01000: 19.91 01001: 19.34 01010: 18.77 01011: 18.26 01100: 17.77 01101: 17.31 10000: 16.99 10001: 16.41 10010: 15.85 10011: 15.34 10100: 14.85 10101: 14.39 11000: 13.89 11001: 13.31 11010: 12.77 11011: 12.24 11100: 11.77 11101: 11.31 others: reseved	
7	ULS_HMUTE	RW	ultrasonic datapath mute control 0: Normal 1: Mute	1
6	HAGCE	RW	Disable/Enable Hardware AGC 0: Disable 1: Enable	0
5	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: Disable 1: Enable	1
4	HMUTE	RW	Disable/Enable Hardware mute module 0: Disable 1: Enable	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: WCK	0
2	Reserved	RW	Not used	1
1	AMPPD	RW	Amplifier power down control bit, PowerDown until system configuration finished 0: Working 1: Power Down	0
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	0

SYSCTRL2: (Address 05h)

Bit	Symbol	R/W	Description	Default
15	GPIO_MUTE	RW	GPIO mute by MUTE PIN 0: disable 1: enable	0
14	INPLEV	RW	Input level selection bit, i2s input signal will be attenuated by -6dB at first when this register is set to 1. 0: 0dB 1:-6dB	0

13	Reserved	RW	Not used	0
12	IRQZ_PU	RW	IRQZ pad internal pull up enable (20K) 0: disable 1: enable	0
11	SDZ_VOL_RAMP	RW	volume ramp down when SDZ pin is asserted low 0: disable 1: enable	1
10	VOL_RAMP	RW	VOL ramp enable signal 0: disable 1: enable	0
9:0	VOL	RW	Volume control, from 0 to-96dB, in unit of-0.094dB val * 0.094 dB	0

SYSCTRL3: (Address 06h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	1
14:12	Reserved	RW	Not used	110
11	Reserved	RW	Not used	0
10	Reserved	RW	Not used	1
9	Reserved	RW	Not used	1
8:7	SDZ_DEG_TTH	RW	SDZ timeout set 00: 5.46ms 01: 0.68ms 10: 1.36ms 11: 21.8ms	0
6:5	SDZ_MODE	RW	SDZ_MODE<1:0> 00: Shutdown after SDZ timeout 01: shutdown immediate 10~11: Reserved	0
4	RMSE	RW	Hardware AGC mode selection 0: Peak AGC 1: RMS AGC	0
3	I2SRXEN	RW	Disable/Enable I2S receiver module 0: Disable 1: Enable	1
2	I2STXEN	RW	Disable/Enable I2S transmitter module 0: Disable 1: Enable	1
1:0	CDS_MODE	RW	Class-D switching mode 00: PSM, high power on PVDDL (power mode1) 01: PVDDL Only Supply of Class D (power mode3) 10: PVDDH Only Supply of Class D (power mode0) 11: PSM, low power on PVDDL (power mode2)	0

I2SCTRL1: (Address 07h)

Bit	Symbol	R/W	Description	Default
15:12	CFSEL	RW	I2S legacy path output data selection 0000: HAGC 0110: IV 0111:IVBT Others: Reserved	110

11:10	CHSEL	RW	Left/right channel selection for I2S input 00: Reserved 01: Left 10: Right 11: Mono	1
9:8	I2SMD	RW	I2S interface mode selection 00: Philip Standard 01: MSB justified 10: LSB justified 11: Reserved	0
7:6	I2SFS	RW	I2S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	11
5	I2S_TXEDGE	RW	I2S TX clock edge selection 0: negedge 1: posedge	0
4	I2S_DRV_STREN	RW	I2S pad_dout data out strenth enlarge: 0: disable 1: enable	0
3:0	I2SSR	RW	I2S interface sample rate configuration 0110: 32 kHz 0111: 44 kHz 1000: 48 kHz 1001: 96 kHz 1010: 192kHz Others: Reserved	1000

I2SCTRL2: (Address 08h)

Bit	Symbol	R/W	Description	Default
15	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-bck	0
14:12	SLOT_NUM	RW	I2S TDM mode control. 000: I2S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: TDM16s 111: Reserved	0
11:8	I2S_TX_SLOTVLD	RW	TX slot selection, data will be sent to one of the slots. 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	0
7:4	I2S_RXR_SLOTVLD	RW	RX right channel slot selection 0000: Slot 0 0001: Slot 1	1

			0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	
3:0	I2S_RXL_SLOTVLD	RW	RX left channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	0

I2SCTRL3: (Address 09h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15	IV2CH	RW	I2S TX channel data packing mode control. When I2SBCK is set to 32*fs mode, Current & Voltage data could be transmitted to I2S Left & Right channels by Using Special Mode. 0: Legacy 1: Special	0
14	I2SDOSEL	RW	I2S unused channel data selecion 0: Zeros 1: TXData	0
13	DOHZ	RW	Unused channel Data control, When it is set to 0, all Channels are available. Otherwise Unused channel is set to be HiZ. 0: All 1: HiZ	1
12	I2SCHS	RW	I2S Tx Channel selection 0: Left 1: Right	0
11:4	Reserved	RW	Not used	0
3:0	I2S_RXULS_SLOTVLD	RW	RX ultrasonic channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 ..... 1111: Slot 15	1

I2SCTRL4: (Address 0Ah)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
15:11	I2SBCK	RW	Word length in one slot, = set_num+1 (bits)	11111
10:6	I2S_SHIFTS	RW	The bit width of shift from WCK edge(0~31)	0
5	WSINV	RW	I2S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I2S bit clock invert control 0: Not invert 1: Inverted	0
3:2	TDM_ULS_EN	RW	uls tdm mode 00: Disable 01: Mix in INTP	0

			10: MIX in HSRC 11: Not allowed	
1:0	Reserved	RW	Not used	0

DACCFG1: (Address 0Bh)

Bit	Symbol	R/W	Description	Default
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC) : P0= ((i/256*Gain)**2)/RLoad/2 RMSE = 1 (RMS AGC) : P0=(i/256)*(Gain**2)/RLoad i is the register value, default 0x40 Gain is the Speaker Gain configured by SYSCTRL.SET_GAIN. RLoad is 8ohm	101010
7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC) : P0= ((i/256*Gain)**2)/RLoad/2 RMSE = 1 (RMS AGC) : P0=(i/256)*(Gain**2)/RLoad i is the register value, default 0x40 Gain is the Speaker Gain configured by SYSCTRL.SET_GAIN. RLoad is 8ohm	101101

DACCFG2: (Address 0Ch)

Bit	Symbol	R/W	Description	Default
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8us	964

DACCFG3: (Address 0Dh)

Bit	Symbol	R/W	Description	Default
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	258F

DACCFG4: (Address 0Eh)

Bit	Symbol	R/W	Description	Default
15:9	Reserved	RW	Not used	1110
8	Reserved	RW	Not used	0
7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	1100100

DACCFG6: (Address 11h)

Bit	Symbol	R/W	Description	Default

15	FADE_EN	RW	mute ramp enable signal 0: disable 1: enable	1
14:12	MUTE_SPEED	RW	mute ramp speed control 000: 5.3ms 001: 10.7ms 010: 21.3ms 011: 42.7ms 100: 64ms 101: 85.3ms 110: 128ms 111: 170.7ms	1
11:8	Reserved	RW	Not used	1010
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	0
5:3	Reserved	RW	Not used	111
2	Reserved	RW	Not used	0
1	Reserved	RW	Not used	1
0	Reserved	RW	Not used	1

DACCFG10: (Address 15h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14:12	Reserved	RW	Not used	11
11:9	Reserved	RW	Not used	111
8	PSM_EN	RW	PSM enable signal 0: disable 1: enable	1
7:5	Reserved	RW	Not used	1
4	AMPNG_EN	RW	Power down amplifier when in noise gate mode 0: disable 1: enable	1
3	Reserved	RW	Not used	0
2:0	Reserved	RW	Not used	0

DACCFG12: (Address 17h)

Bit	Symbol	R/W	Description	Default
15:12	Reserved	RW	Not used	101
11:10	Reserved	RW	Not used	0
9:8	Reserved	RW	Not used	0
7	Reserved	RW	Not used	1
6:5	Reserved	RW	Not used	11
4	Reserved	RW	Not used	1
3	PSM_DET	RW	Low Voltage Signaling threshold 0: Fixed 1: Relative to PVDDL voltage	1
2	Reserved	RW	Not used	1
1	Reserved	RW	Not used	0
0	Reserved	RW	Not used	0

DACCFG13: (Address 18h)

Bit	Symbol	R/W	Description	Default
15:14	Reserved	RW	Not used	0
13	Reserved	RW	Not used	0
12:11	Reserved	RW	Not used	1
10:2	ULS_VOL	RW	Ultransonic data volume control, f from 0 to-96dB, in unit of-0.188dB	0
1	Reserved	RW	Not used	0
0	Reserved	RW	Not used	0

SYSCFG1: (Address 1Ah)

Bit	Symbol	R/W	Description	Default
15	VOL_CDC_BYP	RW	Bypass ramp/fade function 0: normal 1: bypass	0
14:12	Reserved	RW	Not used	11
11	Reserved	RW	Not used	0
10	Reserved	RW	Not used	1
9	Reserved	RW	Not used	1
8	Reserved	RW	Not used	1
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	0
5	Reserved	RW	Not used	1
4	Reserved	RW	Not used	1
3:2	Reserved	RW	Not used	00
1	Reserved	RW	Not used	0
0	Reserved	RW	Not used	1

SYSCFG2: (Address 1Bh)

Bit	Symbol	R/W	Description	Default
15:12	Reserved	RW	Not used	110
11:10	Reserved	RW	Not used	11
9	Reserved	RW	Not used	1
8	PWM_CTRL_OEN	RW	PAD_PWM output enable: 0: enable output 1: disable output	1
7:3	Reserved	RW	Not used	0
2	Reserved	RW	Not used	0
1	MUTE_IEN	RW	MUTE PAD input enable when MUTE_PAD_EN high 0: disable 1: enable	0
0	MUTE_PAD_EN	RW	MUTE PAD enable 0: disable MUTE PAD 1: enable MUTE PAD	0

I2SCFG1: (Address 1Ch)

Bit	Symbol	R/W	Description	Default
15:13	Reserved	RW	Not used	0
12	Reserved	RW	Not used	0
11	Reserved	RW	Not used	0
10	Reserved	RW	Not used	0
9	Reserved	RW	Not used	0

8	GPIO_MUTE_SEL	RW	GPIO mute active mode sel 0: low active 1: high active	0
7	Reserved	RW	Not used	1
6	SPIN_BYP	RW	IIS Spin Bypass 0: Spin Data 1: Normal Data	1
5:4	SPIN_STEP	RW	IIS Spin Step 00: 8192@64fs(170ms) 01: 4096@64fs(85ms) 10: 2048@64fs(42ms) 11: 1024@64fs(21ms)	0
3	Reserved	RW	Not used	0
2	Reserved	RW	Not used	0
1:0	Reserved	RW	Not used	0

PTC: (Address 1Eh)

Bit	Symbol	R/W	Description	Default
15:14	Reserved	RW	Not used	1
13:12	Reserved	RW	Not used	10
11:9	Reserved	RW	Not used	0
8:7	PWM_SEL	RW	PTC pwm frequency 00: 192k-16step 01: 384k-8step 10: 192k-32step 11: 384k-16step	0
6:1	Reserved	RW	Not used	0
0	Reserved	RW	Not used	0

TEMP1: (Address 21h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	TEMP1_DET	RO	Reference temperature(2's complement) for environment Please convert it to decimal number, resolution 0.5°C	110010

PVDDL: (Address 22h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RO	Not used	1
14	Reserved	RO	Not used	1
13:10	Reserved	RO	Not used	0
9:0	PVDDL_DET	RO	Voltage of PVDDH, resolution: 12.4/1023 V	110011100

PVDDH: (Address 23h)

Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	PVDDH_DET	RO	Voltage of PVDDL, resolution: 12.4*2.25/1023 V	1010010100

TEMP2: (Address 24h)

Bit	Symbol	R/W	Description	Default
15	Reserved	RO	Not used	0

14	Reserved	RO	Not used	0
13:10	Reserved	RO	Not used	0
9:0	TEMP2_DET	RO	Reference temperature(2's complement) for vsense calibration Please convert it to decimal number val*0.5	110010

TESTDET: (Address 29h)

Bit	Symbol	R/W	Description	Default
15	PVDDL_UVLO_DET	RO	AVDD UVLO signal 0: normal 1: AVDD UVLO	0
14	PVDDH_UVLO_DET	RO	AVDD UVLO signal 0: normal 1: AVDD UVLO	0
13	IOVDD_UVLO_DET	RO	IOVDD UVLO signal 0: normal 1: IOVDD UVLO	0
12	AVDD_UVLO_DET	RO	AVDD UVLO signal 0: normal 1: AVDD UVLO	0
11	A2D_OVP_PVDDH_MK	RO	PVDDH OVP flag 0: normal 1: ovp	0
10	A2D_OVP_PVDDL_MK	RO	PVDDL OVP flag 0: normal 1: ovp	0
9:0	Reserved	RO	Not used	0

IVSCTRL1: (Address 2Ah)

Bit	Symbol	R/W	Description	Default
15:14	Reserved	RW	Not used	0
13	Reserved	RW	Not used	1
12	Reserved	RW	Not used	0
11	Reserved	RW	Not used	0
10	Reserved	RW	Not used	0
9:8	Reserved	RW	Not used	0
7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	1
5	Reserved	RW	Not used	1
4	Reserved	RW	Not used	1
3	EN_ISENSE	RW	Disable/Enable Isense SD ADC 0: Disable 1: Enable	1
2	Reserved	RW	Not used	1
1	EN_VSENSE	RW	Disable/Enable Vsense SD ADC 0: Disable 1: Enable	1
0	Reserved	RW	Not used	1

CDACTRL1: (Address 53h)				
Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14	Reserved	RW	Not used	0
13	Reserved	RW	Not used	1
12	Reserved	RW	Not used	1
11:10	Reserved	RW	Not used	0
9	Reserved	RW	Not used	0
8	Reserved	RW	Not used	1
7	Reserved	RW	Not used	1
6	Reserved	RW	Not used	0
5	Reserved	RW	Not used	0
4:3	GDTX_EDGE	RW	Adjust GATEDRIVER edge time 00: slow pull down 01: 6ns 10: 10ns 11: 16ns	10
2:0	Reserved	RW	Not used	100

PRTCTRL2: (Address 56h)				
Bit	Bit	Bit	Bit	Bit
15:14	Reserved	RW	Not used	0
13:11	OT_TEMP2_TH	RW	OT temp2 threshold 000: 90°C 001: 100°C 010: 110°C 011: 120°C 100: 130°C 101: 140°C 110: 150°C 111: 160°C	110
10:9	OT_TEMP1_TH	RW	OT temp1 threshold 00: 130°C 01: 140°C 10: 150°C 11: 160°C	10
8:6	TF_TEMP2_TH	RW	TFB temp2 threshold 000: 95°C 001: 100°C 010: 105°C 011: 110°C 100: 115°C 101: 120°C 110: 125°C 111: 130°C	0
5:4	TF_TEMP1_TH	RW	TFB temp1 threshold 00: 100°C 01: 110°C 10: 120°C 11: 130°C	0
3:2	OT_EN	RW	OT enable for temp1 & temp2 00: disable 01: TEMP1 OT enable	10

			10: TEMP2 OT enable 11:TEMP1 & TEMP2 OT both enable	
1:0	TFB_EN	RW	TFB enable signal 00: disable 01: enable Others: reserved	0

OCCTRL1: (Address 59h)

Bit	Symbol	R/W	Description	Default
15	OC_EN	RW	OC enable signal 0: disable 1: enable	1
14	Reserved	RW	Not used	1
13	Reserved	RW	Not used	1
12	Reserved	RW	Not used	0
11	Reserved	RW	Not used	0
10:9	Reserved	RW	Not used	1
8	Reserved	RW	Not used	1
7:6	Reserved	RW	Not used	11
5	Reserved	RW	Not used	0
4:0	Reserved	RW	Not used	0

CBCCTRL: (Address 5Bh)

Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14	Reserved	RW	Not used	0
13:11	Reserved	RW	Not used	100
10	Reserved	RW	Not used	0
9	Reserved	RW	Not used	1
8	Reserved	RW	Not used	0
7	Reserved	RW	Not used	1
6:5	Reserved	RW	Not used	0
4:2	Reserved	RW	Not used	0
1	Reserved	RW	Not used	0
0	EN_CBC	RW	CBC enable signal 0: disable 1: enable	1

RAMPGEN1: (Address 5Fh)

Bit	Symbol	R/W	Description	Default
15:13	Reserved	RW	Not used	1
12:5	Reserved	RW	Not used	10000000
4:3	Reserved	RW	Not used	0
2	Reserved	RW	Not used	0
1	Reserved	RW	Not used	0
0	RAMP_EN_SS	RW	Spread spectrum enable signal. 0: Spread spectrum off 1: Spread spectrum is on	0

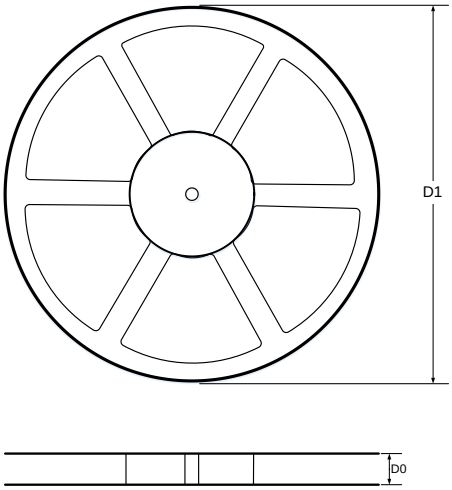
RAMPGEN2: (Address 60h)

Bit	Symbol	R/W	Description	Default

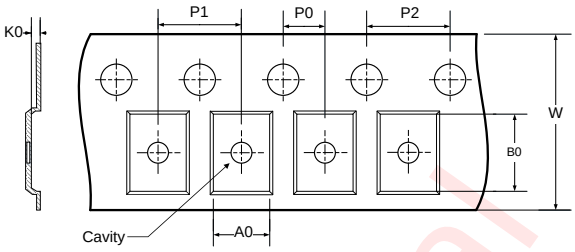
15	Reserved	RW	Not used	0
14	RAMP_EN_SS_TRI	RW	Triangle spread spectrum enable signal 0: Triangle spread spectrum off 1: Triangle spread spectrum is on	0
13:11	Reserved	RW	Not used	101
10:7	Reserved	RW	Not used	0
6	Reserved	RW	Not used	1
5	Reserved	RW	Not used	1
4	Reserved	RW	Not used	1
3	Reserved	RW	Not used	1
2	RAMP_EN_SS_RDM	RW	Random spread spectrum enable signal. 0: random spread spectrum off 1: The random spread spectrum is turned on	0
1:0	Reserved	RW	Not used	1

Tape and Reel Information

REEL DIMENSIONS

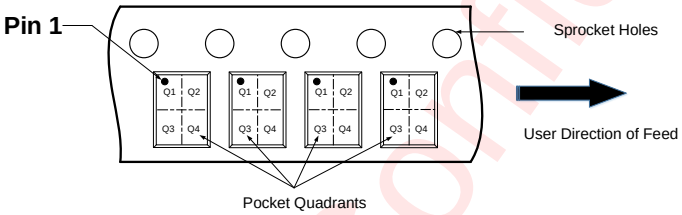


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



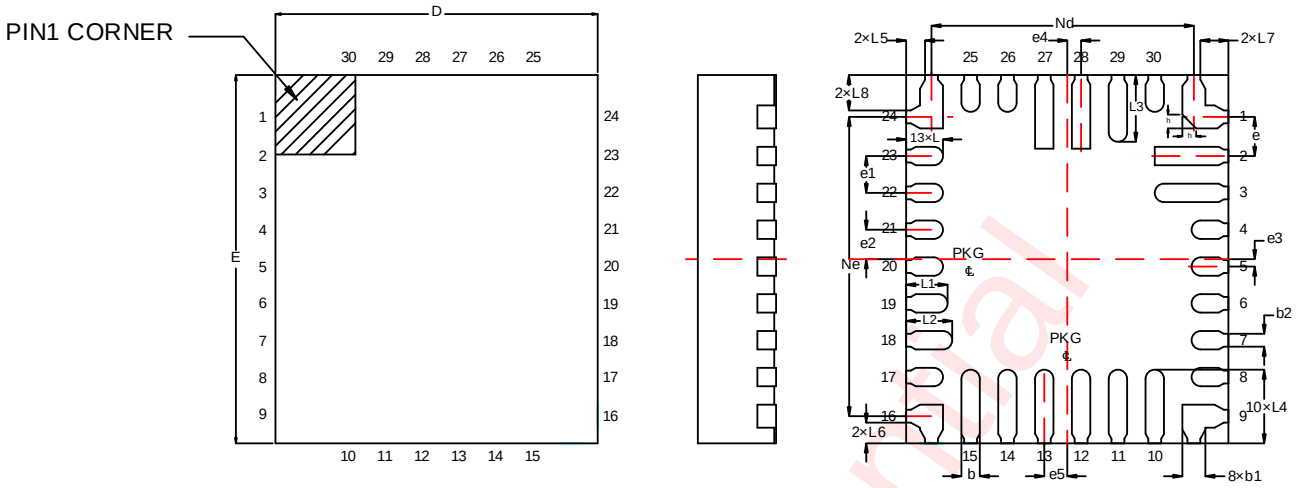
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.75	4.25	1.1	2	8	4	12	Q1

All dimensions are nominal

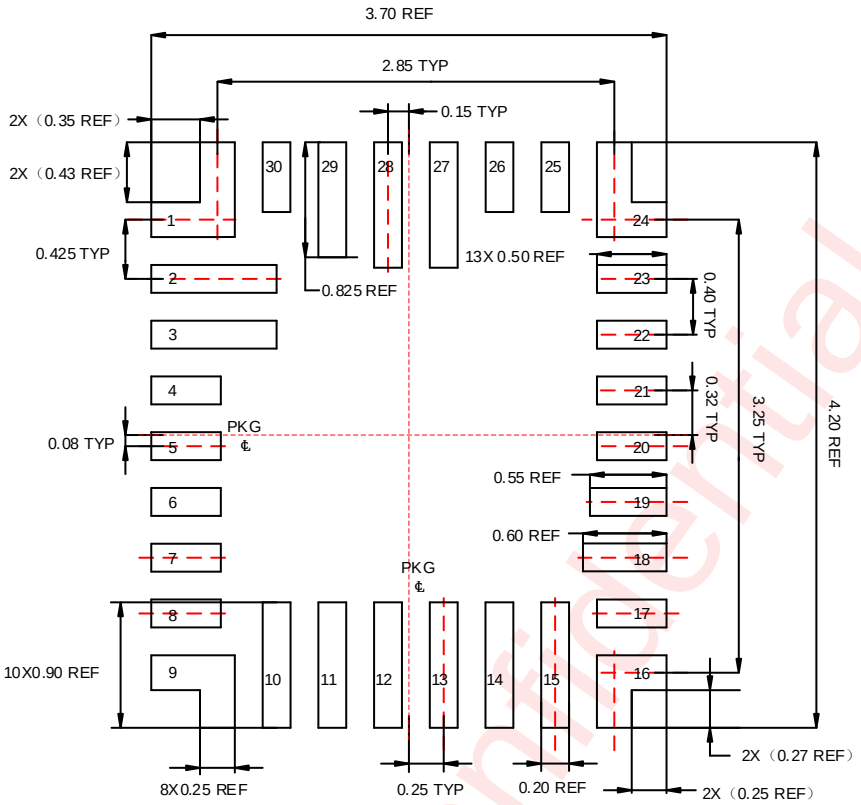
Package Description

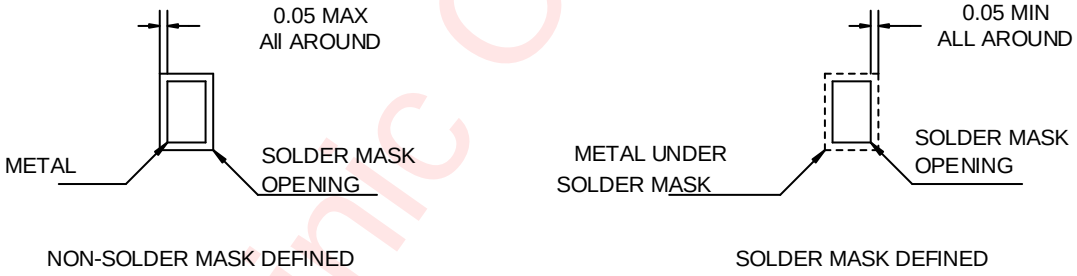


SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.20	0.25	0.30
b2	0.140REF		
c	0.203REF		
D	3.40	3.50	3.60
E	3.90	4.00	4.10
e	0.425BSC		
e1	0.40BSC		
e2	0.32BSC		
e3	0.08BSC		
e4	0.15BSC		
e5	0.25BSC		
Nd	2.85BSC		
Ne	3.25BSC		
L	0.30	0.40	0.50
L1	0.35	0.45	0.55
L2	0.40	0.50	0.60
L3	0.625	0.725	0.825
L4	0.70	0.80	0.90
L5	0.205REF		
L6	0.225REF		
L7	0.305REF		
L8	0.385REF		
h	0.15REF		

Land Pattern Data





Unit: mm

Revision History

Version	Date	Changed Record
V1.0	Oct 2025	Officially Released

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