Triple Schmitt-Trigger Inverter

Features

- Wide Supply Voltage Range: 1.65V to 5.5V
- Low Static Power Consumption (I_{CC}= 0.1μA)
- Low Input Capacitance (C_i= 4pF)
- I_{OFF} Supports Partial Power-Down-Mode Operation
- t_{pd}= 5.3ns at 3.3 V
- ±12mA Output Drive at 3.3 V
- 5.5-V I/O Tolerant to Support Mixed-Mode Signal Operations
- Suitable for Point-to-Point Applications
- WBTSSOP 3mmx3mm-8L package

General Description

AWS74LVC3G14 is a triple Schmitt-trigger inverter. The device accepts any supply voltage from 1.65V to 5.5V. AWS74LVC3G14 has three independent inverters, which have a Schmitt trigger architecture that can give them a wider input level and stronger anti-interference ability.

The AWS74LVC3G14 is fully specified for partial power-down applications using off output current (I_{OFF}).The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

Applications

Personal computer
Telecommunications equipment
Networking servers
Route, clock buffer, and mux

Typical Application Circuit

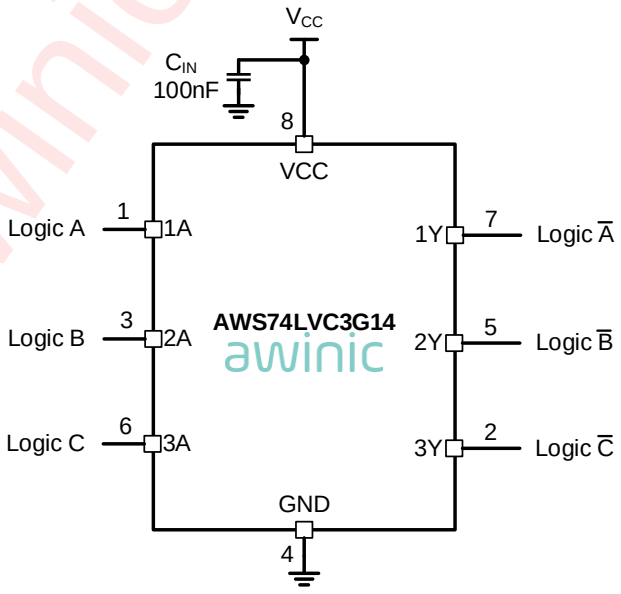
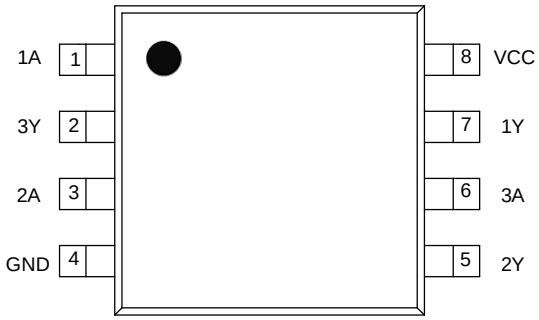


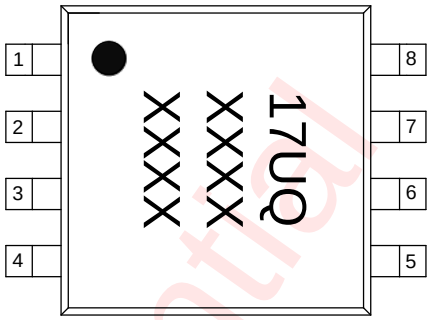
Figure 1 Schmitt-Trigger Inverter Function Application

Pin Configuration And Top Mark

AWS74LVC3G14SPR
(Top View)



AWS74LVC3G14SPR Marking
(Top View)



17UQ - AWS74LVC3G14SPR
XXXX/XXXX - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	1A	Data input 1
2	3Y	Data output 3
3	2A	Data input 2
4	GND	Ground
5	2Y	Data output 2
6	3A	Data input 3
7	1Y	Data output 1
8	VCC	Power supply

Pin Functions

Input nA	Output nY
L	H
H	L

Functional Block Diagram

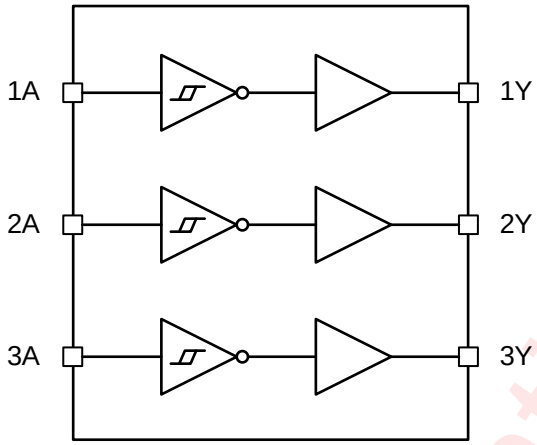


Figure 3 Functional Block Diagram

Typical Application Circuits

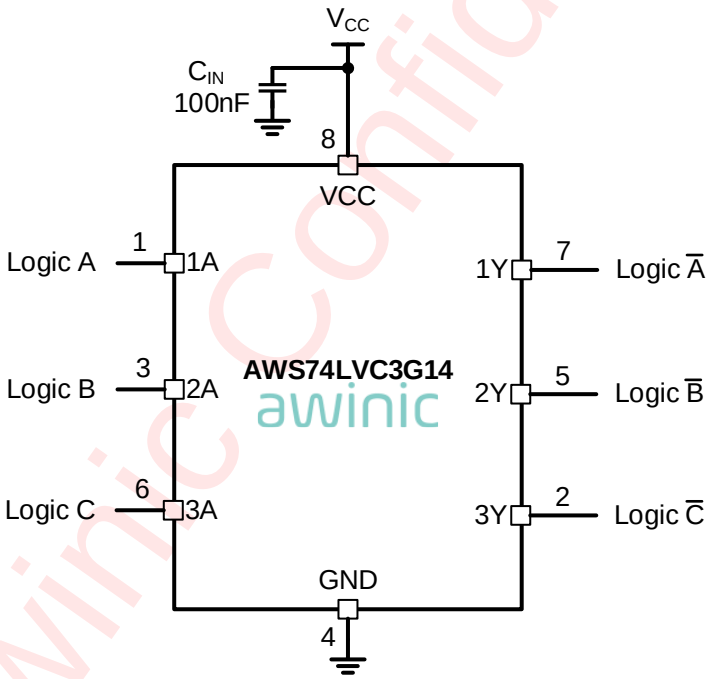


Figure 4 AWS74LVC3G14 Application Circuit

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS74LVC3G14SPR	-40℃～125℃	WBTSSOP 3mmx3mm -8L	17UQ	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.3V to 6.5V
Input voltage range		-0.3V to 6.5V
Output voltage range		-0.3V to 6.5V
Input clamp current, I_{Ik}	V_I <0	±50mA
Output clamp current, I_{OK}	V_O <0	±50mA
Output current, I_O		50mA
Supply current, I_{CC}		100mA
Ground current, I_{GND}		-100mA
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM (All pins, per ESDA/JEDEC JS-001-2017) (NOTE 2)		±2kV
CDM (All pins, per ESDA/JEDEC JS -002-2018)		±1.5kV
Latch-Up		
Test condition: JESD78E		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		1.65	5.5	V
V_I	Input voltage(NOTE1)		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	VCC=1.65V		-4	mA
		VCC=2.3V		-6	mA
		VCC=3V		-12	mA
		VCC=4.5V		-18	mA
I_{OL}	Low-level output current	VCC=1.65V		4	mA
		VCC=2.3V		6	mA
		VCC=3V		12	mA
		VCC=4.5V		18	mA
T_A	Operating free-air temperature T_A		-40	125	°C

NOTE1: All unused data inputs of the device must be held at VCC or GND to ensure proper device operation.

Electrical Characteristics

VCC=3.3V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
I_{CC}	VCC supply current	V_I=0V or 3.6V, I_O=0A; V_{CC}=1.65V to 5.5V; T_A=25°C		0.1	0.5	μA
		V_I=0V or 3.6V, I_O=0A; V_{CC}=1.65V to 5.5V; T_A=-40~125°C			10	μA
ΔI_{CC}	Additional supply current	One input at VCC–0.3V, other inputs at V_{CC} or GND; I_O=0A; V_{CC}=3V to 5.5V; T_A=25°C		0.5	2	μA
		One input at VCC–0.3V, other inputs at V_{CC} or GND; I_O=0A; V_{CC}=3V to 5.5V; T_A=-40~125°C			20	μA
I_I	Input leakage current	V_I=0V or 5.5V; V_{CC}=1.65V to 5.5V; T_A=25°C		0.05	1	μA
		V_I=0V or 5.5V; V_{CC}=1.65V to 5.5V; T_A=-40~125°C			1	μA
I_{OFF}	Power off leakage current	V_I or V_O=5.5V; V_{CC}=0V; T_A=25°C		0.02	0.5	μA
		V_I or V_O=5.5V; V_{CC}=0V; T_A=-40~125°C			2	μA
V_{IH}	High-level input voltage	V_{CC}=1.65V to 1.95V	0.65V_{CC}			V
		V_{CC}=2.3V to 2.7V	1.6			V
		V_{CC}=3V to 3.6V	2			V
		V_{CC}=4.5V to 5.5V	0.7V_{CC}			V
V_{IL}	Low-level input voltage	V_{CC}=1.65V to 1.95V			0.35V_{CC}	V
		V_{CC}=2.3V to 2.7V			0.7	V
		V_{CC}=3V to 3.6V			0.9	V
		V_{CC}=4.5V to 5.5V			0.3V_{CC}	V
V_{OH}	High-level output voltage	I_{OH}=-100μA, V_{CC}=1.65~4.5V	V_{CC}-0.1			V
		I_{OH}=-4mA, V_{CC}=1.65V	1.2			V
		I_{OH}=-6mA, V_{CC}=2.3V	1.9			V
		I_{OH}=-12mA, V_{CC}=3V	2.4			V
		I_{OH}=-18mA, V_{CC}=4.5V	3.8			V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL}=100μA, V_{CC}=1.65~4.5V			0.1	V
		I_{OL}=4mA, V_{CC}=1.65V			0.45	V
		I_{OL}=6mA, V_{CC}=2.3V			0.3	V
		I_{OL}=12mA, V_{CC}=3V			0.75	V
		I_{OL}=18mA, V_{CC}=4.5V			0.75	V
C_I(1)	Input capacitance	V_I=0V or 3.3V, V_{CC}=3.3V		4.0		pF
C_O	Output capacitance	V_O=GND, V_{CC}=0V		4.0		pF
SWITICHING CHARACTERISTICS						
t_{pd}(2)	Propagation delay	V_{CC} = 1.65V to 1.95V		7.5		ns
		V_{CC} = 2.3V to 2.7V		5.7		ns
		V_{CC} = 3.0V to 3.6V		5.3		ns
		V_{CC} = 4.5V to 5.5V		4.6		ns

(1) Typical value set by simulation only.

(2) Typical values are measured at V_{CC}=1.8V, 2.5V, 3.3V and 5V respectively.

Typical Characteristics

TEST INFORMATION

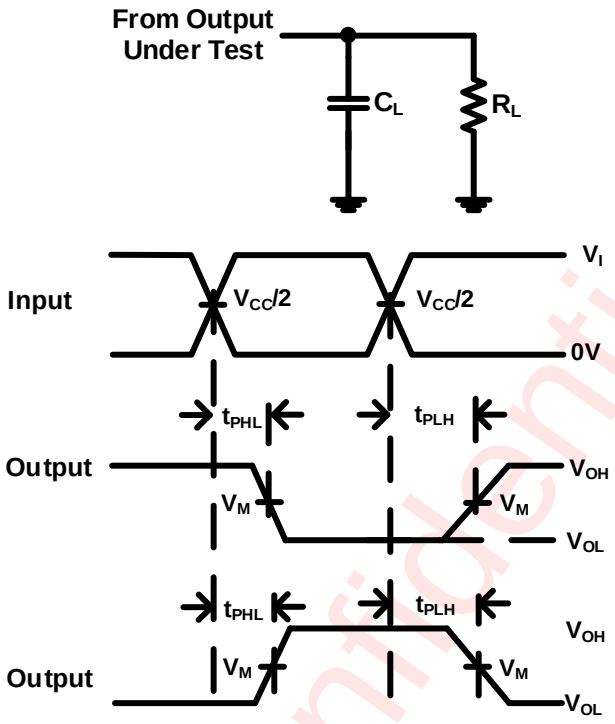


Figure 5 Load Circuit and Propagation Delay Measurement

1. The following table gives the test condition under different supply voltage：

V_{CC}	V_I	t_r/t_f	V_M	C_L	R_L
1.65V to 1.95V	V_{CC}	≤2ns	$V_{CC}/2$	30pF	1kΩ
2.3V to 2.7V	V_{CC}	≤2ns	$V_{CC}/2$	30pF	500Ω
3.0V to 3.6V	3V	≤2.5ns	1.5V	50pF	500Ω
4.5V to 5.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	50pF	500Ω

2. Load capacitance including probe and jig capacitance.

3. t_{PHL} and t_{PLH} is measured at V_M.

4. t_{PHL} and t_{PLH} are same as t_{pd}.

Detailed Functional Description

AWS74LVC3G14 is a triple Schmitt-trigger inverter. The device accepts any supply voltage from 1.65V to 5.5V. AWS74LVC 3G14 has three independent inverters, which have a Schmitt-trigger architecture that can give them a wider input level and stronger anti-interference ability.

The hysteresis characteristics of Schmitt-trigger inverter is shown in Figure 6. When the input level is raised to V_{T+}, the output level flips low, and when the output level drops to V_{T-}, the output level flips high. For each input state, there is a corresponding output state. The Schmitt-trigger inverters have a wide input range and they can effectively overcome input level disturbances.

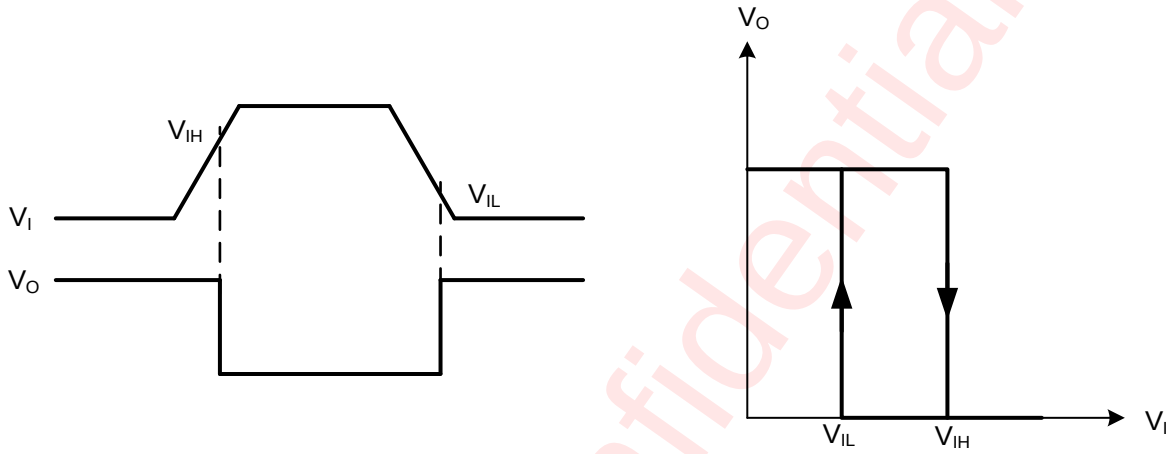


Figure 6 Hysteresis Characteristics of Schmitt-trigger Inverter

The AWS74LVC3G14 is fully specified for partial power-down applications using off output current (I_{OFF}).The outputs for this device enter a high-impedance state when the device is powered down, preventing any damaging backflow current through the device.

PCB Layout Consideration

To obtain the optimal performance of AWS74LVC3G14SPR, PCB layout should be considered carefully. Here are some guidelines:

1. Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCC pin and GND pin. A 0.1 μF capacitor is recommended, but transient performance can be improved by having both 1 μF and 0.1 μF capacitors in parallel as bypass capacitors.
2. Routing and load conditions should be considered to prevent ringing.

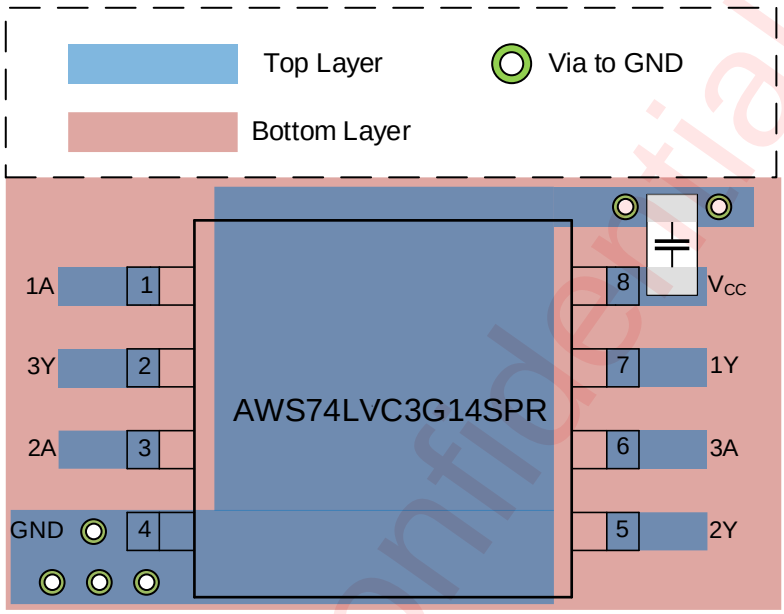
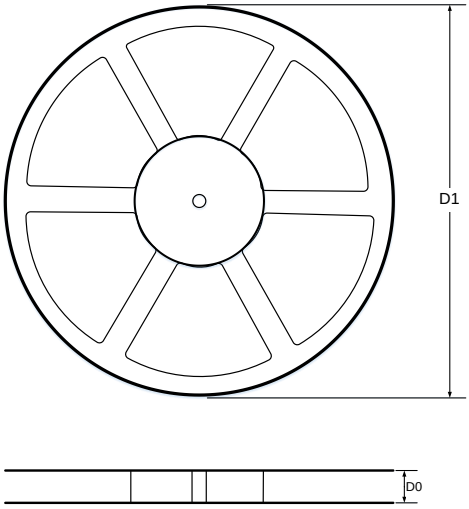


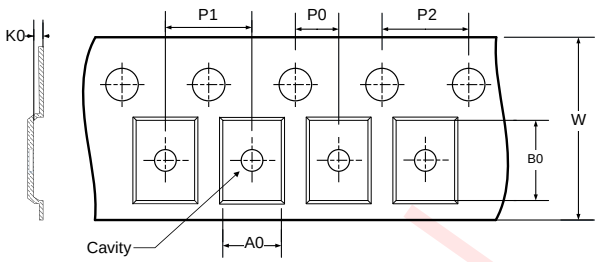
Figure 7 PCB Layout Reference

Tape And Reel Information

REEL DIMENSIONS

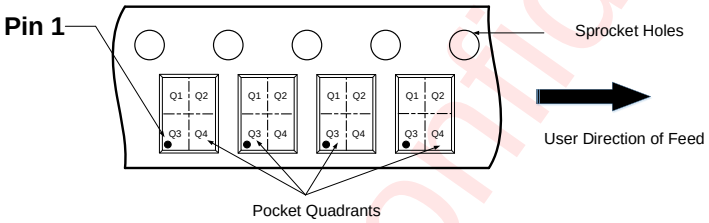


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



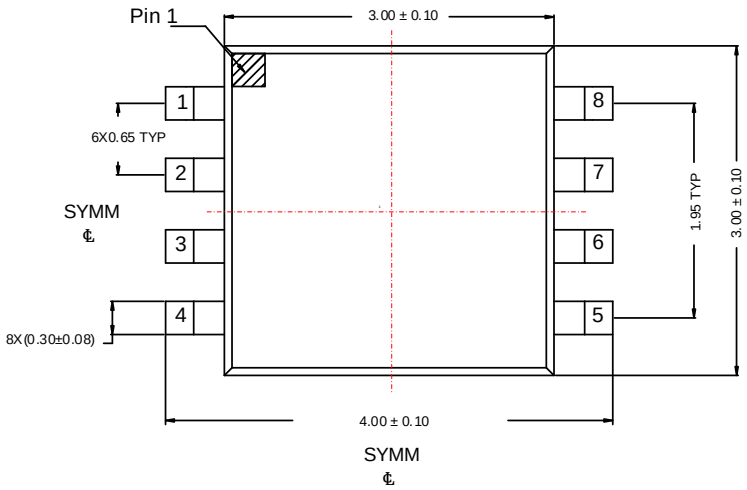
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

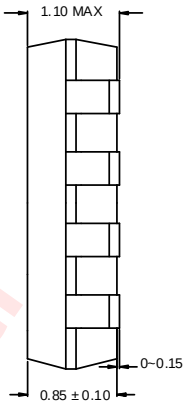
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.35	4.45	1.45	2	4	4	12	Q3

All dimensions are nominal

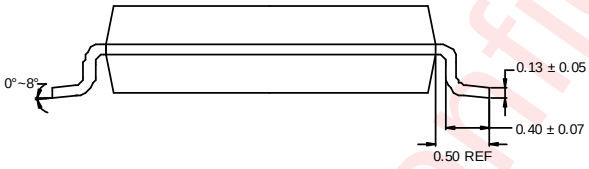
Package Description



Top View



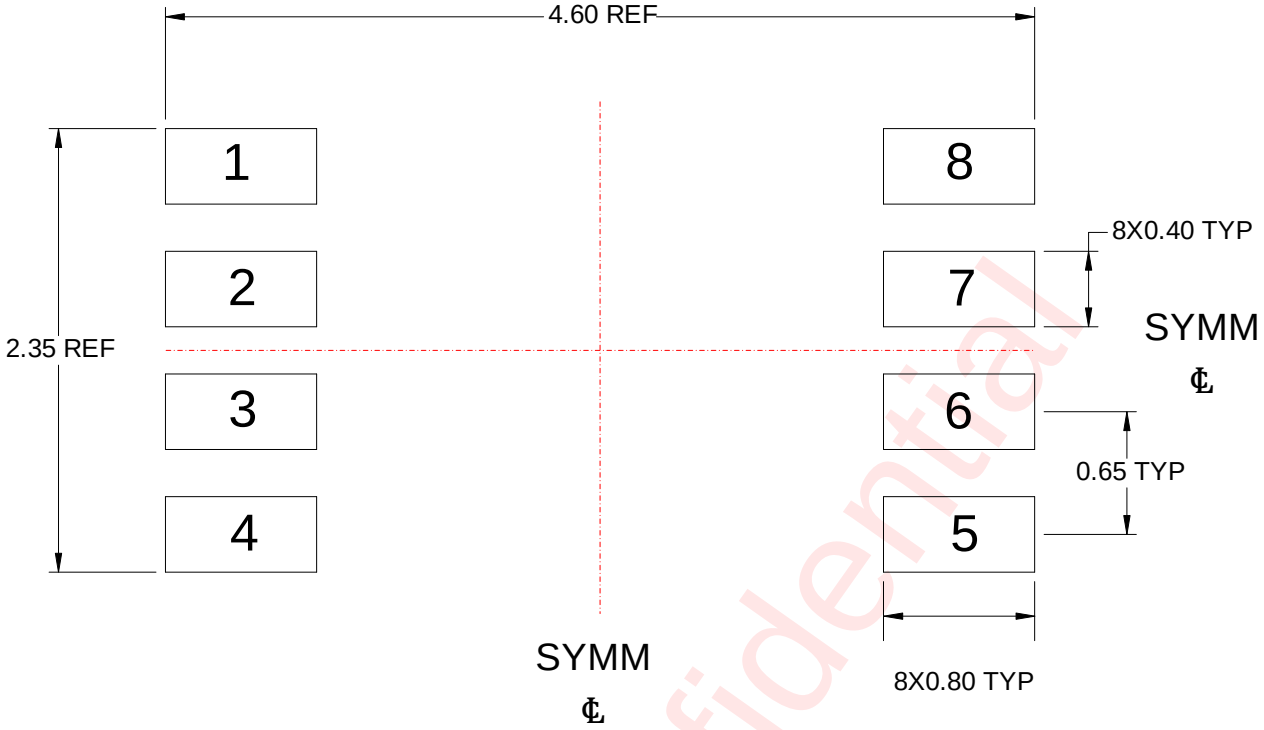
Side View



Side View

Unit:mm

Land Pattern Data



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit:mm

Revision History

Version	Date	Change Record
V1.0	Oct. 2023	Officially released

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

