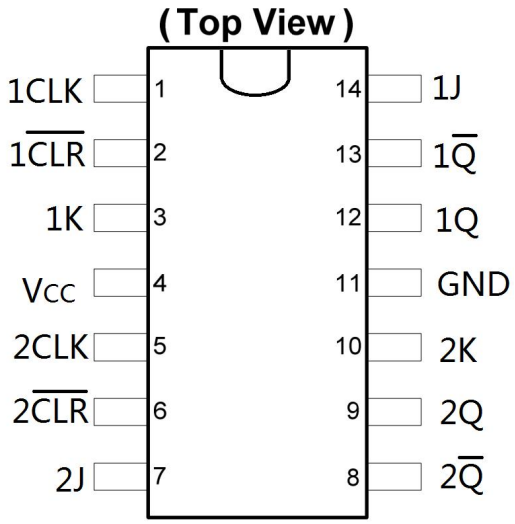
1. DESCRIPTION

The XD74LS73 contains two independent negative-edge-triggered flip-flops.

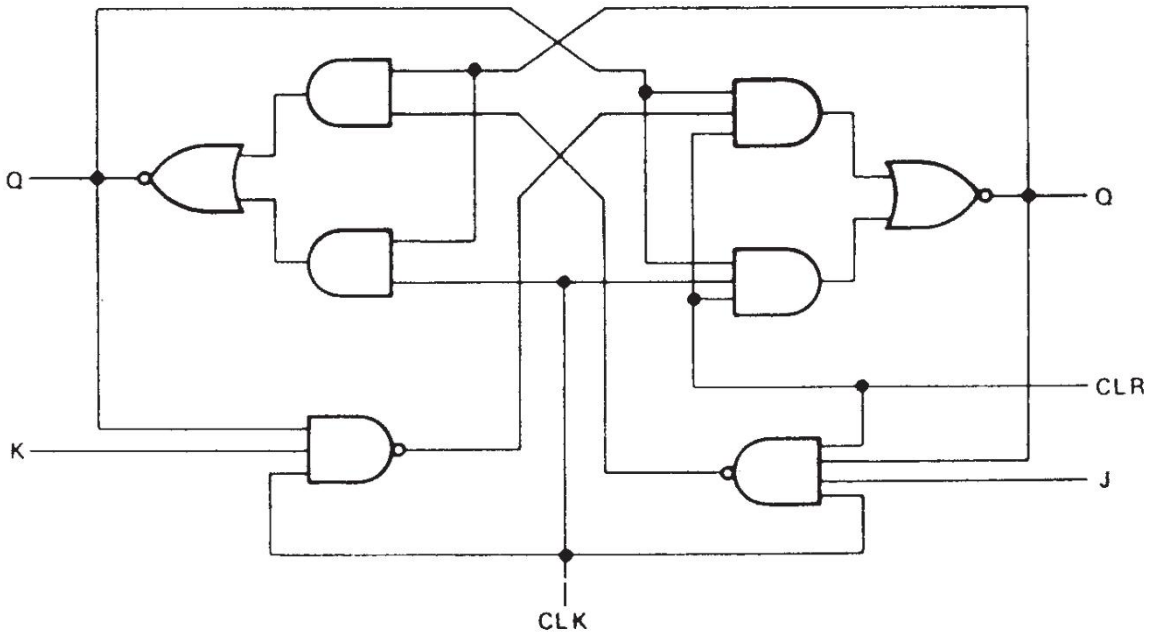
The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the $\overline{\text{clear}}$ is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{\text{Q}}$ output high.

2. PIN CONFIGURATIONS

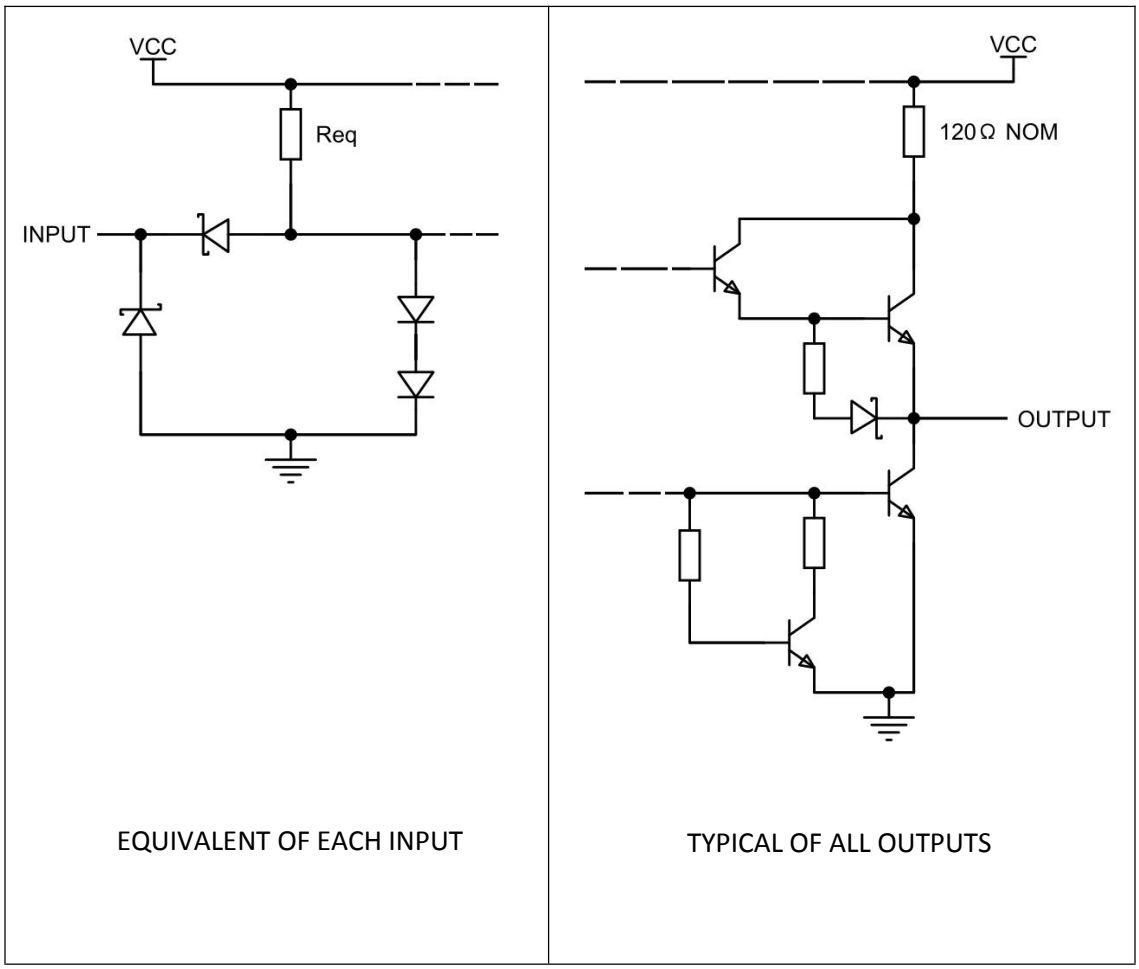


INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q_0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q_0}$

3. LOGIC DIAGRAM



4. SCHEMATICS OF INPUTS AND OUTPUTS



EQUIVALENT OF EACH INPUT

TYPICAL OF ALL OUTPUTS

5. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, V_{CC} (see Note 1)..... 7V

Input voltage, VI: 74LS73..... 7V

Operating free-air temperature range: DIP package..... 0°C to 70°C

Storage temperature range, Tstg..... −65°C to 150°C

NOTES: 1. Voltage values, except inter-emitter voltage, are with respect to the network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

6. RECOMMENDED OPERATING CONDITIONS

			74LS73			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage					V
I_{OH}	High-level output current				0.8	mA
I_{OL}	Low-level output current				−0.4	mA
f_{clock}	Clock frequency		0		8	MHz
t_w	Pulse duration	CLK high	20		30	ns
		$\overline{CLR}$ low	20			
t_{su}	Set up time-before CLK↓	Data high or low	20			ns
		$\overline{CLR}$ inactive	20			
t_h	Hold time-data after CLK↓		0			ns
T_A	Operating free-air temperature		0		70	°C

7. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†	74LS73			UNIT
			MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = 4mA	2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} MAX, I_{OL} = 8mA		0.25	0.4	V
				0.35	0.5	
I_I	J or K	V_{CC} = MAX, V_I = 7 V			0.1	mA
	$\overline{CLR}$				0.3	
	CLK				0.4	
IIH	J or K	V_{CC} = MAX, V_I = 2.7 V			20	μA
	$\overline{CLR}$				60	
	CLK				80	
I_{IL}	J or K	V_{CC} = MAX, V_I = 0.4 V			−0.4	mA
	$\overline{CLR}$ or CLK				−0.8	
I_{OS}§		V_{CC} = MAX	−20		−100	mA
I_{CC} (Totall)		V_{CC} = MAX		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

8. SWITCHING CHARACTERISTICS,VCC = 5 V, TA = 25℃

PARAMETER	FROM(INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L=15 pF,R_L=2kΩ, See Note 3	30	45		MHz
t_{PLH}	$\overline{CLR}$ or CLK	Q or $\overline{Q}$			15	20	ns
t_{PHL}					15	20	ns

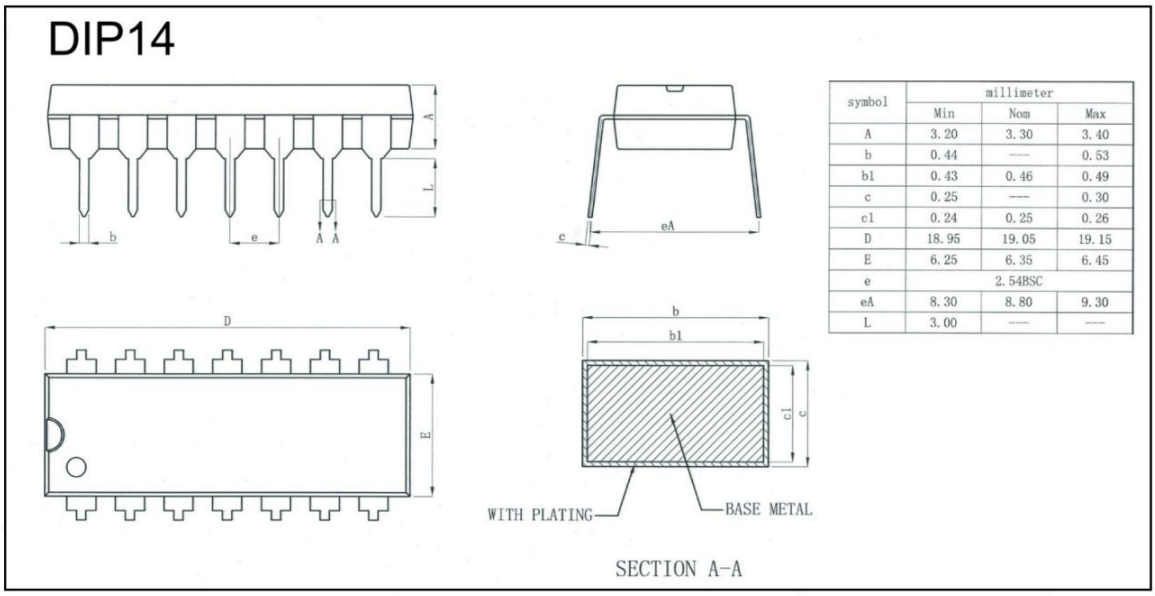
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

9. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD74LS73	XD74LS73	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

10. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	——	0.53
b1	0.43	0.46	0.49
c	0.25	——	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	——	——