

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRFB7434G
▶ Overseas	Part Number	IRFB7434G
▶ Equivalent	Part Number	IRFB7434G

EV is the abbreviation of name EVVO

Description

40V /180A Power MOSFET
Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
Pb-free lead plating; RoHS compliant

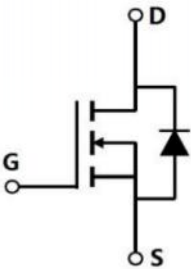
TO-220-3L Pin Configuration



40V N-Channel Enhancement Mode MOSFET

General Features

V_{DS}	40	V
$R_{DS(on),TYP@V_{GS}=10V}$	2.6	mΩ
$R_{DS(on),TYP@V_{GS}=4.5}$	3.5	mΩ
I_D	180	A



Absolute Maximum Ratings ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	40	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾	I_D	180	A
Pulsed drain current ²⁾	$I_{D,pulse}$	390	A
Power dissipation ³⁾	P_D	140	W
Single pulsed avalanche energy ⁴⁾	E_{AS}	200	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^{\circ}\text{C}$
Thermal resistance, junction-case	$R_{\theta JC}$	0.89	$^{\circ}\text{C/W}$
Thermal resistance, junction-ambient ⁵⁾	$R_{\theta JA}$	62	$^{\circ}\text{C/W}$

40V N-Channel Enhancement Mode MOSFET
Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	40			V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(ON)}$		2.6	2.8	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=55\text{ A}$
Drain-source on-state resistance	$R_{DS(ON)}$		3.0	3.5	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$, $I_D=55\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		6587.4		pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=100\text{ kHz}$
Output capacitance	C_{oss}		2537.3		pF	
Reverse transfer capacitance	C_{rss}		178.8		pF	
Turn-on delay time	$t_{d(on)}$		26.6		ns	$V_{GS}=10\text{ V}$, $V_{DS}=20\text{ V}$, $R_G=2\text{ }\Omega$, $I_D=20\text{ A}$
Rise time	t_r		9.3		ns	
Turn-off delay time	$t_{d(off)}$		96		ns	
Fall time	t_f		39.3		ns	
Total gate charge	Q_g		96.8		nC	$I_D=20\text{ A}$, $V_{DS}=20\text{ V}$, $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		14.5		nC	
Gate-drain charge	Q_{gd}		18.4		nC	
Gate plateau voltage	$V_{plateau}$		2.7		V	
Diode forward current	I_S			130	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			390		
Diode forward voltage	V_{SD}			1.3	V	$I_S=20\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		205		ns	$I_S=20\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		557.4		nC	
Peak reverse recovery current	I_{rrm}		4.3		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) $V_{DD}=30\text{ V}$, $R_G=50\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_J=25^{\circ}\text{C}$.
- 5) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25^{\circ}\text{C}$.

40V N-Channel Enhancement Mode MOSFET

Typical Characteristics

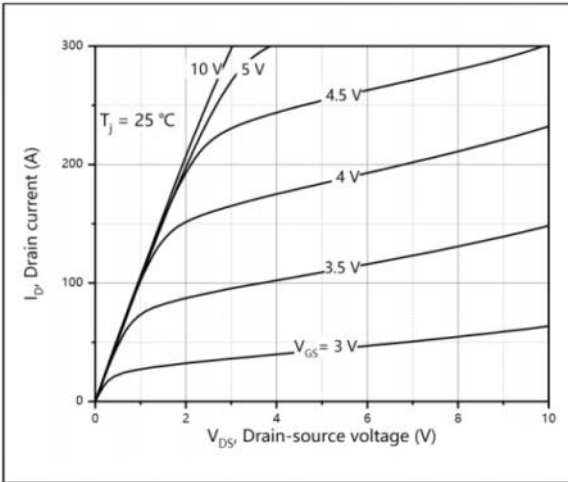


Figure 1, Typ. output characteristics

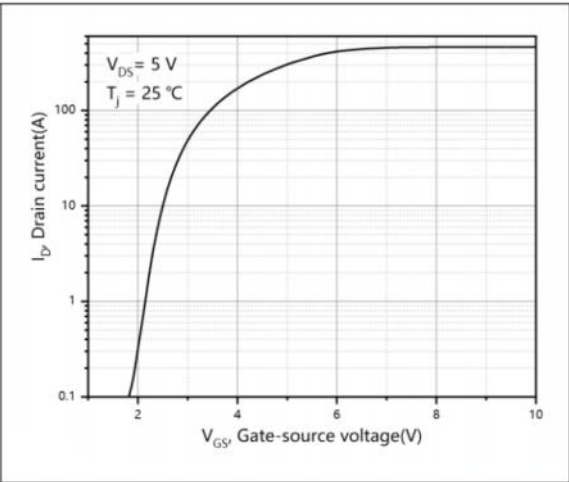


Figure 2, Typ. transfer characteristics

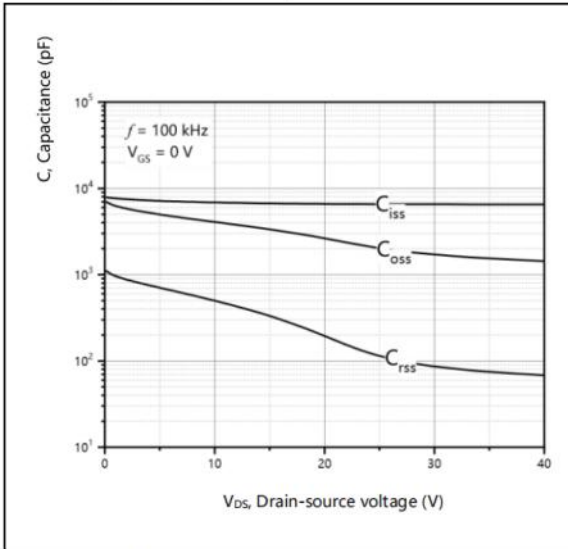


Figure 3, Typ. capacitances

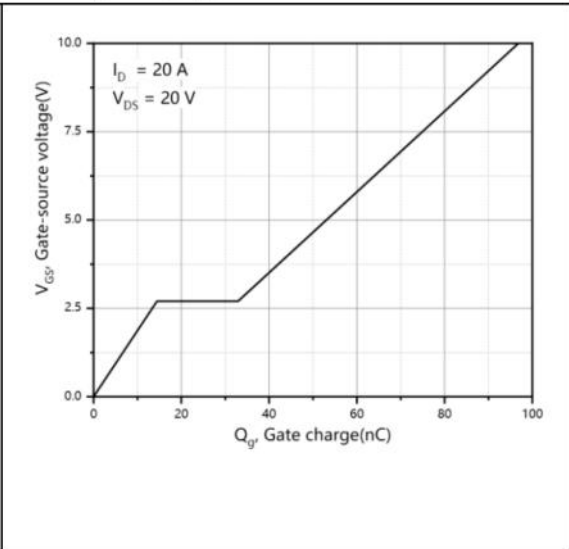


Figure 4, Typ. gate charge

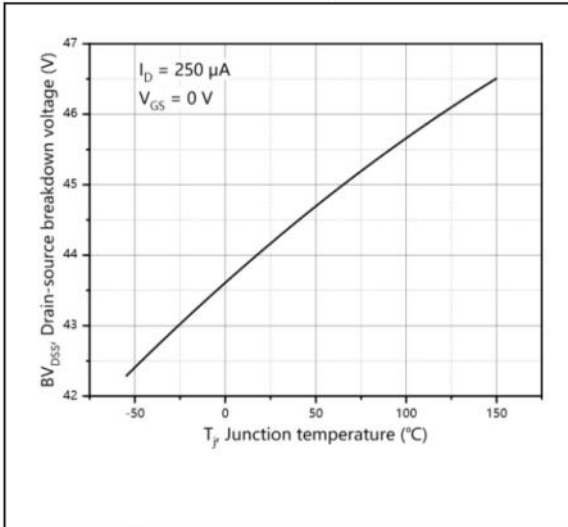


Figure 5, Drain-source breakdown voltage

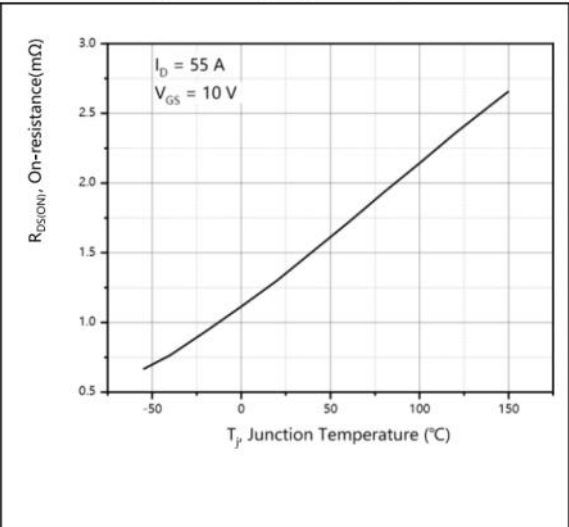


Figure 6, Drain-source on-state resistance

40V N-Channel Enhancement Mode MOSFET

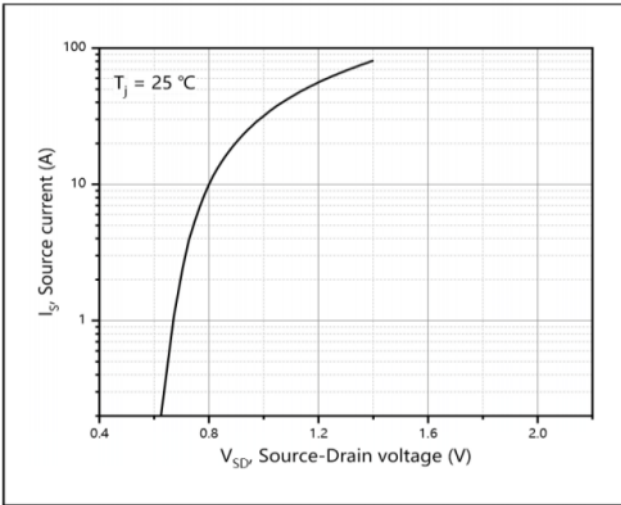


Figure 7, Forward characteristic of body diode

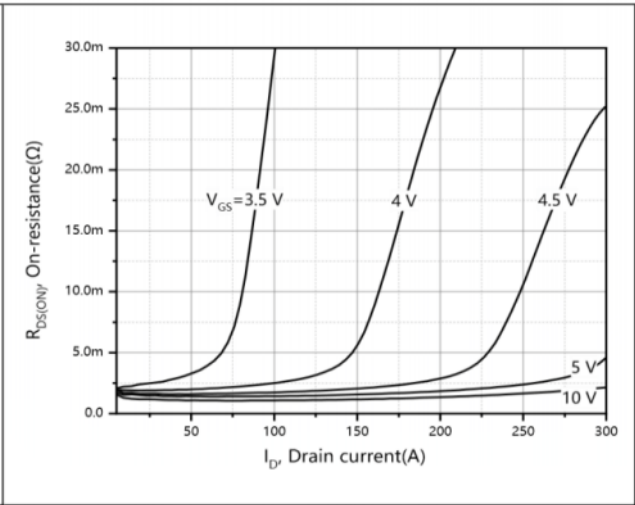


Figure 8, Drain-source on-state resistance

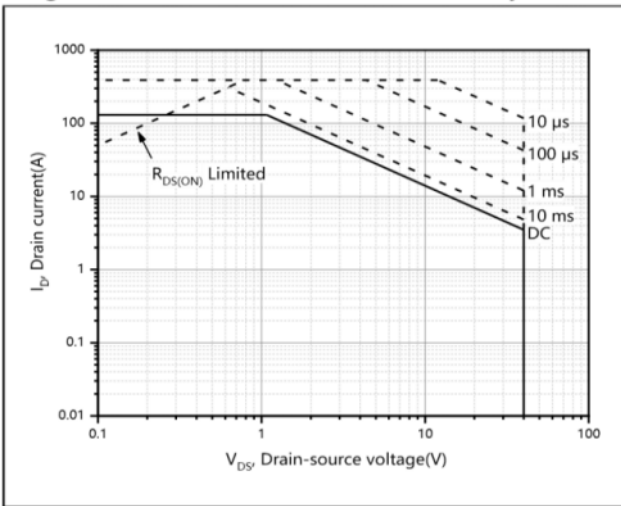


Figure 9, Safe operation area $T_C=25\text{ }^{\circ}\text{C}$

40V N-Channel Enhancement Mode MOSFET

Test circuits and waveforms

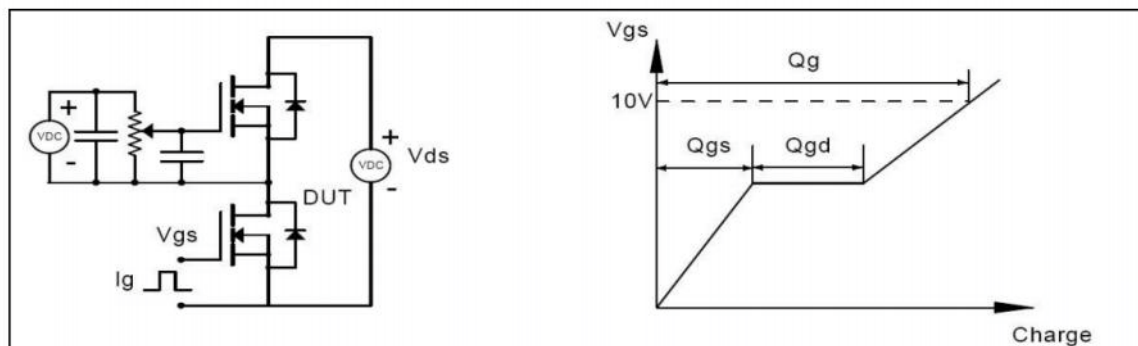


Figure 1. Gate charge test circuit & waveform

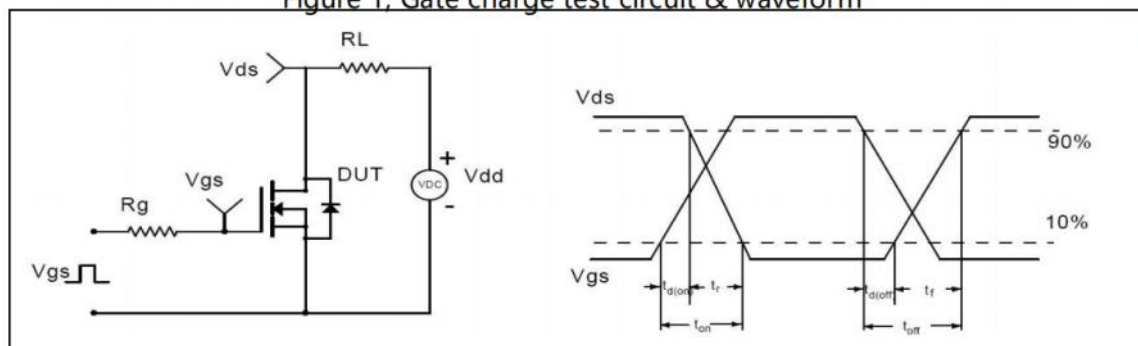


Figure 2. Switching time test circuit & waveforms

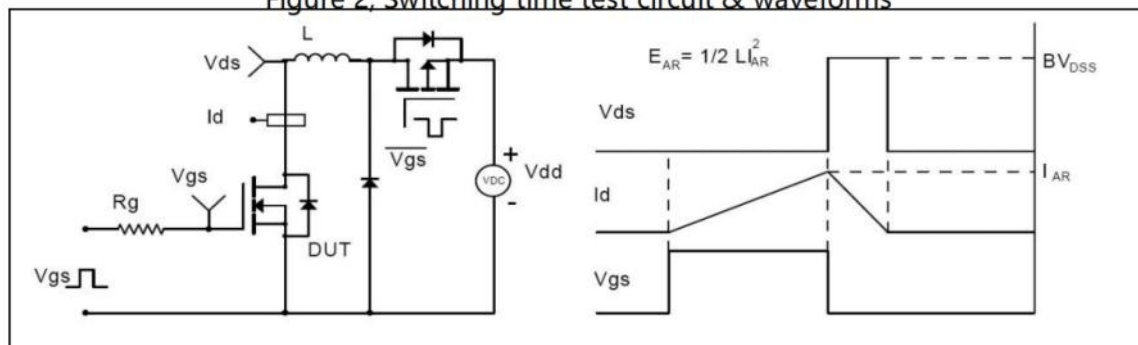


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

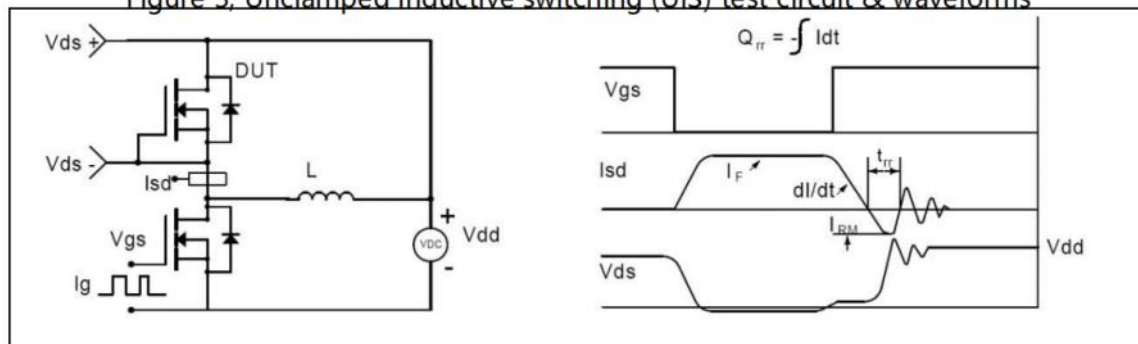
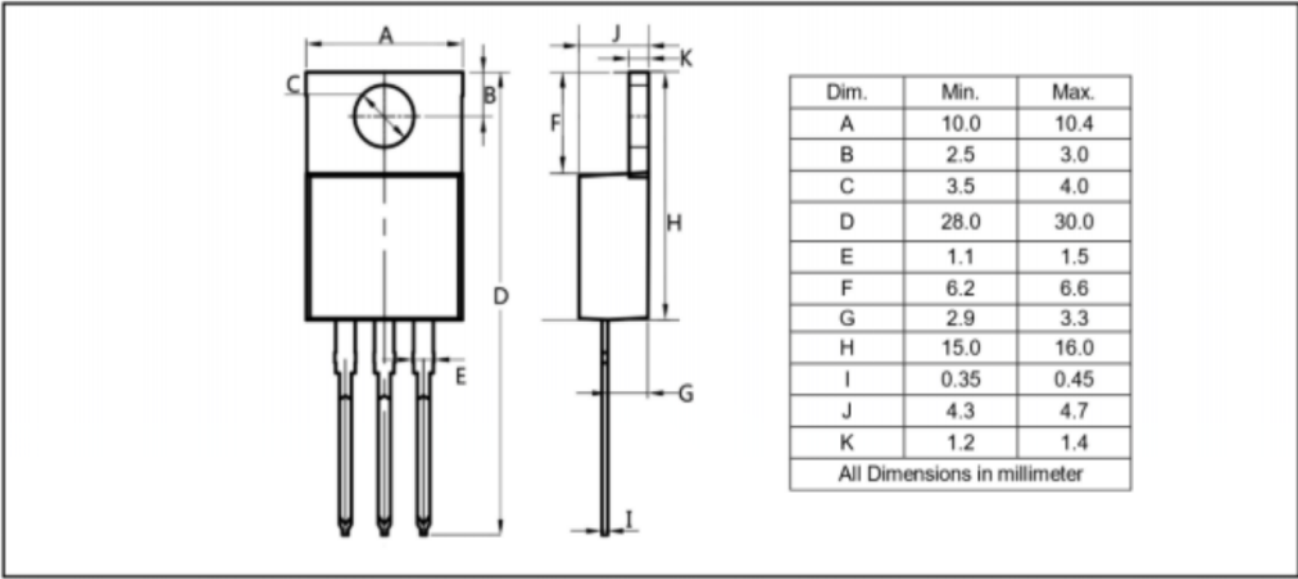


Figure 4. Diode reverse recovery test circuit & waveforms

40V N-Channel Enhancement Mode MOSFET

Package Mechanical Data-TO-220-3L



Disclaimer

EVVOSEMI ("EVVO") reserves the right to make corrections, enhancements, improvements, and other changes to its products and services at any time, and to discontinue any product or service without notice.

EVVO warrants the performance of its hardware products to the specifications applicable at the time of sale in accordance with its standard warranty. Testing and other quality control techniques are used as deemed necessary by EVVO to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Customers should obtain and confirm the latest product information and specifications before final design, purchase, or use. EVVO makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does EVVO assume any liability for application assistance or customer product design. EVVO does not warrant or accept any liability for products that are purchased or used for any unintended or unauthorized application.

EVVO products are not authorized for use as critical components in life support devices or systems without the express written approval of EVVOSEMI.

The EVVO logo and EVVOSEMI are trademarks of EVVOSEMI or its subsidiaries in relevant jurisdictions. EVVO reserves the right to make changes without further notice to any products herein.