

Power Distribution Switch with Fixed Current Limit

Features

- Integrated P-channel MOSFET power switch
- Input voltage: 2.5V to 5.5V
- Fix current limit
- Switch on-resistance(typ.):
R_{dson}=65mΩ at V_{IN}=5V
- ±10% current limit accuracy
- Reverse current protection
- Internal EN pull-down/up resistor
- Under voltage lockout
- Over temperature protection
- Quick Output Discharge(QOD)
- SOT23-5L package
- Certificated by UL(AW35045CD/45LCD)
UL62368-1: 2021, file no. E542176
- Certificated by CB(AW35045CD/45LCD)
IEC62368-1:2018, file no. E542176

Applications

USB Ports

Power Distribution Switch

Notebook and Desktop Computer

High-Definition Television(HDTV)

Typical Application Circuit

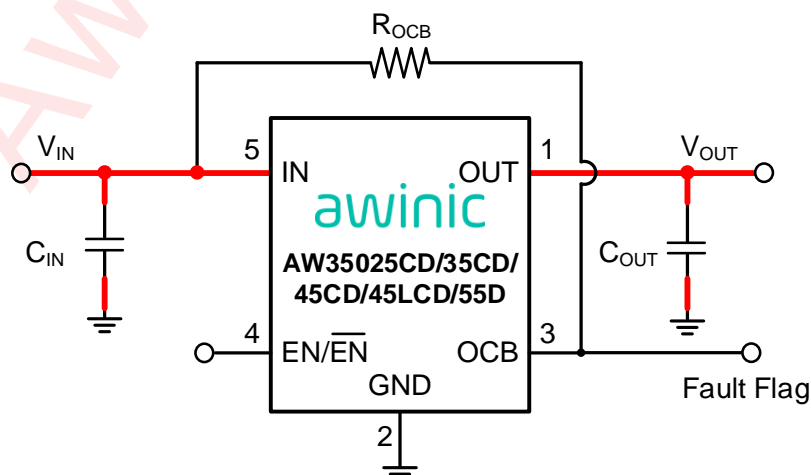


Figure 1 Typical Application Circuit of AW35025CD/35CD/45CD/45LCD/55D

General Description

The AW35025CD/35CD/45CD/45LCD/55D is a P-channel MOSFET power distribution switch which intended for high-side load-switching applications. The device integrates current limit function to protect power source from over current and short circuit condition. Besides, a flag output is available to indicate fault conditions.

The AW35025CD/35CD/45CD/45LCD/55D also features fast short-circuit response, under voltage lockout, over temperature protection, reverse current protection. The AW35025CD/35CD/45CD/45LCD/55D builds in quick output discharge function.

Fixed current limit selection table:

AW35025CD	1.1A fixed current limit
AW35035CD	1.5A fixed current limit
AW35045CD AW35045LCD	2.1A fixed current limit
AW35055D	2.5A fixed current limit

Pin Configuration And Top Mark

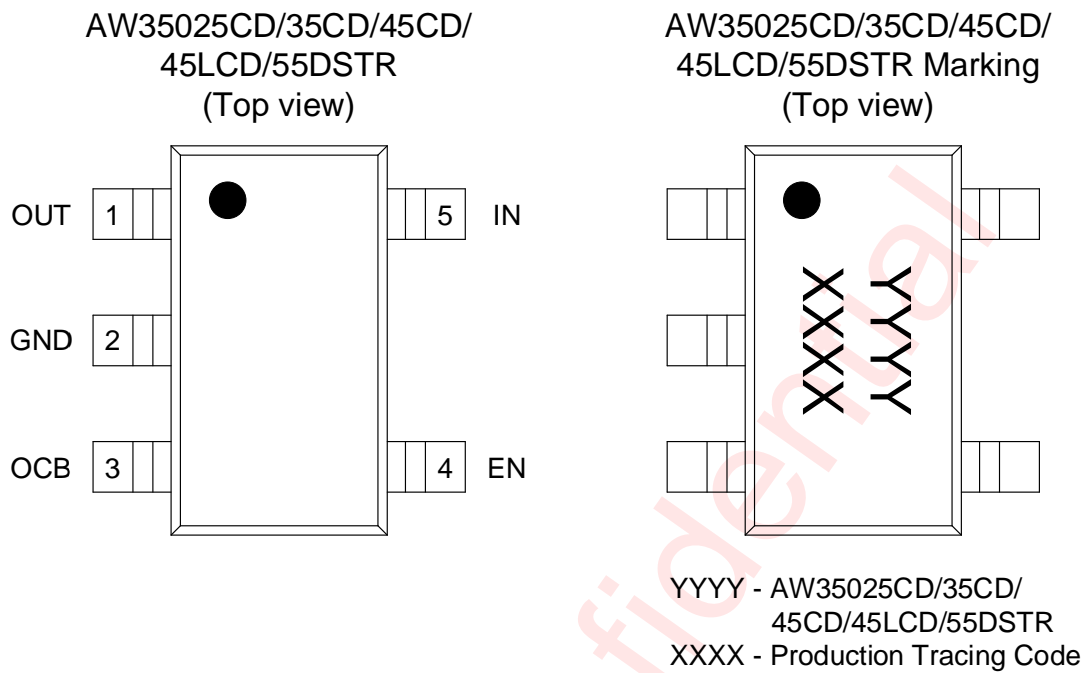


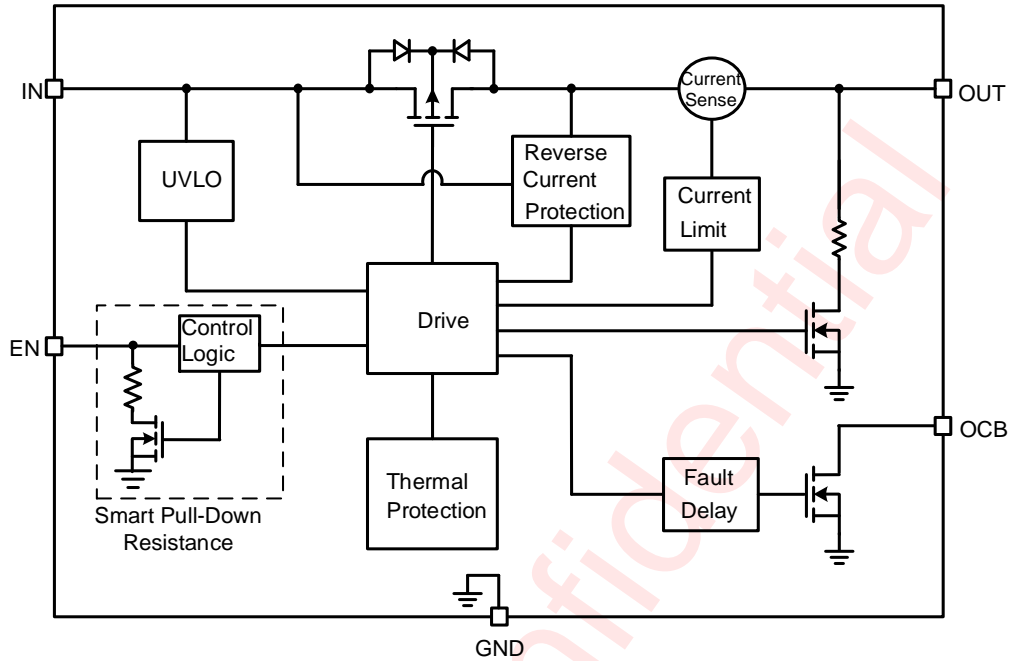
Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin	Name	Description
1	OUT	Output pin
2	GND	Ground
3	OCB	Fault flag output
4	EN/EN	Chip enable (Active High/Low)
5	IN	Power supply input

Functional Block Diagram

- For Enable Active High Version



- For Enable Active Low Version

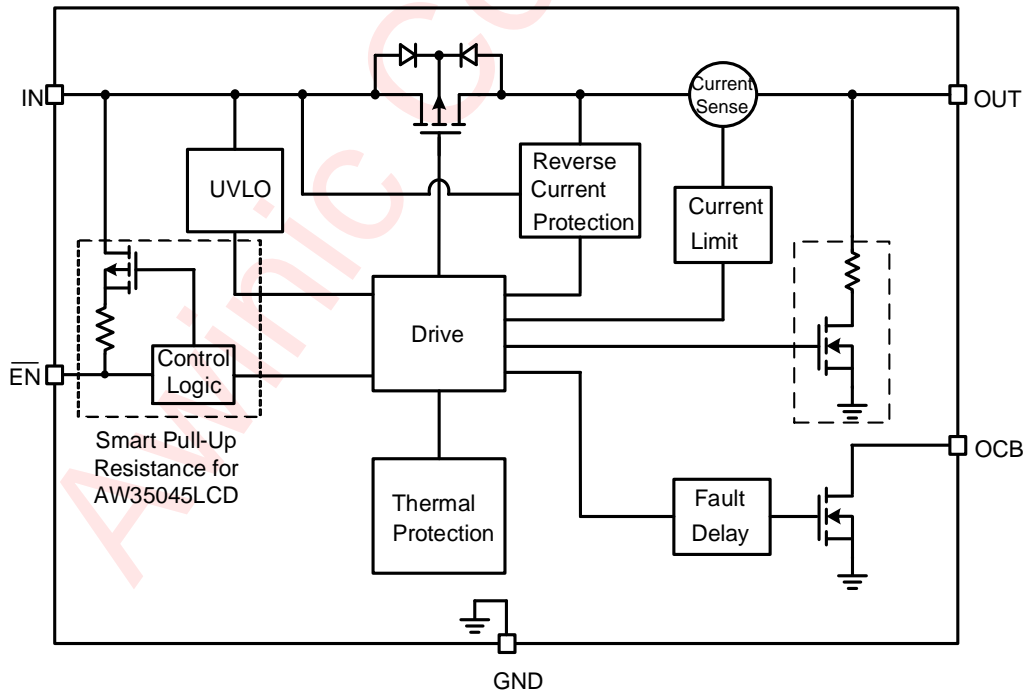


Figure 3 Functional Block Diagram

Typical Application Circuits

- For Enable Active High Version

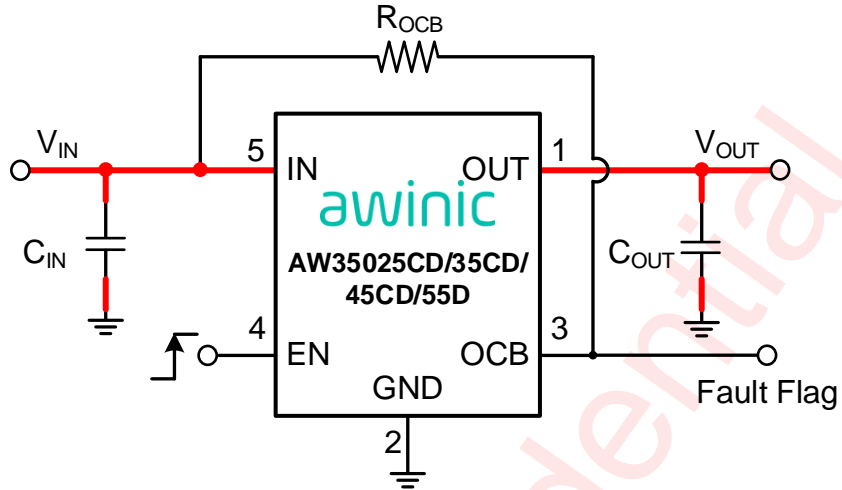


Figure 4 Typical Application Circuit of AW35025CD/35CD/45CD/55D

- For Enable Active Low Version

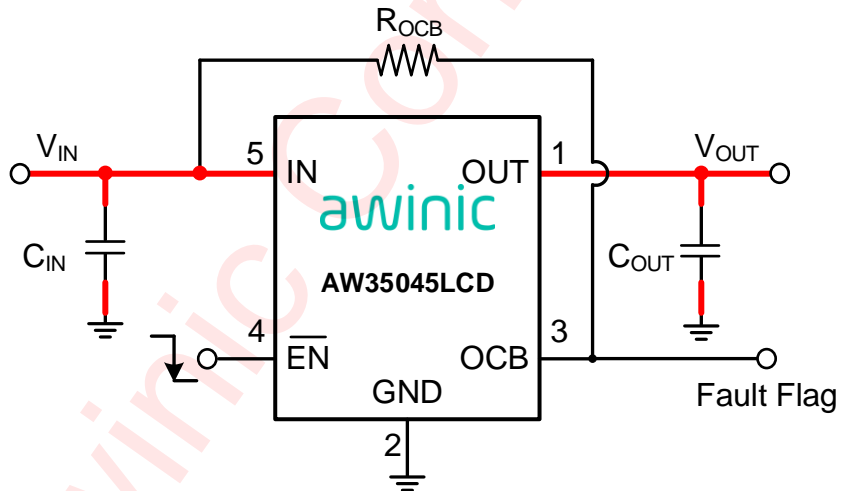


Figure 5 Typical Application Circuit of AW35045LCD

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35025CDSTR	-40°C ~ 85°C	SOT23-5L	D8VA	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35035CDSTR	-40°C ~ 85°C	SOT23-5L	D72K	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35045CDSTR	-40°C ~ 85°C	SOT23-5L	K63T	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35045LCDSTR	-40°C ~ 85°C	SOT23-5L	62HA	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW35055DSTR	-40°C ~ 85°C	SOT23-5L	6G6L	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
EN Voltage Range	EN	-0.3V to 6V
Output Voltage Range	OUT	-0.3V to 6V
Maximum Continuous Switch Current for $V_{IN} \geq 2.5V$ ^(NOTE 2)		2.5A
Maximum Peak Switch Current for $V_{IN} \geq 2.5V$ ^(NOTE 3)		2.8A
Junction-to-ambient thermal resistance θ_{JA} ^(NOTE 4)		158.9°C/W
Junction-to-case thermal resistance θ_{JC}		57°C/W
Operating Free-air Temperature Range		-40°C to 85°C
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD		
HBM (Human Body Model) ^(NOTE 5)		±2kV
CDM(Charged Device Model) ^(NOTE 6)		±1.5kV
Latch-Up		
Test Condition: JEDEC78E.		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Limited by thermal design.

NOTE3: Limited by thermal design, and tested in 10ms width pulse current.

NOTE4: Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout.

NOTE5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE6: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	2.5		5.5	V
V_{EN}	EN Voltage	0		5.5	V
V_{OUT}	Output Voltage	0		V_{IN}	V
C_{IN}	Input capacitance	0.1	1		μF
C_{OUT}	Output capacitance	0.1	1		μF

Electrical Characteristics

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 1μF, I_{IN} ≤ 2.5A.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT	
SUPPLY CURRENT							
I _Q	Input quiescent current	V _{IN} =5.0V, EN(EN)=Active, I _{OUT} =0A		30		μA	
I _{SD}	Shutdown current from IN to GND	V _{IN} =5.0V, EN(EN)=Inactive		0.32	1	μA	
I _{LEAKEN}	EN pin leakage current	V _{IN} =0V, V _{EN} =5.5V		0.52	1	μA	
POWER SWITCH							
R _{dson}	Internal switch MOSFET on-state resistance	V _{IN} =5.0V, I _{OUT} =500mA		65		mΩ	
R _{EN}	EN pin pull down resistor	V _{IN} =5V, V _{EN} =0.1V (AW35025CD/35CD/45CD/55D)		9.2		MΩ	
	EN pin pull up resistor	V _{IN} =5V, V _{EN} =3V (AW35045LCD)					
R _{DIS}	Output discharge resistance	V _{IN} =5.0V, EN(EN)=Inactive, I _{OUT} Sinking 2mA		75		Ω	
t _R	Output rise time	V _{IN} =5.0V, C _{OUT} =1μF, R _L =100Ω		1.5		ms	
t _{ON}	Switch turn on time			2.3		ms	
t _F	Output fall time			93		μs	
t _{OFF}	Switch turn off time			99		μs	
V _{IH}	EN input high threshold level		1.4			V	
V _{IL}	EN input low threshold level				0.4	V	
CURRENT LIMIT							
I _{LIMIT}	Current limit threshold	V _{OUT} =4V	AW35025CD	1100	1225	1350	mA
			AW35035CD	1500	1665	1830	
			AW35045CD/45LCD	2100	2335	2570	
			AW35055D	2500	2780	3060	
t _{IOS}	Response time to short circuit	V _{IN} =5.0V			10		μs
t _{OCF}	Current-limit response time	V _{IN} =5.0V, I _{OUT} =1.5 × I _{LIMIT}			100		μs
UNDER VOLTAGE LOCKOUT							
V _{UVLO}	UVLO threshold voltage	V _{IN} rising			2.3	2.5	V
V _{UVLO_HYS}	UVLO hysteresis	V _{IN} falling			95		mV

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise noted. Typical values are guaranteed for V_{IN} = 5V, C_{IN} = 1μF, I_{IN} ≤ 2.5A.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
REVERSE VOLTAGE PROTECT						
V _{REV}	Reverse voltage trip point	EN(EN)=Active, V _{OUT} > V _{IN}		43		mV
I _{REV}	Reverse leakage current	V _{OUT} =5V, V _{IN} =0V, EN(EN)=Inactive		0.68		μA
I _{REV_ACT}	Reverse activation current	V _{IN} =5V, C _{OUT} =1μF, V _{OUT} > V _{IN}		0.6		A
I _{REV_PRO}	Reverse protection current	V _{OUT} - V _{IN} > V _{REV}		5		μA
FAULT FLAG						
R _{OCB}	OCB output low Resistance	V _{IN} =5V, I _{SINK} =1mA		190		Ω
I _{LEAK_OCB}	OCB off-state leakage current	V _{OCB} =5.5V		0.03		μA
t _{OCB}	OCB delay time	V _{IN} =5V, From fault condition to OCB assertion		2		ms
THERMAL PROTECTION						
T _{SD}	Thermal shutdown threshold			155		°C
T _{SD_HYS}	Thermal shutdown hysteresis			25		°C

Timing Diagram

- For Enable Active High Version

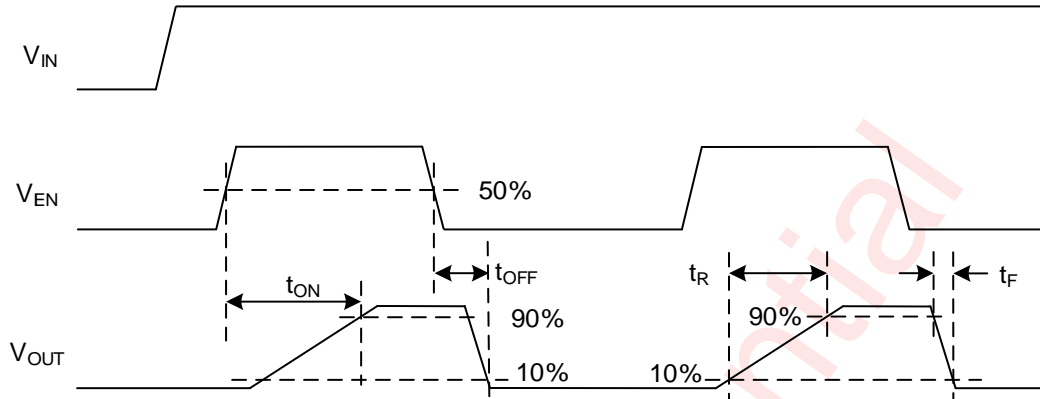


Figure 6 AW35025CD/35CD/45CD/55D Timing Diagram

- For Enable Active Low Version

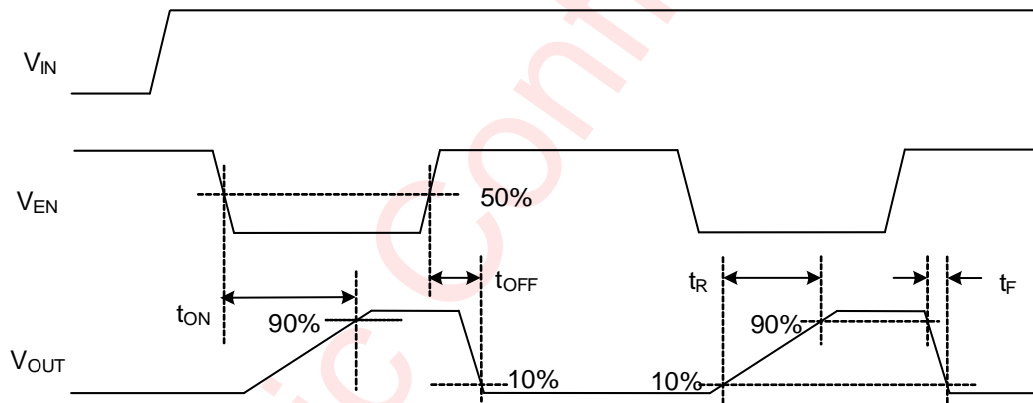


Figure 7 AW35045LCD Timing Diagram

Typical Characteristics

Ambient temperature is 25°C, $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted.

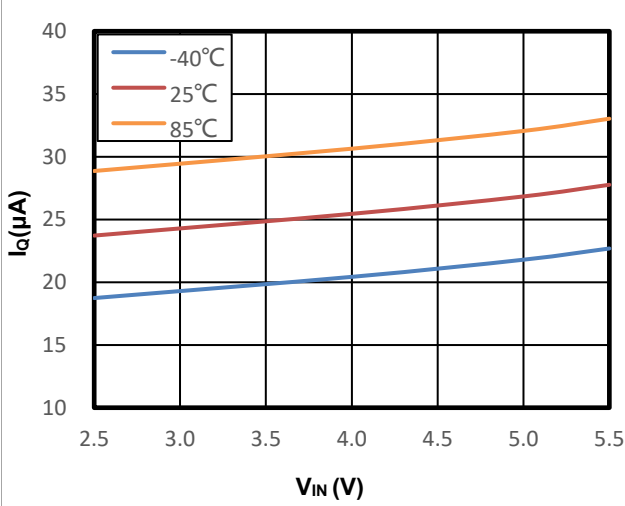


Figure 8 Quiescent Current vs. V_{IN}, No load

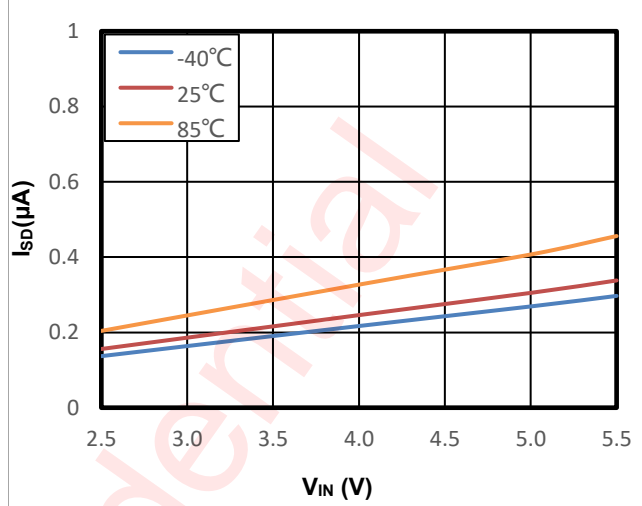


Figure 9 IN Shutdown Current vs. V_{IN}

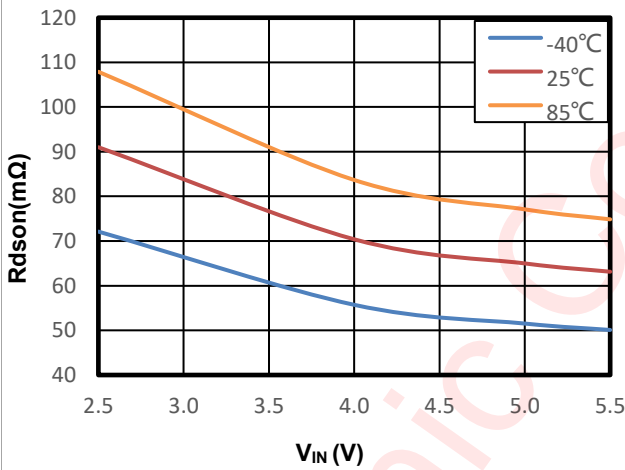


Figure 10 Rdson vs. V_{IN} (I_{OUT}=500mA)

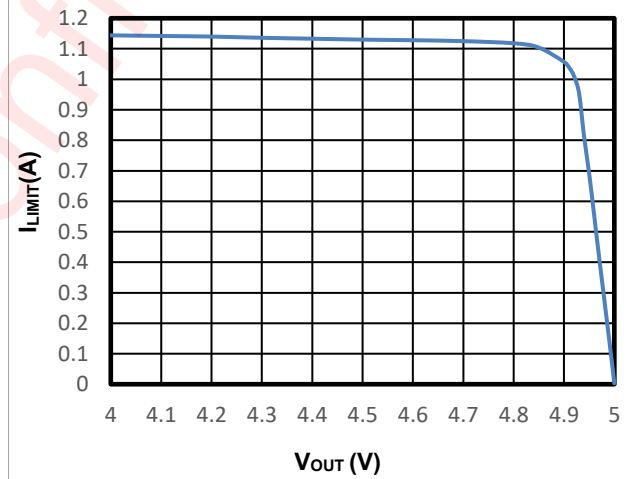


Figure 11 I_{LIMIT} vs. V_{OUT}
(AW35025CD)

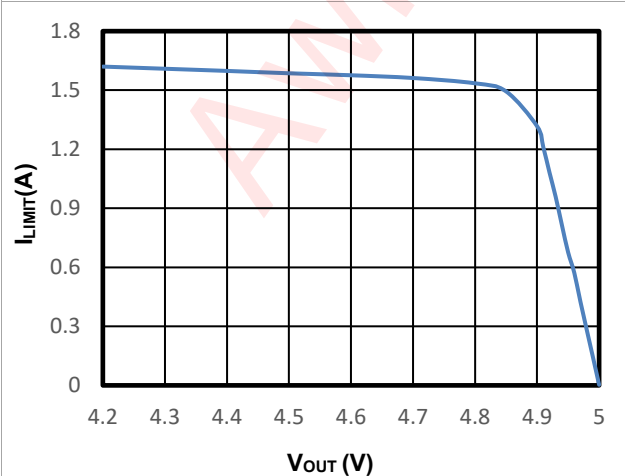


Figure 12 I_{LIMIT} vs. V_{OUT}
(AW35035CD)

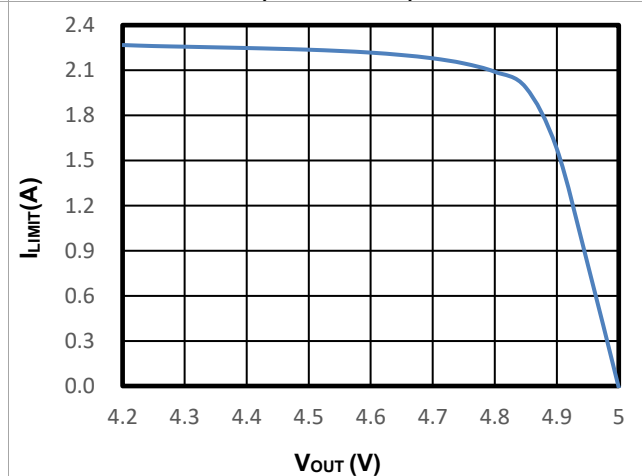


Figure 13 I_{LIMIT} vs. V_{OUT}
(AW35045CD/45LCD)

Typical Characteristics (continued)

Ambient temperature is 25°C, $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted.

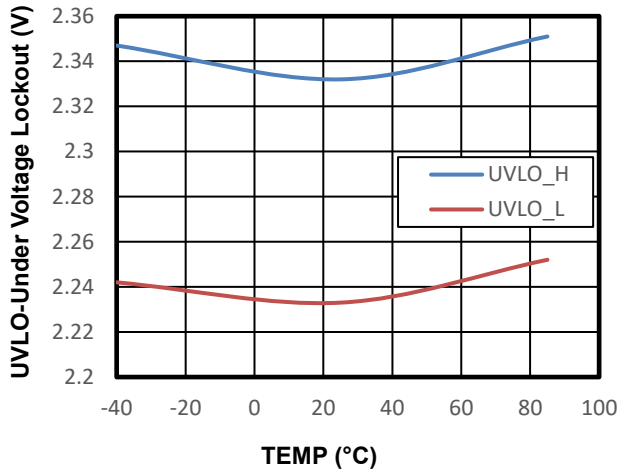
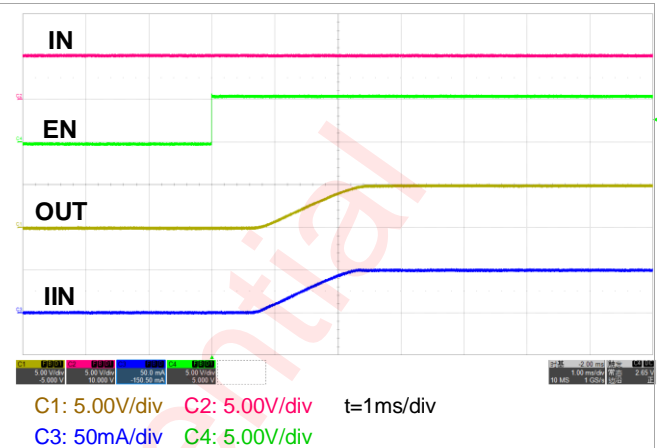
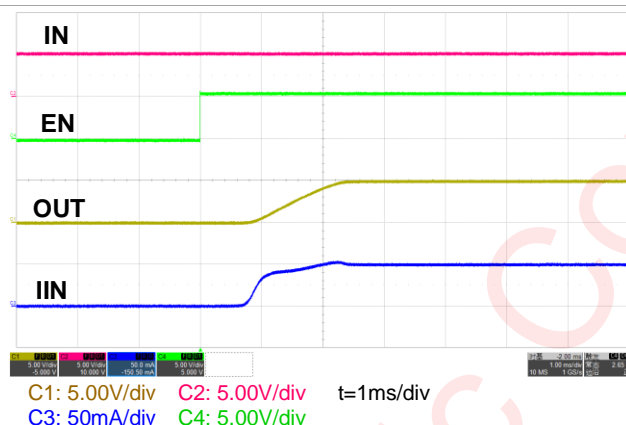


Figure 14 UVLO vs. TEMP



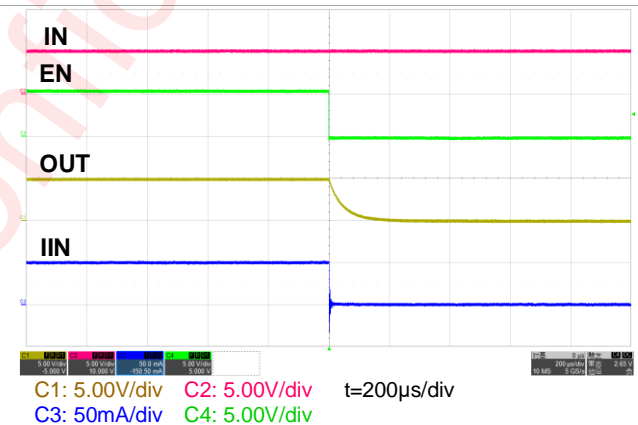
$V_{IN} = 5V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $R_L = 100\Omega$

Figure 15 Turn On Response



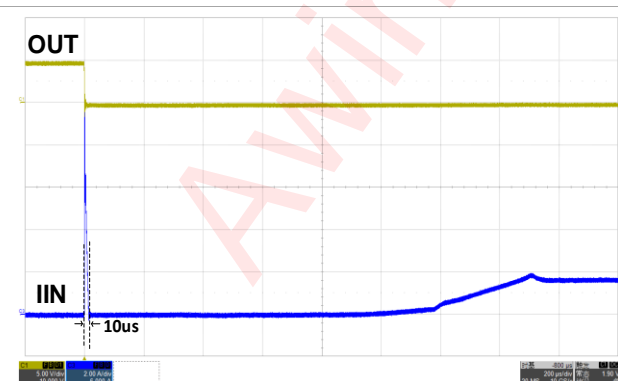
$V_{IN} = 5V$, $C_{IN} = 1\mu F$, $C_{OUT} = 10\mu F$, $R_L = 100\Omega$

Figure 16 Turn On Response



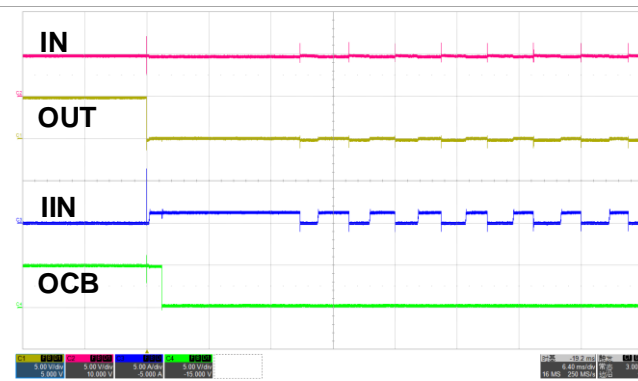
$V_{IN} = 5V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $R_L = 100\Omega$

Figure 17 Turn Off Response



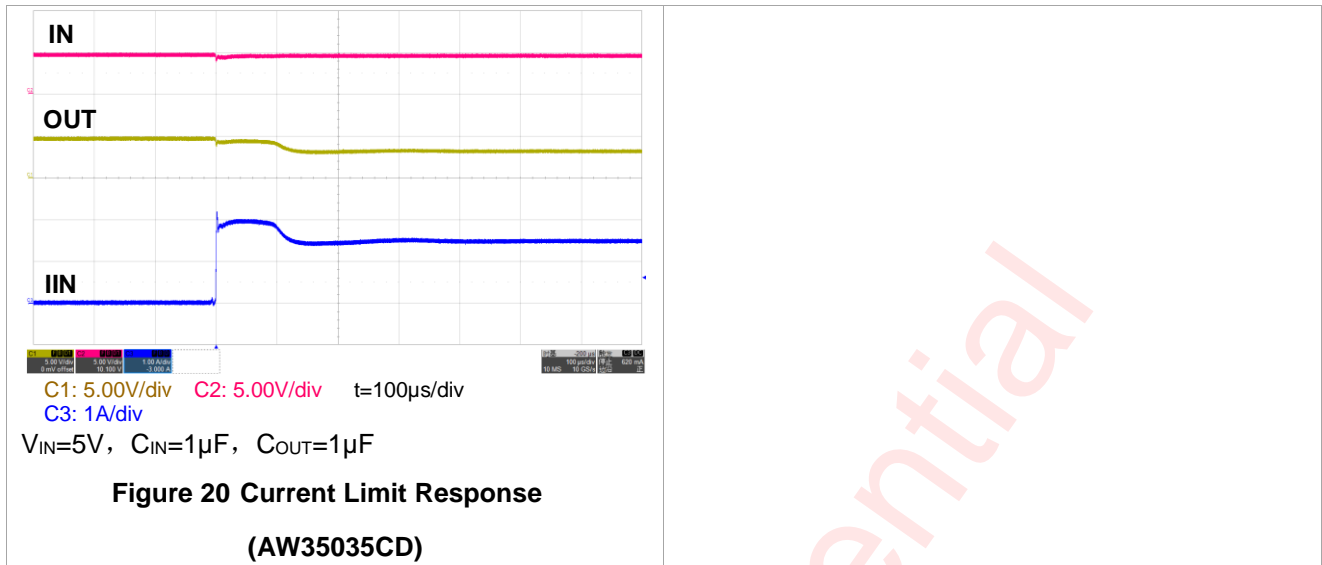
$V_{IN} = 5V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$

Figure 18 Short Circuit Response
(AW35035CD)



$V_{IN} = 5V$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$

Figure 19 Continuous Short Response



Functional Description

The AW35025CD/35CD/45CD/45LCD/55D is a P channel MOSFET power distribution switch with current limit function. In addition, the switch also features fast short-circuit response, under voltage lockout, over temperature protection and reverse current protection.

Current Limit Threshold Setting

The AW35025CD/35CD/45CD/45LCD/55D provides fixed current limit threshold. The current limit function can prevent the switch from over current condition.

AW35025CD	1.1A fixed current limit
AW35035CD	1.5A fixed current limit
AW35045CD/45LCD	2.1A fixed current limit
AW35055D	2.5A fixed current limit

Fast Short Circuit Protection

The AW35025CD/35CD/45CD/45LCD/55D provides short circuit protection function which can limit the output current to a safe level without damaging the switch.

Under Voltage Lockout (UVLO)

The AW35025CD/35CD/45CD/45LCD/55D has under voltage lockout function which can disable the switch until the input voltage reaches the UVLO threshold (typical 2.3V). The UVLO threshold has a 95mV hysteresis voltage which can prevent the unwanted on/off cycling when there is noise on the input voltage.

Over Temperature Protection (OTP)

When the junction temperature exceeds 155°C, the internal OTP circuit turn off the power switch. There is a temperature hysteresis 25°C, in other words, the OTP circuit can turn on the switch only if the junction temperature is below 130°C.

Quick Output Discharge

The AW35025CD/35CD/45CD/45LCD/55D include the Quick Output Discharge (QOD) feature, in order to discharge the application capacitor connected on OUT pin. When EN pin is set to low level, a discharge resistance with a typical value of 75Ω is connected between the output and ground, pull down the output and prevent it from floating when the device is disabled.

Reverse Current Protection (RCP)

The AW35025CD/35CD/45CD/45LCD/55D includes the Reverse Current Protection(RCP) function, which can prevent the current to flowing through the P-FET or the body diode when V_{OUT} greater than V_{IN} . Whatever the switch is on or off, the AW35025CD/35CD/45CD/45LCD/55D always has this function. When $V_{OUT}-V_{IN}$ greater than V_{REV} , the internal comparator quickly turns off the switch, in order to prevent large reverse current from V_{OUT} to V_{IN} . The switch will return to normal operation once the reverse voltage scenario disappeared.

The I_{REV_ACT} parameter in the figure 21 can be calculated by the following formula:
$$I_{REV_ACT} = \frac{V_{REV}}{R_{dson}}$$

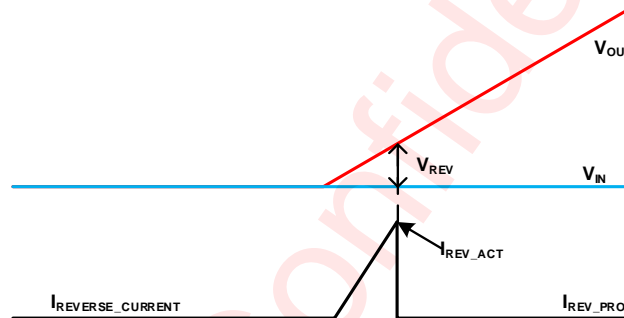


Figure 21 RCP parameter diagram

OCB Output

The AW35025CD/35CD/45CD/45LCD/55D provides an open-drain output to indicate that a fault condition has occurred. When any of over current or over temperature or reverse current protection occurs for a deglitch time of t_{OCB} , the OCB goes low. If fault condition remove, OCB will goes high. Connect a resistor to between OCB and V_{IN} for normal work.

Application Information

Input and Output Capacitor Selection

Input and output capacitance improves the performance of the device, the actual capacitance should be optimized for the particular application. For all applications, a $1\mu\text{F}$ or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions.

Placing a $1\mu\text{F}$ or greater ceramic capacitor on the output pin is recommended when large transient currents are expected on the output.

PCB Layout Consideration

AW35025CD/35CD/45CD/45LCD/55D is a low ON-Resistance power switch, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor C_{IN} on the top layer (same layer as the AW35025CD/35CD/45CD/45LCD/55D) and close to IN pin, and place the output capacitor C_{OUT} on the top layer (same layer as the AW35025CD/35CD/45CD/45LCD/55D) and close to OUT pin.
2. AW35025CD/35CD/45CD/45LCD/55D integrates an up to 2.5A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation. Blue bold paths on Figure 22 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.
3. Use rounded corners on the power trace from the power supply connector to AW35025CD/35CD/45CD/45LCD/55D to decrease EMI coupling.

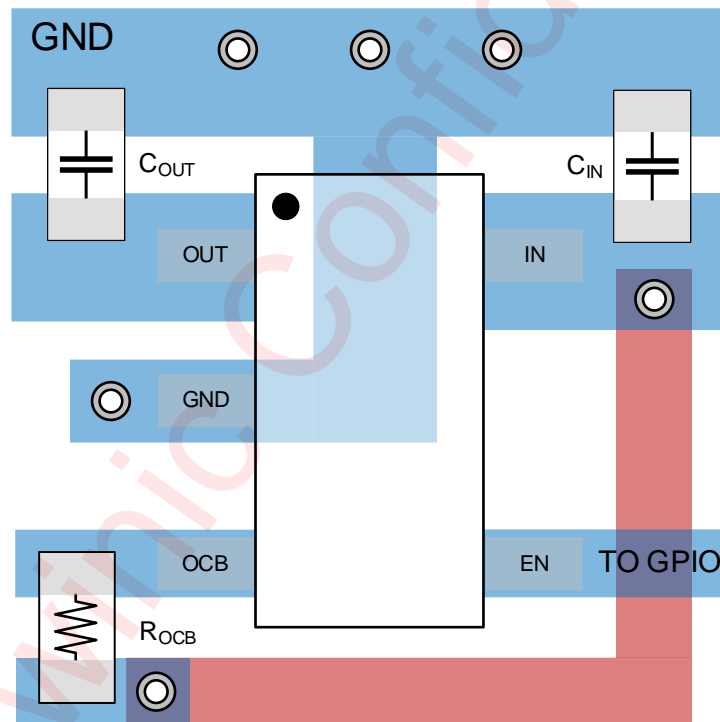
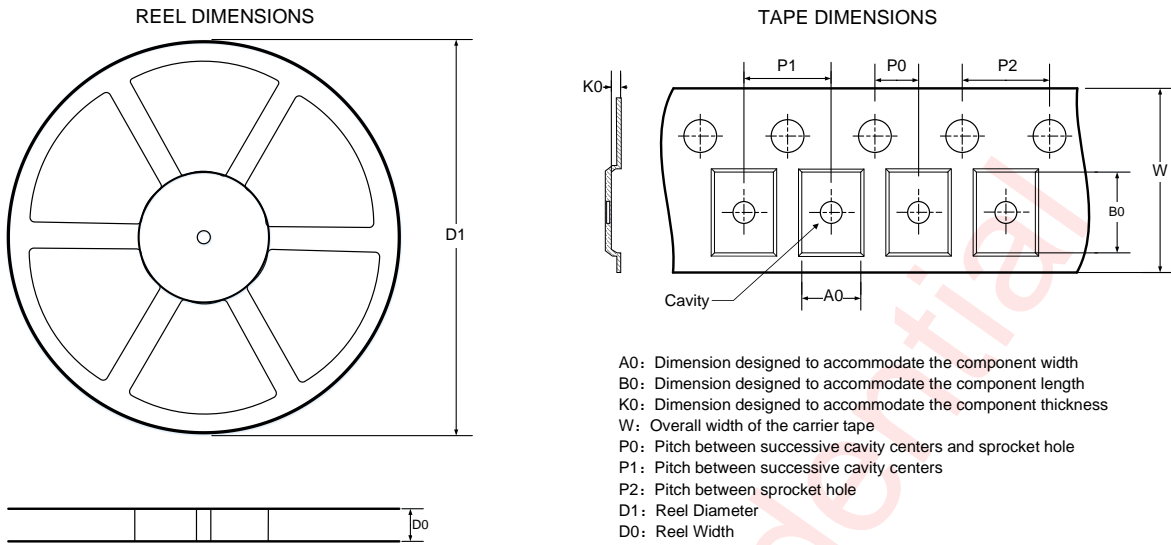
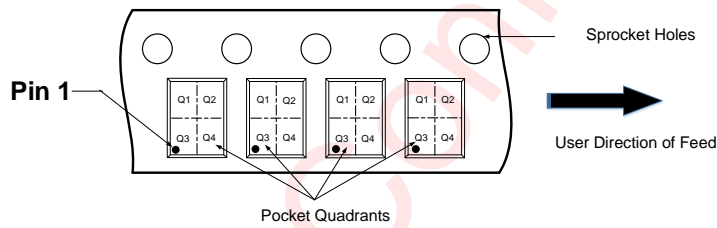


Figure 22 PCB layout example

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



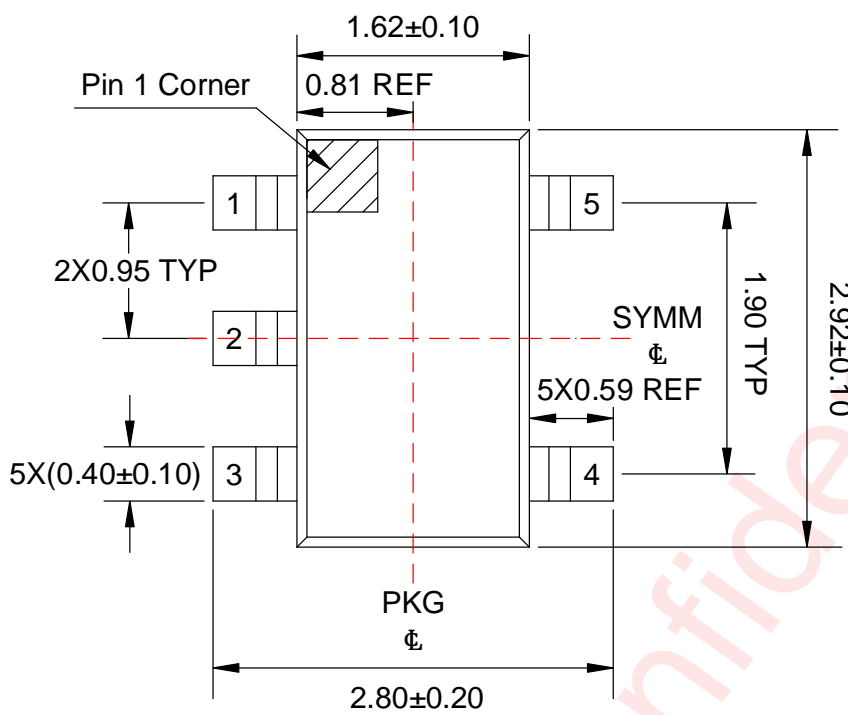
Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

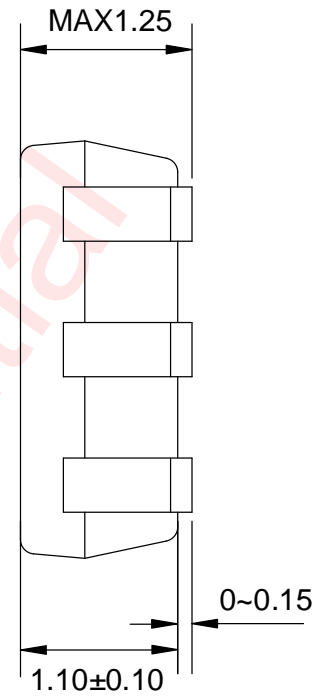
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.5	3.3	3.2	1.4	2	4	4	8	Q3

All dimensions are nominal

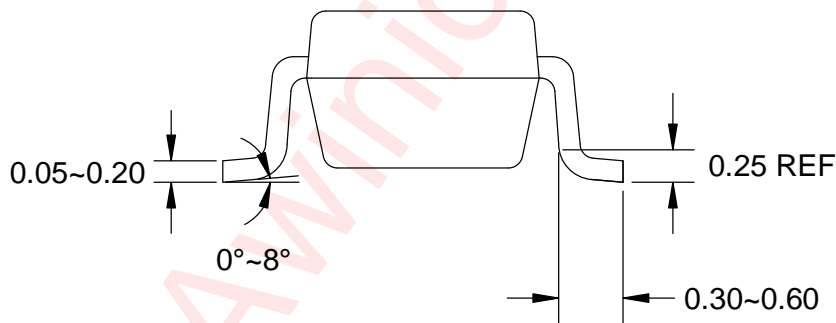
Package Description



Top View



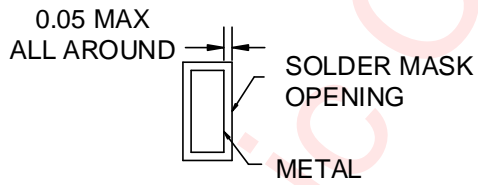
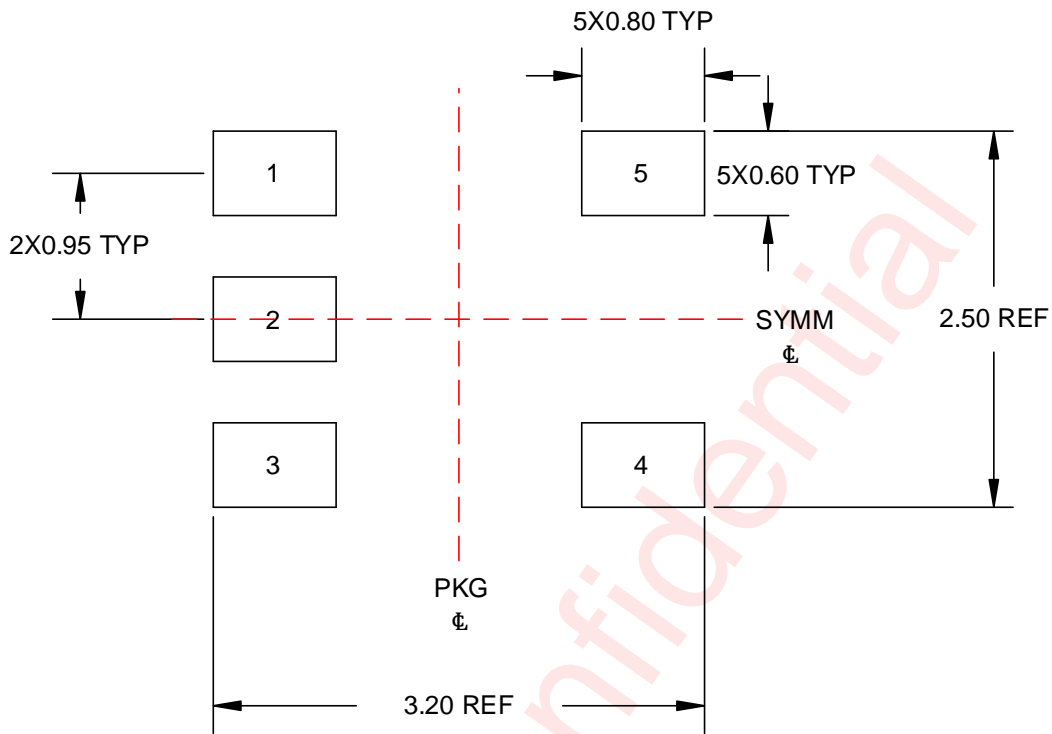
Side View



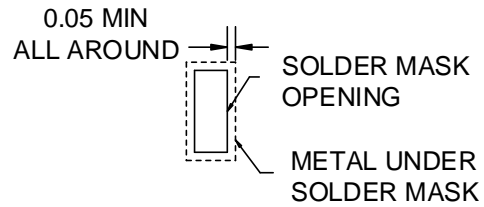
Side View

Unit: mm

Land Pattern Data



NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2024	Officially released
V1.1	Aug. 2024	Add UL/CB certificate file number(P1)
V1.2	Dec. 2024	1. Add the parameter of θ_{JC} (P6) 2. Update the figure of "Turn On Response".(P11)

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