1. General Description

The EM74HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input ($\overline{MR}$) clears the register and forces all outputs LOW, independently of otherinputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and Benefits

- High noise immunity
- CMOS low power dissipation
- Gated serial data inputs
- Asynchronous master reset
- Latch-up performance exceeds 250 mA
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

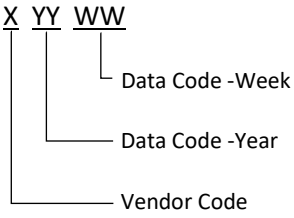
3. Ordering Information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Quantity
EM74HCT164D	HCT164 XYYWW	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	3000
EM74HCT164PW	HCT164 XYYWW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	3000

MARKING INFORMATION

NOTE: XYYWW = Vendor Code and Data Code.



4. Function Diagram

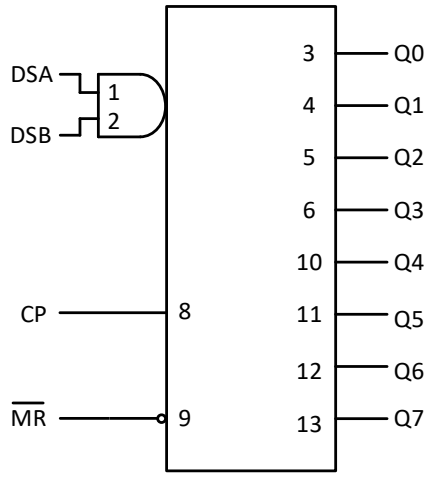


Fig. 1. Logic symbol

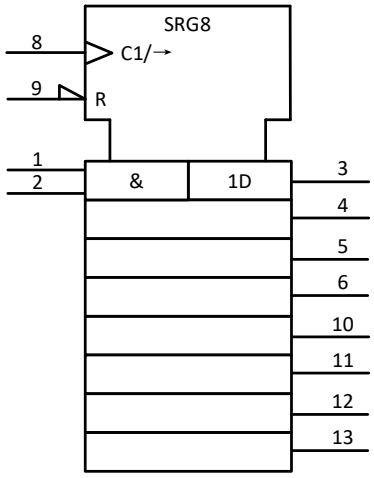


Fig. 2. IEC logic symbol

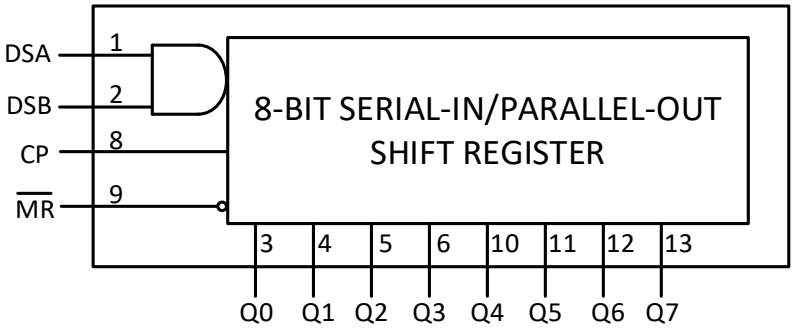


Fig. 3. Logic diagram

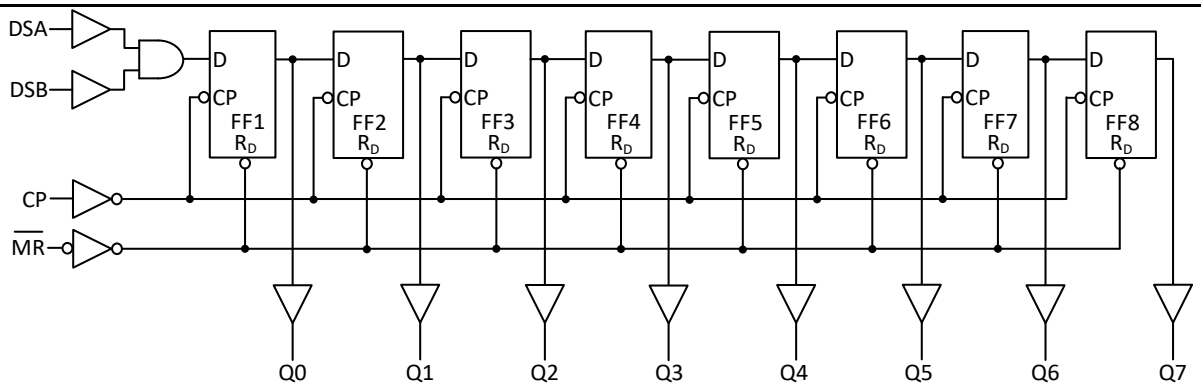


Fig. 4. Functional diagram

5.Pinning Information

5.1. Pinning

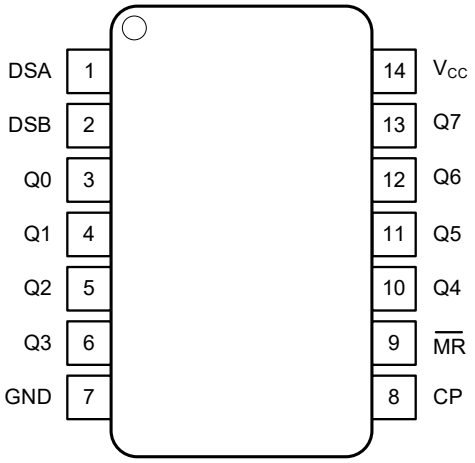


Fig. 5. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input
DSB	2	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 4, 5, 6, 10, 11, 12, 13	output
CP	8	clock input (LOW-to-HIGH, edge-triggered)
$\overline{MR}$	9	master reset input (active LOW)
V_{CC}	14	supply voltage
GND	7	ground

6.Functional Description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition; L = LOW voltage level; I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition; ↑ = LOW-to-HIGH transition; X = don't care

Operating modes	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset(clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		±25	mA
I_{CC}	supply current			50	mA
I_{GND}	ground current		-50		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	EM74HCT164			Unit
			Min	Typ	Max	
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	V
V_O	output voltage		0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V		1.67	139	ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.5		2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V		1.2	0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20μA;	4.4	4.5		4.4		V
		I_O = -4.0 mA;	3.84	4.4		3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20μA;		0.01	0.1		0.1	V
		I_O = -5.2 mA;		0.04	0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V		0.01	±1		±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 5.5 V		10	20		40	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; IO = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V		180	300		350	μA
C_I	input capacitance	Pin DSA,DSB,CP		7.0				pF
		Pin MR		3.0				pF

[1]All typical values are measured at T_{amb} = 25°C.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 6 [2]						
		V_{CC} = 4.5 V		11.5	18		21	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 7						
		V_{CC} = 4.5 V		12.1	18		21	ns
t_t	transition time	see Fig. 6 [3]						
		V_{CC} = 4.5 V		3.5	7		9	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 6						
		V_{CC} = 4.5 V			23		27	ns
		$\overline{MR}$ LOW; see Fig. 7						
		V_{CC} = 4.5 V			23		27	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 7						
		V_{CC} = 4.5 V			20		24	ns
t_{SU}	set up time	DSA and DSB to CP; see Fig. 8						
		V_{CC} = 4.5 V			15		18	ns
t_h	hold time	DSA and DSB to CP; see Fig. 8						
		V_{CC} = 4.5 V			4		4	ns
f_{max}	maximum frequency	for CP; see Fig. 6						
		V_{CC} = 4.5 V			22		18	MHz
C_{PD}	power dissipation capacitance	per package ; V_I = GND to V_{CC} – 1.5 V ; [4]		43				pF

[1] Typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_t is the same as t_{THL} and t_{THL}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

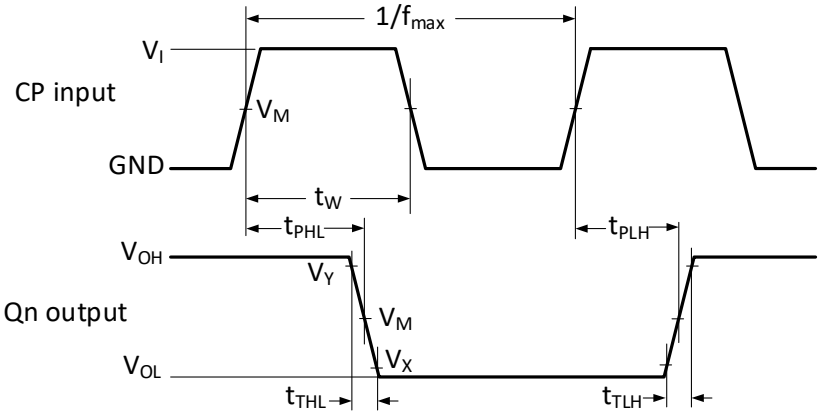
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

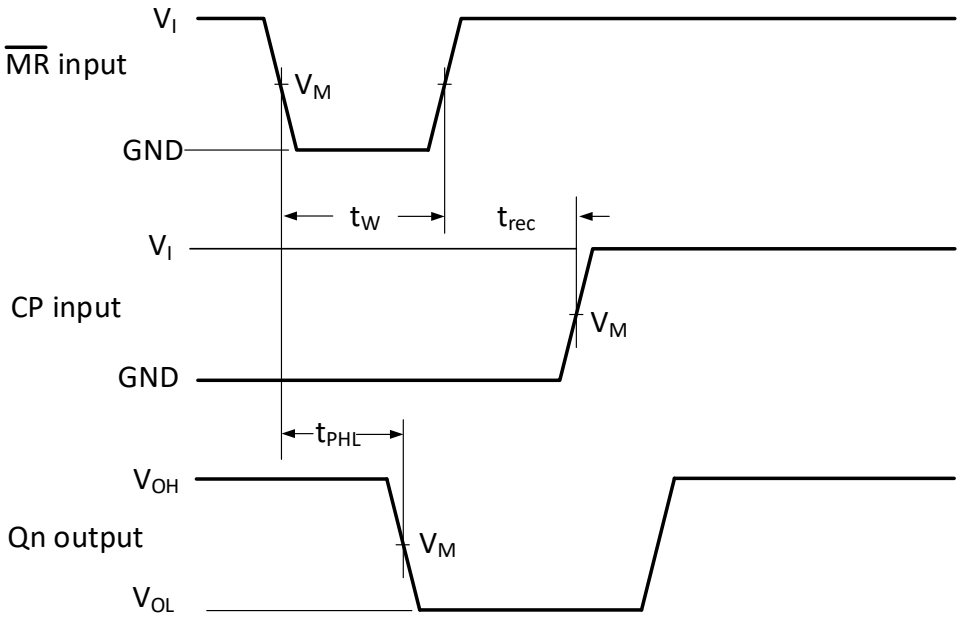
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



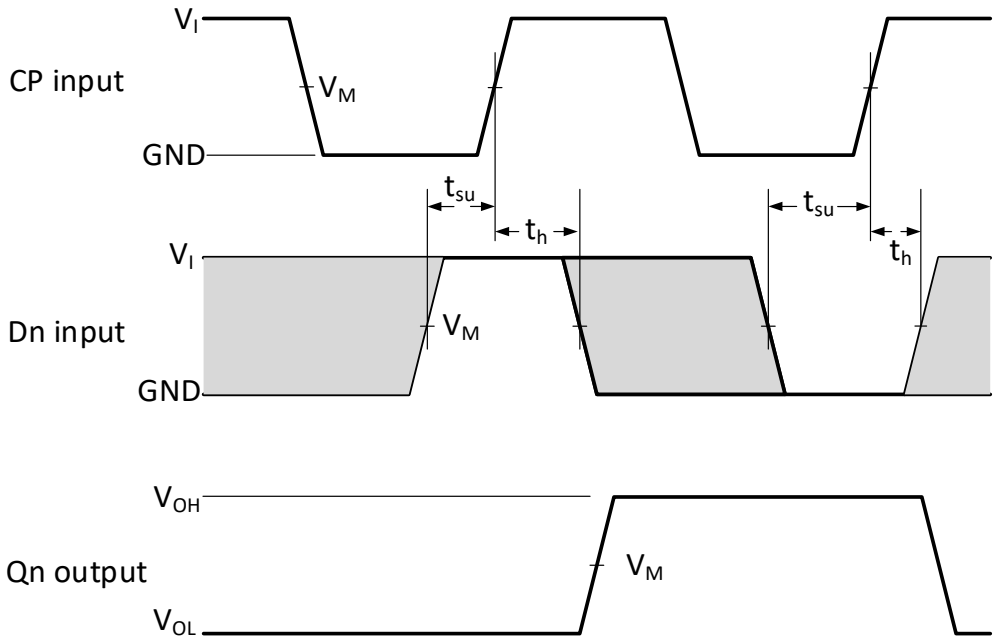
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time

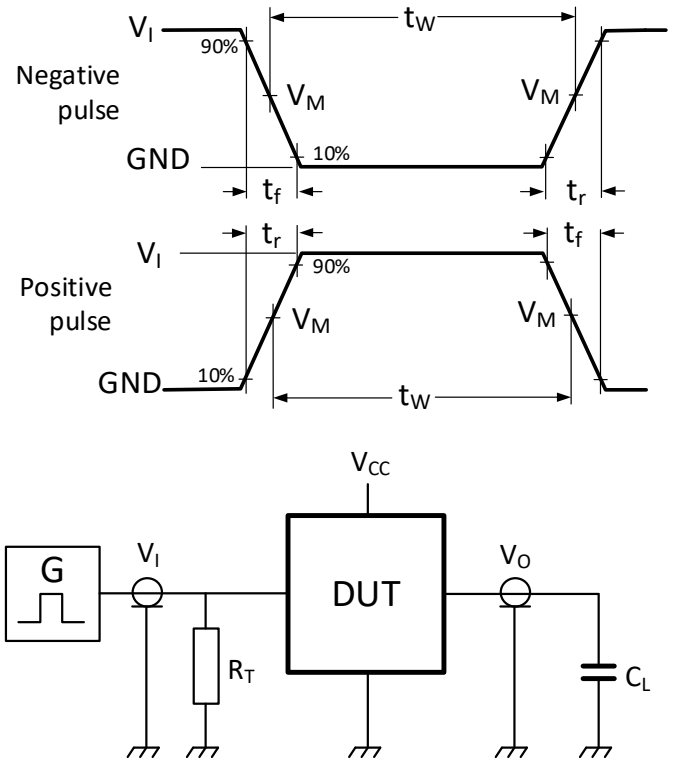


Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Waveforms showing the data set-up and hold times for Dn inputs

Table 8. Measurement points

Type	Input	Output		
	V_I	V_M	V_X	V_Y
EM74HCT164	3.0V	1.3V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.
Definitions for test circuit:
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

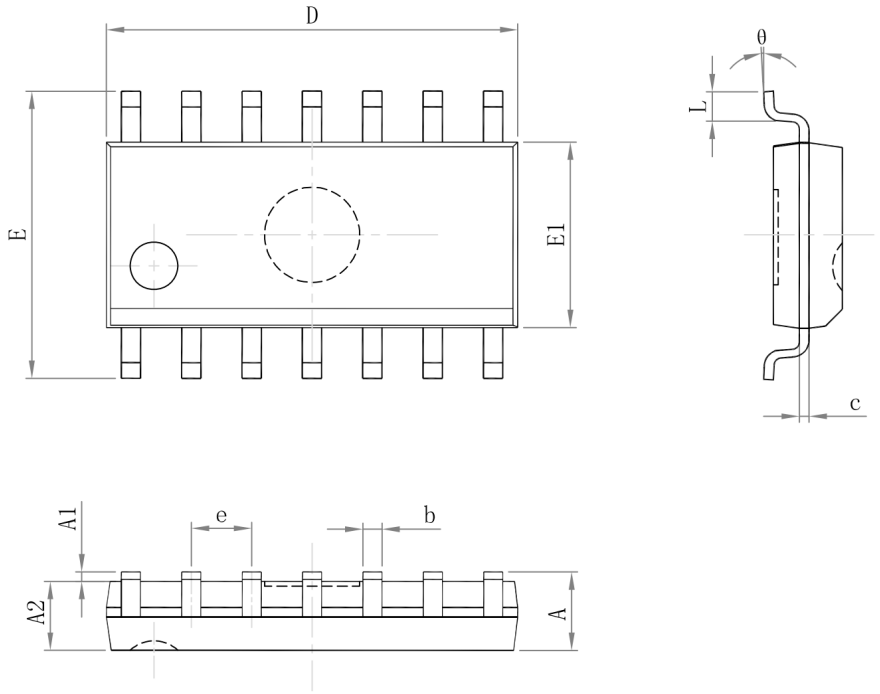
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	$t_r = t_f$	C_L	
EM74HCT164	3.0V	2.5 ns	50 pF	t_{PHL}, t_{PLH}

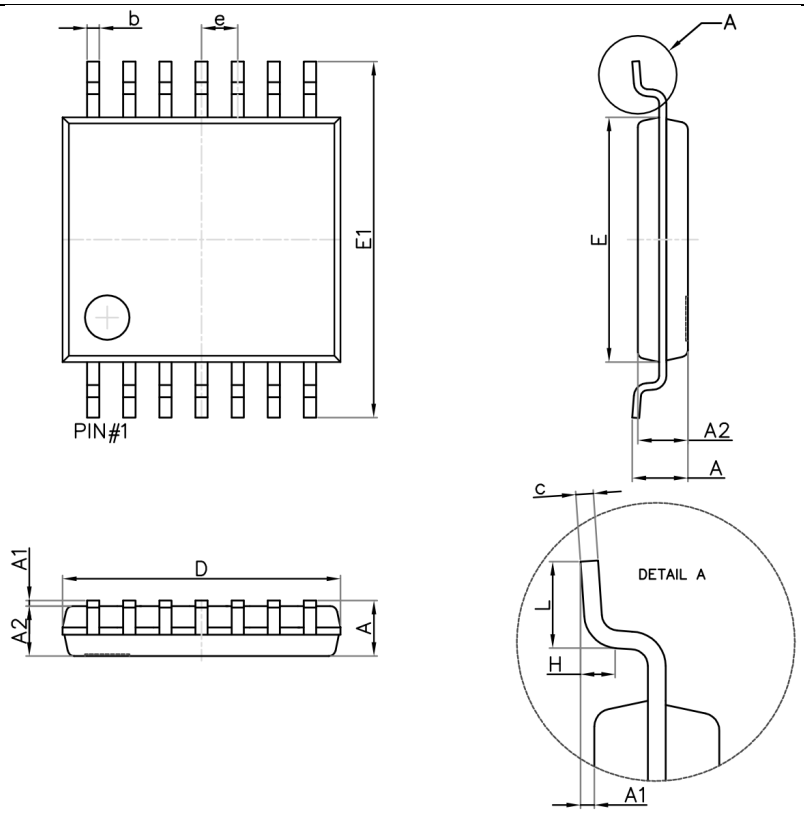
11. Package Outline

SOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	—	1.200	—	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
TTL	Transistor-Transistor Logic
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
EM74HCT164 Rev. 1.0	Mar 18, 2025	Product datasheet		