2.5A, Dual-Input, Single Cell Switch Mode Li-Ion Battery Charger with Power Path Management

Check for Samples: bq24165 , bq24166, bq24167

FEATURES

- High-Efficiency Switch Mode Charger with Separate Power Path Control
  - Make a GSM Call with a Deeply Discharged Battery or No Battery
  - Instantly Startup System from a Deeply Discharged Battery or No Battery
- Dual Input Charger
  - 20V Input Rating, With Over-Voltage Protection (OVP)
    - 6.5V for USB Input
    - 10.5V for IN Input
  - Integrated FETs for Up to 2.5A Charge Rate
    - Up to 2.5A from IN Input
    - Up to 1.5A from USB Input
- Highly Integrated Battery N-Channel MOSFET Controller for Power Path Management
- Safe and Accurate Battery Management Functions
  - 0.5% Battery Regulation Accuracy
  - 10% Charge Current Accuracy
- Adjustable Charge Current, Input Current Limit, and VINDPM Threshold (for IN input)
- Easy JEITA Implementation
  - Charge Parameter Selector Inputs ($\overline{CE1}$, $\overline{CE2}$) for (bq24165)
- Voltage-based, NTC Monitoring Input (TS)
  - Standard Temperature Range (bq24166)
  - JEITA Compatible (bq24167)
- Thermal Regulation Protection for Output Current Control
- Low Battery Leakage Current, BAT Short-Circuit Protection
- Soft-Start Feature to Reduce Inrush Current
- Thermal Shutdown and Protection
- Available in Small 2.8mm x 2.8mm 49-ball WCSP or 4mm x 4mm QFN-24 Packages

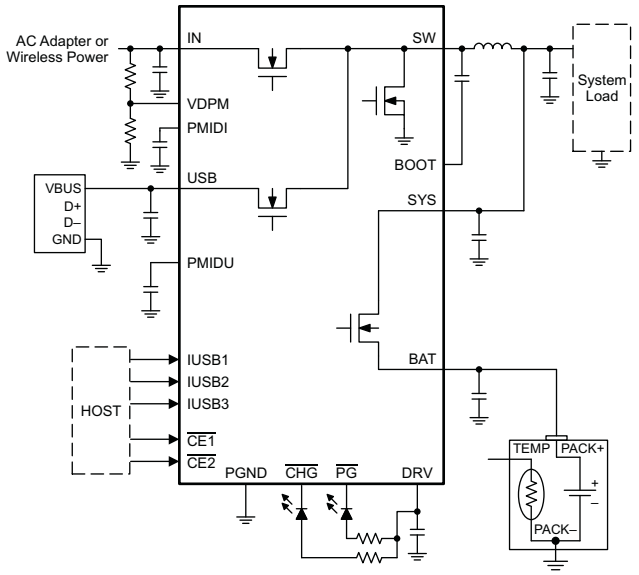
APPLICATIONS

- Handheld Products
- Portable Media Players
- Portable Equipment
- Netbook and Portable Internet Devices

DESCRIPTION

The bq24165, bq24166 and bq24167 are highly integrated single cell Li-Ion battery charger and system power path management devices targeted for space-limited, portable applications with high capacity batteries. The single cell charger has dual inputs which allow operation from either a USB port or higher power input supply (i.e., AC adapter or wireless charging input) for a versatile solution. The two inputs are fully isolated from each other and are managed by the bq24165/166/167 with the IN input having precedence.

APPLICATION SCHEMATIC



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The power path management feature allows the bq24165/166/167 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and timer operation. The system voltage is regulated to the battery voltage but will not drop below 3.5V. This minimum system voltage support enables the system to run with a defective or absent battery pack and enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter. The 2.5A input current capability allows for GSM phone calls as soon as the adapter is plugged in regardless of the battery voltage.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, the bq24166 and bq24167 offer a voltage-based battery pack thermistor monitoring input (TS) that monitors battery temperature for safe charging. The TS function for bq24166 is JEITA compatible.

ORDERING INFORMATION

PART NUMBER	USB OVP	IN OVP	NTC MONITORING (TS)	JEITA COMPATIBLE	Package
bq24165YFFR	6.5V	10.5 V	No	Yes	WCSP
bq24165YFFT	6.5 V	10.5 V	No	Yes	WCSP
bq24165RGER	6.5V	10.5 V	No	Yes	QFN
bq24165RGET	6.5 V	10.5 V	No	Yes	QFN
bq24166YFFR	6.5 V	10.5 V	Yes	No	WCSP
bq24166YFFT	6.5 V	10.5 V	Yes	No	WCSP
bq24166RGER	6.5 V	10.5 V	Yes	No	QFN
bq24166RGET	6.5 V	10.5 V	Yes	No	QFN
bq24167YFFR	6.5 V	10.5 V	Yes	Yes	WCSP
bq24167YFFT	6.5 V	10.5 V	Yes	Yes	WCSP
bq24167RGER	6.5 V	10.5 V	Yes	Yes	QFN
bq24167RGET	6.5 V	10.5 V	Yes	Yes	QFN

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE/UNITS
Pin voltage range (with respect to PGND)	IN, USB	–2 V to 20 V
	PMIDI, PMIDU, BOOT	–0.3 V to 20 V
	SW	–0.7 V to 12V
	ISET, ILIM, SCL, SYS, BAT, BGATE, DRV, $\overline{PG}$, $\overline{CHG}$, VDPM, IUSB_, $\overline{CE}$_,TS	–0.3 V to 7 V
BOOT to SW		–0.3 V to 7 V
Output current (Continuous)	SW	4.5 A
	SYS, BAT	3.5 A
Input current (Continuous)	IN	2.75 A
	USB	1.75 A
Output sink current	$\overline{PG}$, $\overline{CHG}$	10 mA
Operating free-air temperature range		–40°C to 85°C
Junction temperature, T_J		–40°C to 125°C
Storage temperature, T_{STG}		–65°C to 150°C
Lead temperature (soldering, 10 s)		300°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		bq2416x		UNITS
		49 PINS (YFF)	24 PINS (RGE)	
θ_{JA}	Junction-to-ambient thermal resistance	49.8	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	30.5	
θ_{JB}	Junction-to-board thermal resistance	1.1	3.3	
ψ_{JT}	Junction-to-top characterization parameter	1.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter	6.6	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.2	18(1)	V
	IN operating voltage range	4.2	10	
V_{USB}	USB voltage range	4.2	18(1)	V
	USB operating range	4.2	6	
I_{IN}	Input current, IN input		2.5	A
I_{USB}	Input current USB input		1.5	A
I_{SYS}	Ouput current from SW, DC		3	A
I_{BAT}	Charging		2.5	A
	Discharging, using internal battery FET		2.5	A
T_J	Operating junction temperature range	0	125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

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ELECTRICAL CHARACTERISTICS

Circuit of Figure 1, V_{SUPPLY} = V_{USB} or V_{IN} (whichever is supplying the IC), V_{UVLO} < V_{SUPPLY} < V_{OVP} and V_{SUPPLY} > V_{BAT}+V_{SLP}, T_J = 0°C–125°C and T_J = 25ºC for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{SUPPLY}	Supply current for control (V_{IN} or V_{USB})	V_{UVLO} < V_{SUPPLY} < V_{OVP} and V_{SUPPLY} > V_{BAT}+V_{SLP}, PWM switching			15		mA
		V_{UVLO} < V_{SUPPLY} < V_{OVP} and V_{SUPPLY} > V_{BAT}+V_{SLP}, PWM NOT switching				5	
		0°C < T_J < 85°C, High-Z Mode				175	µA
$I_{BATLEAK}$	Leakage current from BAT to the Supply	0°C < T_J < 85°C, V_{BAT} = 4.2 V, V_{USB} = V_{IN} = 0 V				5	µA
I_{BAT_HIZ}	Battery discharge current in high impedance mode, (BAT, SW, SYS)	0°C < T_J < 85°C, V_{BAT} = 4.2 V, V_{SUPPLY} = 0 V or 5V IUSB1=IUSB2=IUSB3=1, High-Z mode				55	µA
POWER PATH MANAGEMENT							
$V_{SYS(REG)}$	System regulation voltage	V_{BAT} < V_{MINSYS}		3.6	3.7	3.82	V
$V_{SYSREGFETOFF}$		Battery FET turned off, Charge disable or termination		4.26	4.33	4.37	
V_{MINSYS}	Minimum system regulation voltage	V_{BAT} < V_{MINSYS}, Input current limit or V_{INDPM} active		3.4	3.5	3.62	V
V_{BSUP1}	Enter supplement mode threshold	V_{BAT} > 2.5 V			V_{BAT} – 40mV		V
V_{BSUP2}	Exit supplement mode threshold	V_{BAT} > 2.5 V			V_{BAT} – 10mV		V
$I_{LIM(Discharge)}$	Current limit, discharge or supplement mode	Current monitored in internal FET only.			7		A
$t_{DGL(SC1)}$	Deglitch time, OUT short circuit during discharge or supplement mode	Measured from(V_{BAT} -V_{SYS}) = 300mV to V_{BGATE} = (V_{BAT} - 600mV)			250		µs
$t_{REC(SC1)}$	Recovery time, OUT short circuit during discharge or supplement mode				60		ms
	Battery range for BGATE operation			2.5		4.5	V
BATTERY CHARGER							
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2 V	YFF pkg		37	57	mΩ
			RGE pkg		50	70	
V_{BATREG}	Battery regulation voltage	T_A = 25°C, $\overline{CE1}$ = $\overline{CE2}$ = 0		4.179	4.2	4.221	V
		$\overline{CE1}$=$\overline{CE2}$ = 0 or V_{WARM} < V_{TS} < V_{COOL}		4.160	4.2	4.24	
		T_A = 25°C, $\overline{CE1}$=1, $\overline{CE2}$=0		4.04	4.06	4.08	
		$\overline{CE1}$=1, $\overline{CE2}$=0 or V_{HOT} < V_{TS} < V_{WARM}		4.02	4.06	4.1	
I_{CHARGE}	Charge current programmable range	$I_{CHARGE} = \frac{K_{ISET}}{R_{ISET}}$		550		2500	mA
K_{ISET}	Programmable fast charge current factor	T_A = 0°C to 125°C, $\overline{CE1}$=$\overline{CE2}$=0 or V_{WARM} < V_{TS} < V_{COOL}		450	490	540	AΩ
		T_A = 0°C to 125°C, $\overline{CE1}$ = 1, $\overline{CE2}$ = 0 or V_{COLD} < V_{TS} < V_{COOL}		225	245	270	
$V_{BATSHRT}$	Battery short threshold	V_{BAT} Rising		2.9	3.0	3.1	V
$V_{BATSHRThys}$	Battery short threshold hysteresis	V_{BAT} Falling			100		mV
$I_{BATSHRT}$	Battery short current	V_{BAT} < $V_{BATSHRT}$			50.0		mA
$t_{DGL(BATSHRT)}$	Deglitch time for battery short to fastcharge transition			32			ms
I_{TERM}	Termination charge current	I_{CHARGE} ≤ 1 A		7	10	11.5	%I_{CHARGE}
		I_{CHARGE} >1 A		8	10	11	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over- drive, t_{RISE}, t_{FALL} = 100 ns			32		ms
V_{RCH}	Recharge threshold voltage	Below VBATREG			120		mV
$t_{DGL(RCH)}$	Deglitch time	VBAT falling below VRCH, tFALL=100ns			32		ms
I_{DETECT}	Battery detection current before charge done (sink current)				2.5		mA
t_{DETECT}	Battery detection time				250		ms
INPUT PROTECTION							
I_{IN_USB}	Input current limiting threshold (USB input only)	USB charge mode, V_{USB} = 5V, Current pulled from PMIDU	IINUSB=USB100	90	95	100	mA
			IINUSB=USB500	450	475	500	
			IINUSB=USB150	135	142.5	150	
			IINUSB=USB900	800	850	900	
			IINUSB=USB800	700	750	800	
			IINUSB=1.5A	1250	1400	1500	

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ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 1, $V_{SUPPLY} = V_{USB}$ or V_{IN} (whichever is supplying the IC), $V_{UVLO} < V_{SUPPLY} < V_{OVP}$ and $V_{SUPPLY} > V_{BAT}+V_{SLP}$, T_J = 0°C–125°C and T_J = 25ºC for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{INLIM}	Maximum input current limit programmable range for IN input	$I_{INLIM} = \frac{K_{ILIM}}{R_{ILIM}}$	1000		2500	mA
K_{ILIM}	Maximum input current factor for IN input		238	251	264	AΩ
$V_{IN_DPM_IN}$	VIN_DPM threshold programmable range for IN Input		4.2		10	V
	VDPM threshold		1.18	1.2	1.22	V
$V_{IN_DPM_USB}$	VIN_DPM threshold for USB Input	USB100, USB150	4.175	4.28	4.36	V
		USB500, USB800, USB900, 1.5A current limit selected	4.35	4.44	4.52	
V_{DRV}	Internal bias regulator voltage	V_{SUPPLY} > 5.45V	5	5.2	5.45	V
I_{DRV}	DRV Output current		10			mA
V_{DO_DRV}	DRV Dropout voltage ($V_{SUPPLY} - V_{DRV}$)	I_{SUPPLY} = 1 A, V_{SUPPLY} = 5 V, I_{DRV} = 10 mA			450	mV
V_{UVLO}	Under-voltage lockout threshold voltage	V_{IN} or V_{USB} rising, 150mV Hysteresis	3.6	3.8	4.0	V
V_{SLP}	Sleep-mode entry threshold, VSUPPLY-VBAT	2.0 V ≤ V_{BAT} ≤ V_{OREG}, V_{IN} falling	0	40	100	mV
V_{SLP_EXIT}	Sleep-mode exit hysteresis	2.0 V ≤ V_{BAT} ≤ V_{OREG}	40	100	175	mV
	Deglitch time for supply rising above $V_{SLP}+V_{SLP_EXIT}$	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns		30		ms
V_{OVP}	Input supply OVP threshold voltage	USB, V_{USB} Rising	6.3	6.5	6.7	V
		IN, V_{IN} Rising	10.3	10.5	10.7	
$V_{OVP(HYS)}$	V_{OVP} hysteresis	Supply falling from V_{OVP}		100		mV
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge	1.025 × V_{BATREG}	1.05 × V_{BATREG}	1.075 × V_{BATREG}	V
$V_{BATUVLO}$	Battery UVLO threshold voltage			2.5		V
I_{LIMIT}	Cycle by Cycle current limit		4.1	4.9	5.6	A
$T_{SHUTDWN}$	Thermal shutdown	10C Hysteresis		165		C
T_{REG}	Thermal regulation threshold			120		C
	Safety Timer		324	360	396	min
IUSB_, $\overline{CE}$_, $\overline{PG}$, $\overline{CHG}$						
V_{IH}	Input high threshold		1.3			V
V_{IL}	Input low threshold				0.4	V
I_{IH}	High-level leakage current	$V_{\overline{CHG}} = V_{\overline{PG}} = 5V$			1	µA
V_{OL}	Low-level output saturation voltage	I_O = 10 mA, sink current			0.4	V
PWM CONVERTER						
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 500 mA, Measured from V_{USB} to PMIDU	95		175	mΩ
		I_{IN_LIMIT} = 500 mA, Measured from V_{IN} to PMIDI	45		80	
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMIDU to SW	100		175	mΩ
		Measured from PMIDI to SW	65		110	
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND	65		115	
f_{OSC}	Oscillator frequency		1.35	1.50	1.65	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0			
BATTERY-PACK NTC MONITOR (bq24166, bq24167)						
V_{HOT}	High temperature threshold	V_{TS} falling	29.7	30	30.5	%V_{DRV}
$V_{HYS(HOT)}$	Hysteresis on high threshold	V_{TS} rising		1		
V_{WARM}	Warm temperature threshold	V_{TS} falling, bq24167 only	37.9	38.3	39.6	%V_{DRV}
$V_{HYS(WARM)}$	Hysteresis on high threshold	V_{TS} rising, bq24167 only		1		
V_{COOL}	Cool temperature threshold	V_{TS} rising, bq24167 only	56.0	56.5	56.9	%V_{DRV}
$V_{HYS(COOL)}$	Hysteresis on low threshold	V_{TS} falling, bq24167 only		1		
V_{COLD}	Low temperature threshold	V_{TS} rising	59.5	60	60.4	%V_{DRV}
$V_{HYS(COLD)}$	Hysteresis on low threshold	V_{TS} falling		1		
T_{SOFF}	TS Disable threshold	V_{TS} rising, 2%V_{DRV} Hysteresis	70		73	%V_{DRV}
$t_{DGL(TS)}$	Deglitch time on TS change			50		ms

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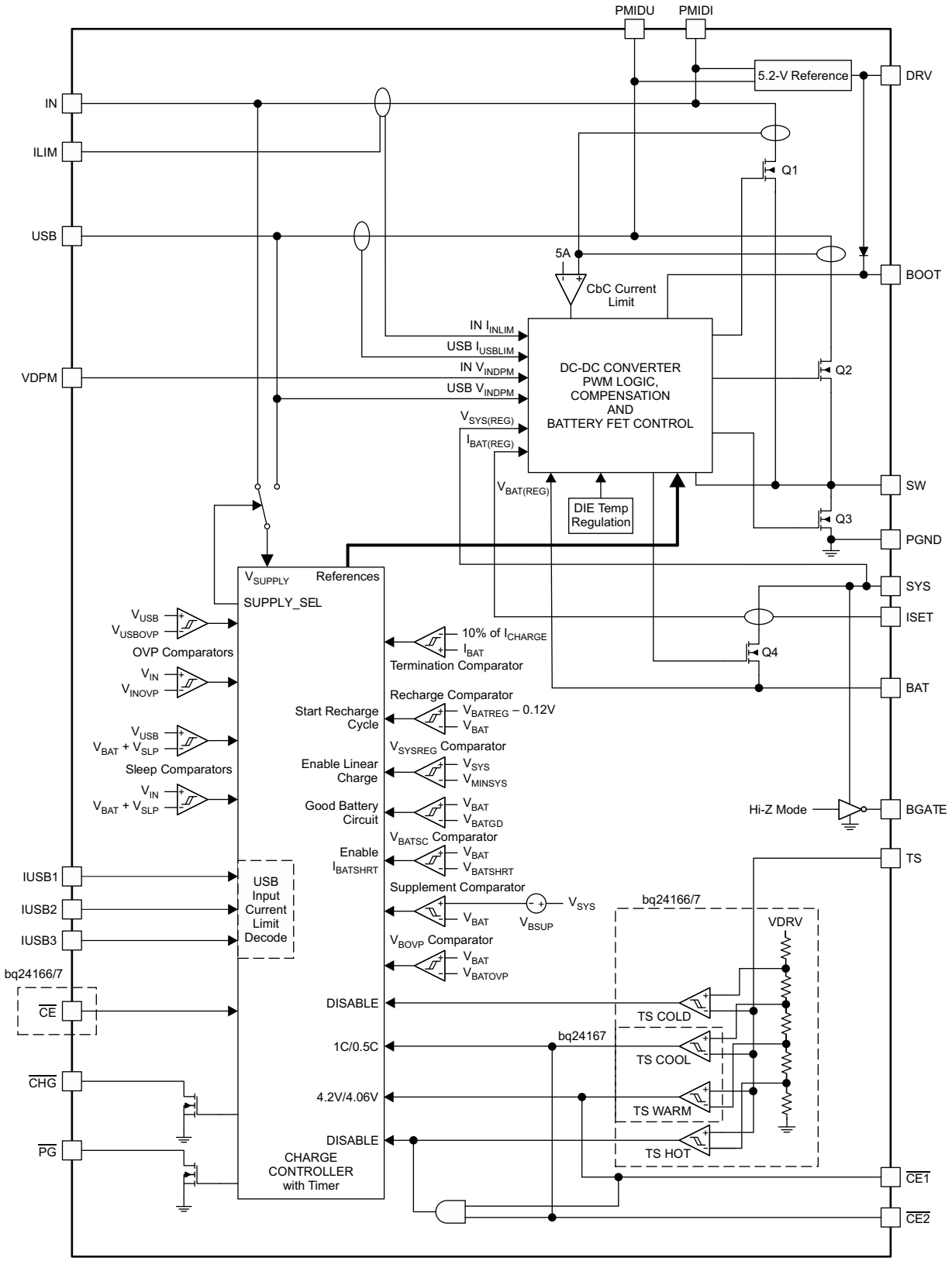
BLOCK DIAGRAM



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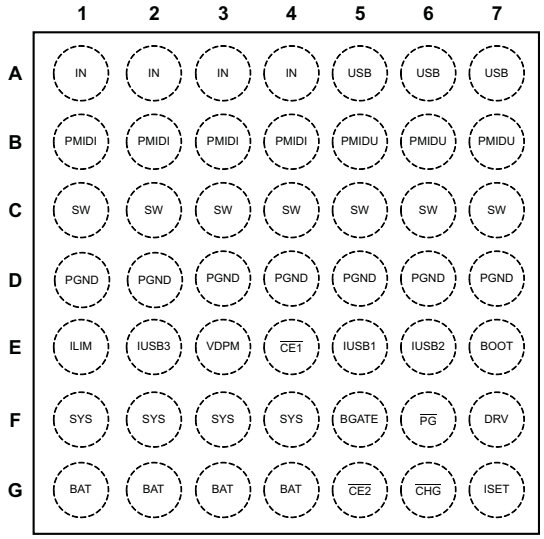
PIN CONFIGURATION

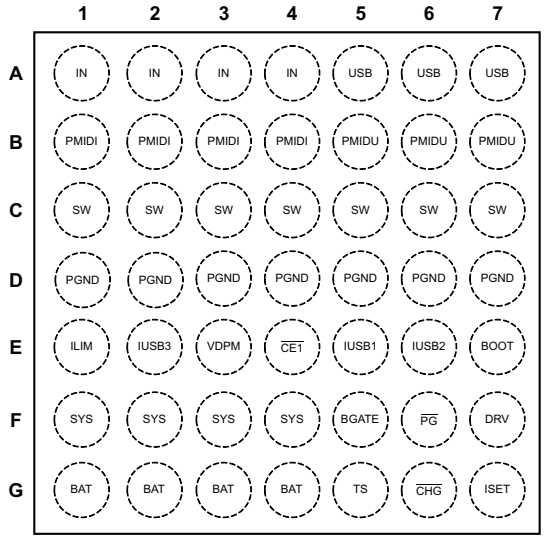
49-Ball 2.8mm x 2.8mm WCSP

bq24165
YFF Package
(Top View)



Pin Configurations are Subject to Change

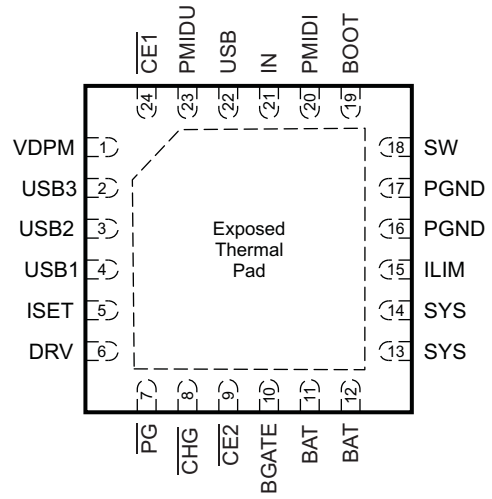
bq24166/7
YFF Package
(Top View)



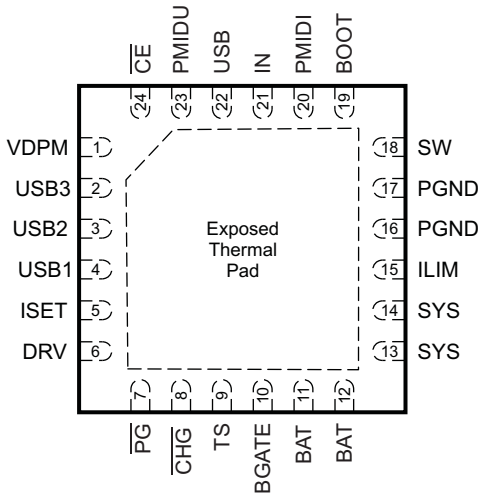
Pin Configurations are Subject to Change

24-Pin 4mm x 4mm QFN

bq24165
RGE Package
(Top View)



bq24166/7
RGE Package
(Top View)



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PIN FUNCTIONS

PIN NAME	PIN NUMBER				I/O	DESCRIPTION
	bq24165		bq24166/7			
	YFF	RGE	YFF	RGE		
IN	A1–A4	21	A1–A4	21	I	Input power supply. IN is connected to the external DC supply (AC adapter or alternate power source). Bypass IN to PGND with at least a 1µF ceramic capacitor.
USB	A5–A7	22	A5–A7	22	I	USB Input Power Supply. USB is connected to the external DC supply (AC adapter or USB port). Bypass USB to PGND with at least a 1µF ceramic capacitor.
PMIDI	B1–B4	20	B1–B4	20	O	Reverse Blocking MOSFET and High Side MOSFET Connection Point for High Power Input. Bypass PMIDI to GND with at least a 4.7µF ceramic capacitor. Use caution when connecting an external load to PMIDI. The PMIDI output is not current limited. Any short on PMIDI will result in damage to the IC.
PMIDU	B5–B7	23	B5–B7	23	O	Reverse Blocking MOSFET and High Side MOSFET Connection Point for USB Input. Bypass PMIDU to GND with at least a 4.7µF ceramic capacitor. Use caution when connecting an external load to PMIDU. The PMIDU output is not current limited. Any short on PMIDU will result in damage to the IC.
SW	C1–C7	18	C1–C7	18	O	Inductor Connection. Connect to the switched side of the external inductor.
PGND	D1–D7	16, 17	D1–D7	16, 17	–	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
ILIM	E1	15	E1	15	I	IN Input Current Limit Programming Input. Connect a resistor from ILIM to GND to program the input current limit for IN. The current limit is programmable from 1A to 2.5A. ILIM has no effect on the USB input.
VDPM	E3	1	E3	1	I	Input DPM Programming Input. Connect a resistor divider from IN to GND with VDPM connected to the center tap to program the Input Voltage based Dynamic Power Management (V_{IN}-DPM) threshold. The input current is reduced to maintain the supply voltage at V_{IN}-DPM. See the *Input Voltage based Dynamic Power Management* section for a detailed explanation.
$\overline{CE}$	–	–	E4	24	I	Charge Enable Input. $\overline{CE}$ is used to disable or enable the charge process. A low logic level (0) enables charging and a high logic level (1) disables charging. When charging is disabled, the SYS output remains in regulation, but BAT is disconnected from SYS. Supplement mode is still available if the system load demands cannot be met by the supply. BGATE is high impedance when $\overline{CE}$ is high.
IUSB1	E5	4	E5	4	I	USB Input Current Limit Programming Inputs. USB1, USB2 and USB3 program the input current limit for the USB input. USB2.0 and USB3.0 current limits are available for easy implementation of these standards. Table 1 shows the settings for these inputs. USB1, USB2 and USB3 have no effect on the IN input.
IUSB2	E6	3	E6	3	I	
IUSB3	E2	2	E2	2	I	
$\overline{CE1}$	E4	24	–	–	I	JEITA Compliance Inputs. $\overline{CE1}$ and $\overline{CE2}$are used to change battery regulation and charge current regulation to comply with the JEITA charging standard. The charge voltage can be reduced by 140mV or the charge current may be reduced to half the programmed value. See Table 2 for programming details.
$\overline{CE2}$	G5	9	–	–	I	
BOOT	E7	19	E7	19	I	High Side MOSFET Gate Driver Supply. Connect a 0.01µF ceramic capacitor (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
SYS	F1–F4	13, 14	F1–F4	13, 14	I	System Voltage Sense and Charger FET Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with at least 10µF. 47µF bypass capacitance is recommended for best transient response.
BGATE	F5	10	F5	10	O	External Discharge MOSFET Gate Connection. BGATE drives an external P-Channel MOSFET to provide a very low resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low during high impedance mode and when no input is connected. BGATE is optional. If unused, leave BGATE unconnected.
$\overline{PG}$	F6	7	F6	7	O	Power Good Open Drain Output. $\overline{PG}$ is pulled low when a valid supply is connected to either USB or IN. A valid supply is between V_{BAT}+V_{SLP} and V_{OVP}. If not supply is connected or the supply is out of this range, $\overline{PG}$ is high impedance.

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PIN FUNCTIONS (continued)

PIN NAME	PIN NUMBER				I/O	DESCRIPTION
	bq24165		bq24166/7			
	YFF	RGE	YFF	RGE		
DRV	F7	6	F7	6	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. bypass DRV to PGND with a 1µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{SUPPLY} > V_{UVLO}$ and $V_{SUPPLY} > (V_{BAT} + V_{SLP})$
BAT	G1–G4	11, 12	G1–G4	11, 12	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with at least a 1µF capacitor.
TS	–	–	G5	9	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function in the bq24166 provides 2 thresholds for Hot/ Cold shutoff, while the bq24167 has 2 additional thresholds for JEITA compliance. See the *NTC Monitor* section for more details on operation and selecting the resistor values. Connect TS to DRV to disable the TS function.
$\overline{CHG}$	G6	8	G6	8	O	Charge Status Open Drain Output. $\overline{CHG}$ is pulled low when a charge cycle starts and remains low while charging. $\overline{CHG}$ is high impedance when the charging terminates and when no supply exists. $\overline{CHG}$ does not indicate recharge cycles.
ISET	G7	5	G7	5	I	Charge Current Programming Input. Connect a resistor from ISET to GND to program the fast charge current. The charge current is programmable from 550mA to 2.5A.
Thermal Pad	–	Pad	–	Pad	–	There is an internal electrical connection between the exposed thermal pad and the PGND pin of the device. The thermal pad must be connected to the same potential as the PGND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. PGND pin must be connected to ground at all times.

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TYPICAL APPLICATION CIRCUIT

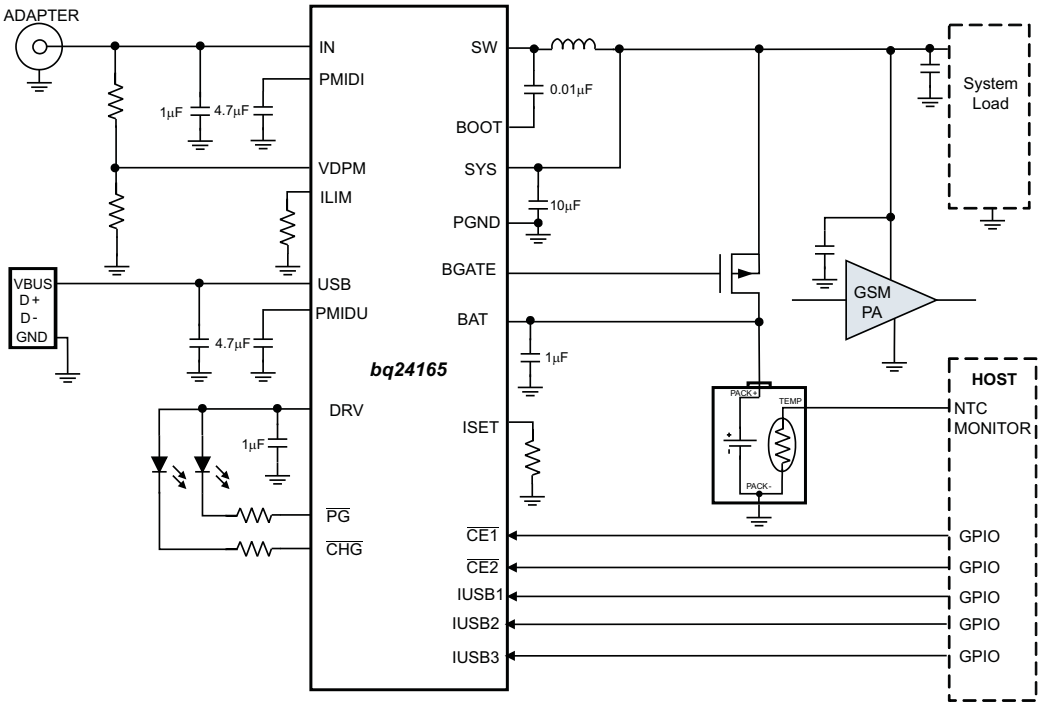

Figure 1. bq24165, Shown with External Discharge FET, PA Connected to System for GSM Call Support with a Deeply Discharged or No Battery

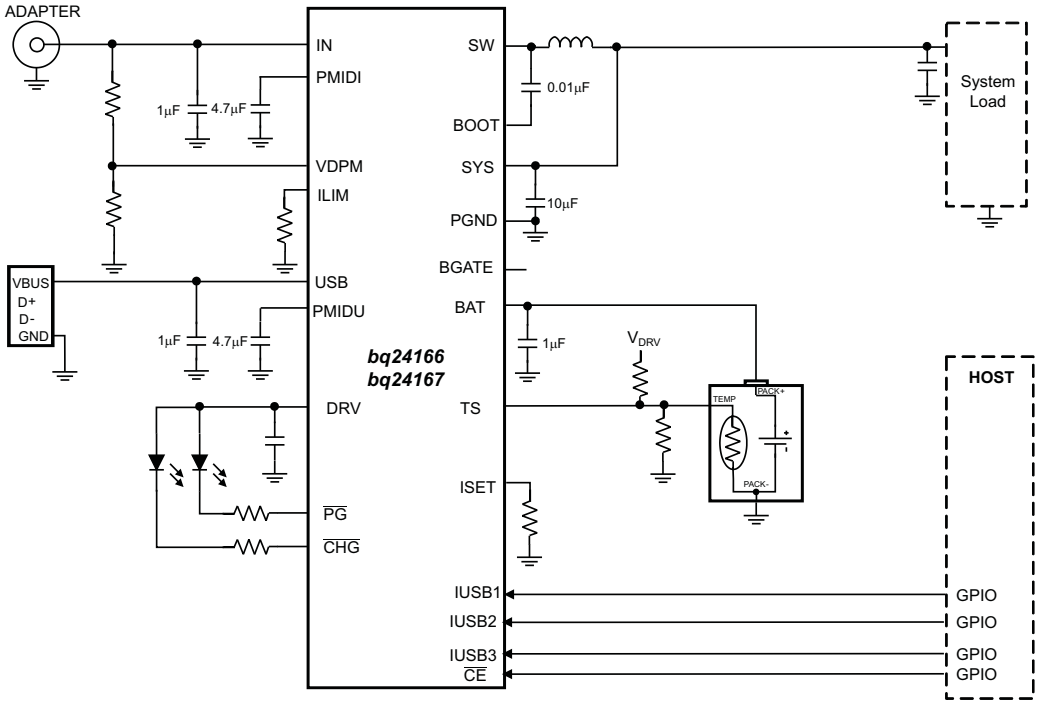

Figure 2. bq24166 and bq24167, Shown with no External Discharge FET, External NTC Monitor

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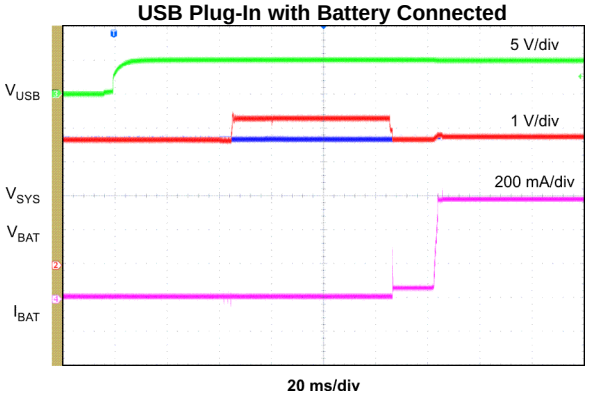
TYPICAL CHARACTERISTICS

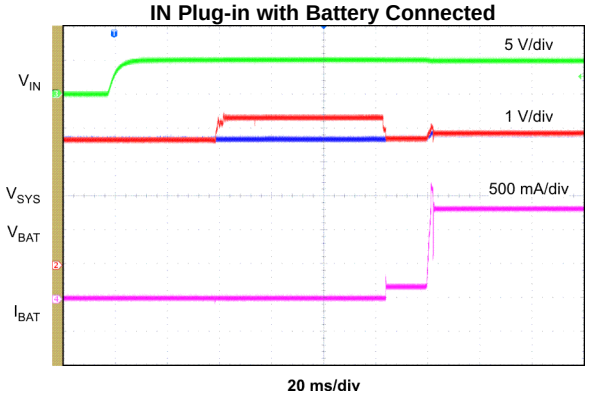
USB Plug-In with Battery Connected



Conditions: USB500, 925mA Charge Setting

Figure 3.

IN Plug-in with Battery Connected



Conditions: 1500mA ILIM, 1300mA Charge Setting

Figure 4.

Adapter Detection USB

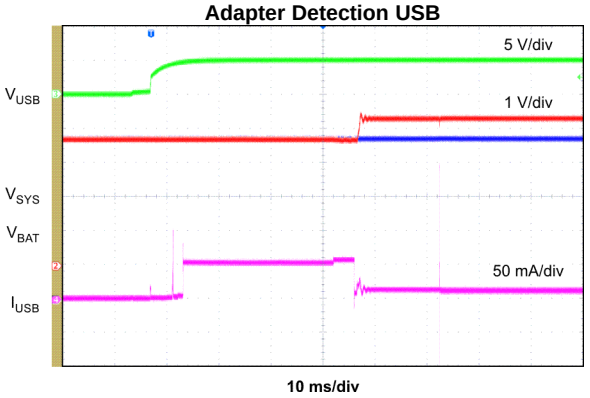
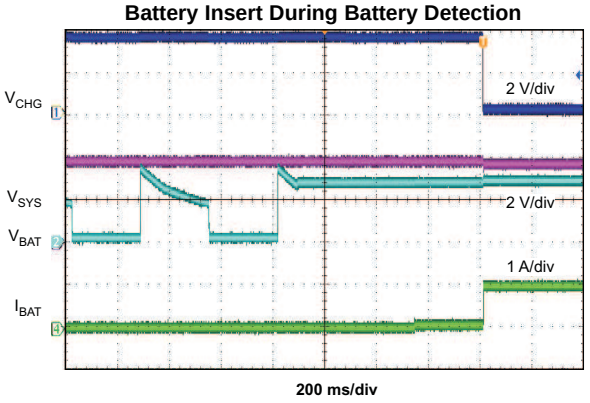


Figure 5.

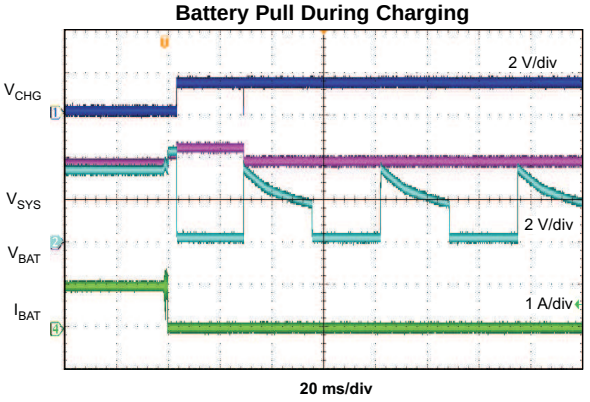
Battery Insert During Battery Detection



Conditions: Termination Enabled

Figure 6.

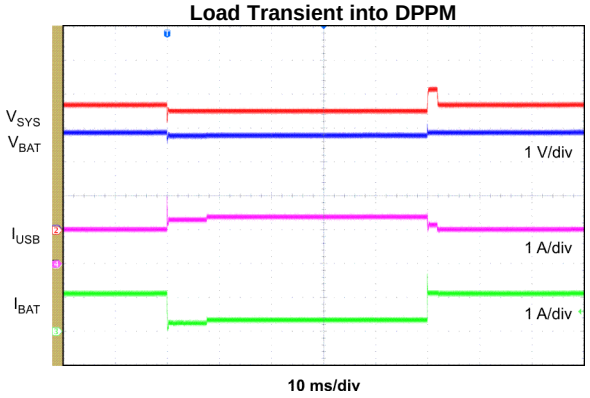
Battery Pull During Charging



Conditions: Termination Enabled

Figure 7.

Load Transient into DPPM



Conditions: MINSYS Operation, USB1500, 200mA-1400mA Load Step on SYS

Figure 8.

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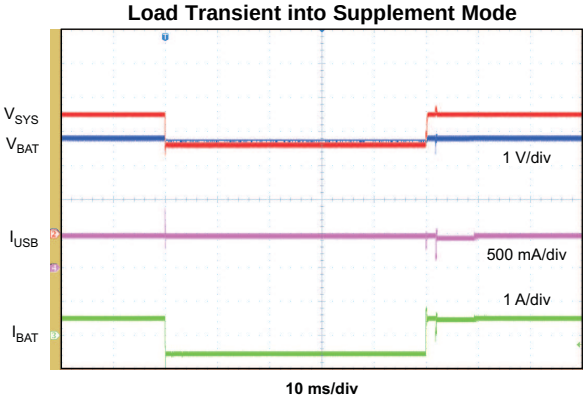
TYPICAL CHARACTERISTICS (continued)



Conditions: MINSYS Operation, USB500, 200mA - 1400mA Load Step on SYS

Figure 9.

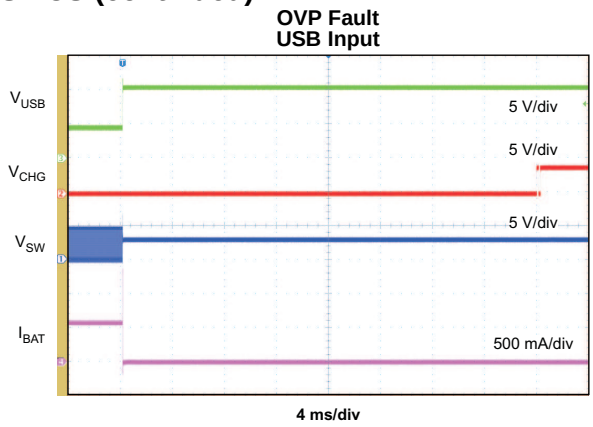
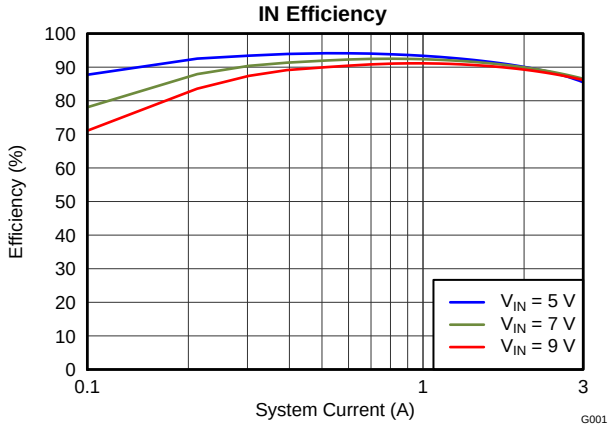
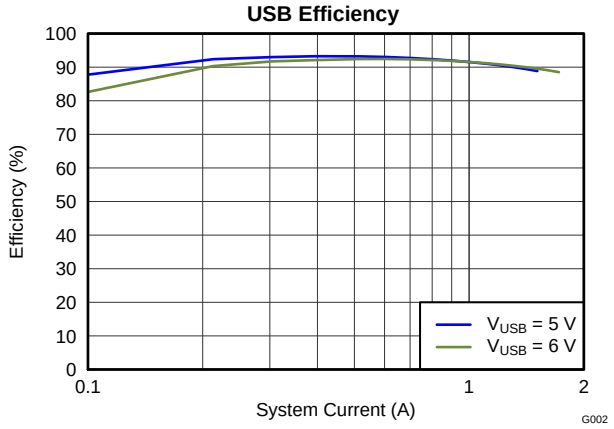


Figure 10.



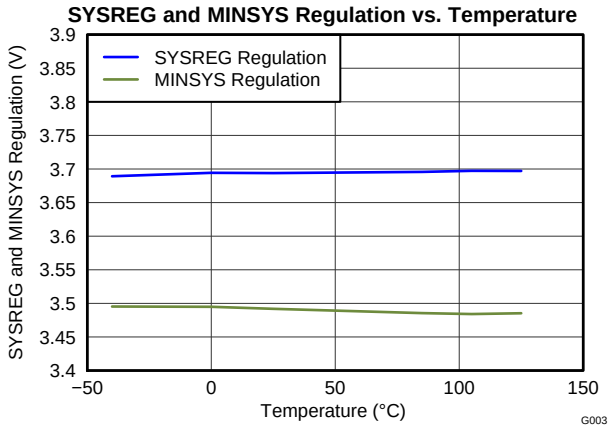
Conditions: Charge Disabled, SYS loaded, V_{BATREG} = 3.6V, IN2500 ILIM

Figure 11.



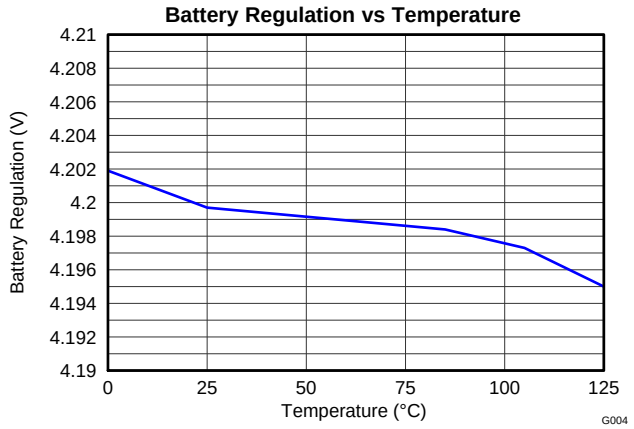
Conditions: Charge Disabled, SYS loaded, V_{BATREG} = 3.6V, USB1500 ILIM

Figure 12.



Conditions: V_{BAT} = 3V

Figure 13.



Conditions: V_{BATREG} = 4.2V, No load, Termination Disabled

Figure 14.

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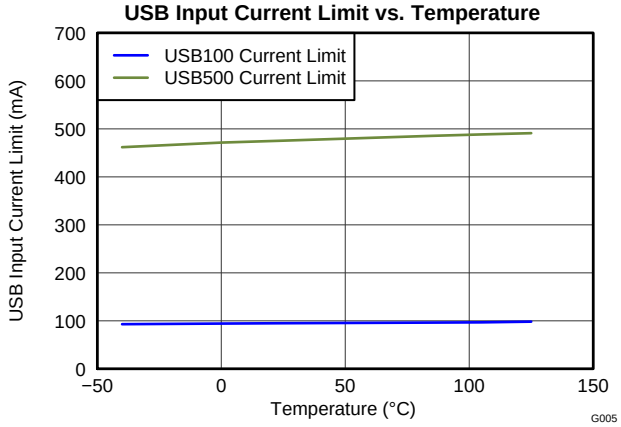
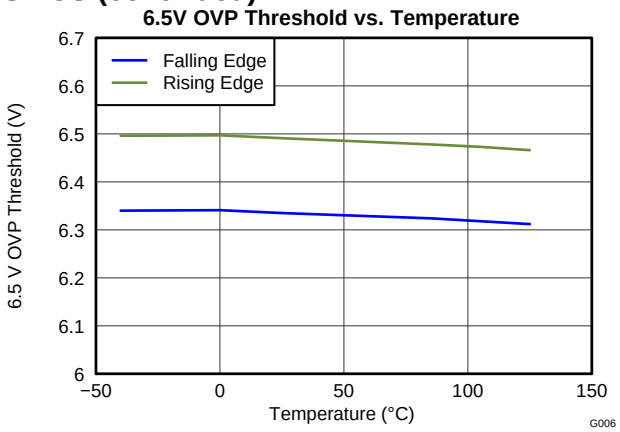
TYPICAL CHARACTERISTICS (continued)



Conditions: USB100 and USB500 current limit, V_{USB} = 5V, V_{BAT} = 3.6V

Figure 15.



Conditions: USB input and IN input (bq24168)

Figure 16.

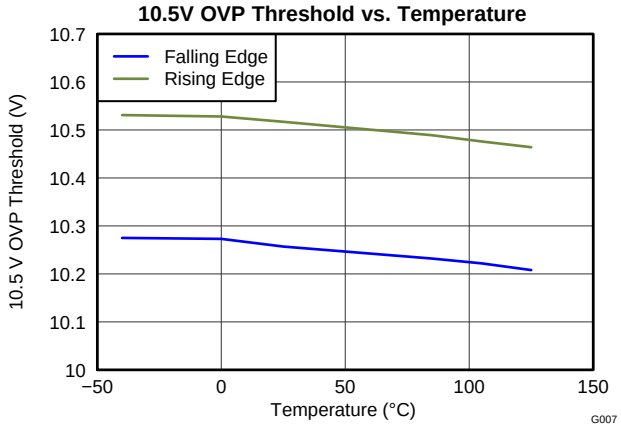
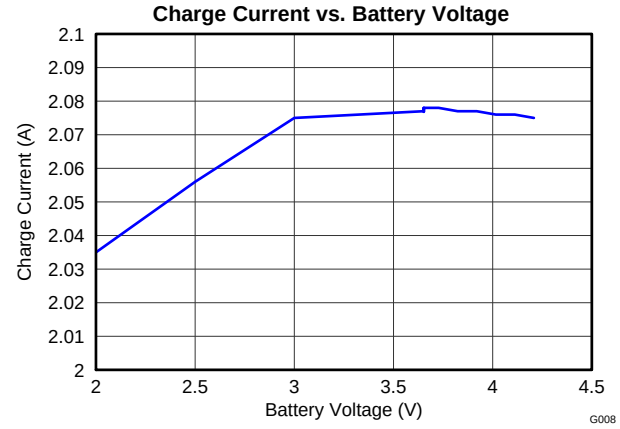


Figure 17.



Conditions: I_{CHARGE} = 2A, V_{IN} = 5V, V_{BATREG} = 4.44V

Figure 18.

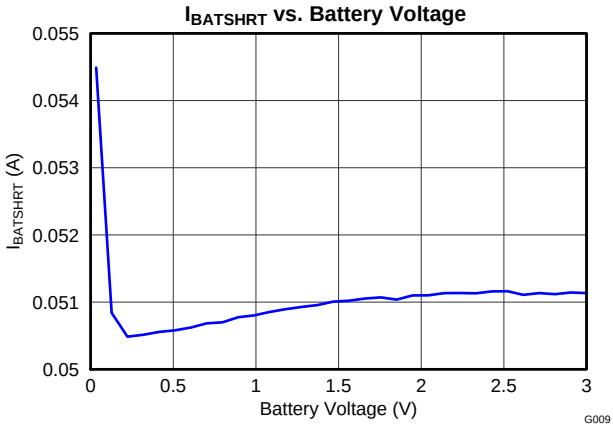


Figure 19.

DETAILED DESCRIPTION

CHARGE MODE OPERATION

Charge Profile

Charging is done through the internal battery MOSFET. When the battery voltage is above 3.5V, the system output (SYS) is connected to the battery to maximize the charging efficiency. There are 6 loops that influence the charge current; constant current loop (CC), constant voltage loop (CV), input current loop, thermal regulation loop, minimum system voltage loop (MINSYS) and input voltage dynamic power management loop (V_{INDPM}). During the charging process, all six loops are enabled and the dominate one takes control. The bq24165/6/7 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. The minimum system output feature regulates the system voltage to a minimum of $V_{SYS(REG)}$, so that startup is enabled even for a missing or deeply discharged battery. Figure 20 shows a typical charge profile including the minimum system output voltage feature.

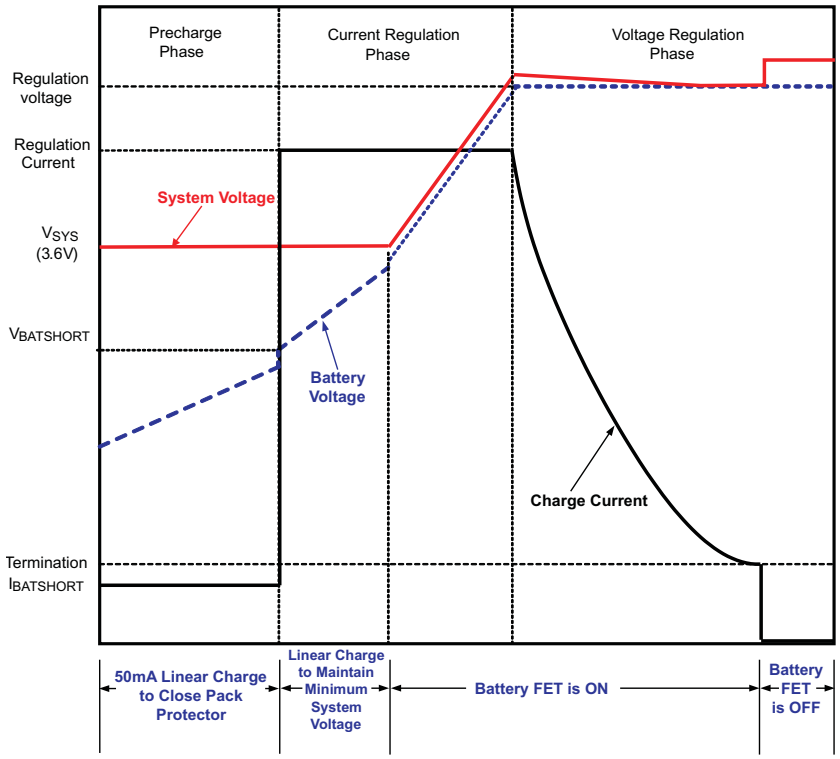


Figure 20. Typical Charging Profile of bq24165/6/7

PWM CONTROLLER IN CHARGE MODE

The bq24165/6/7 provides an integrated, fixed 1.5 MHz frequency voltage-mode converter to power the system and supply the charge current. The voltage loop is internally compensated and provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR.

The bq24165/6/7 input scheme prevents battery discharge when the supply voltages is lower than VBAT and also isolates the two inputs from each other. The high-side N-MOSFET (Q1/Q2) switches to control the power delivered to the output. The DRV LDO supplies the gate drive for the internal MOSFETs. The high side FETs are supplied through a boot strap circuit with external boot-strap capacitor is used to boost up the gate drive voltage for Q1/Q2.

Both inputs are protected by a cycle-by-cycle current limit that is sensed through the internal MOSFETs for Q1 and Q2. The threshold for the current limit is set to a nominal 5-A peak current. The inputs also utilize an input current limit that limits the current from the power source.

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BATTERY CHARGING PROCESS

Assuming a valid input source has already been attached to IN or USB, as soon as a deeply discharged or shorted battery is attached to the BAT pin, the bq24165/6/7 applies a 50mA current to bring the battery voltage up to acceptable charging levels. During this pre-charge time, the battery FET is linearly regulated to maintain the system output regulation at $V_{SYS(REG)}$. Once the battery rises above $V_{BATSHRT}$, the charge current increases to the fastcharge current setting. The SYS voltage is regulated to $V_{SYS(REG)}$ while the battery is linearly charged through the battery FET. Under normal conditions, the time spent in this region is a very short percentage of the total charging time, so if the charge current is reduced, the reduced charge rate does not have a major negative effect on total charge time. If the current limit for the SYS output is reached (limited by the input current limit, or V_{IN}-DPM), the charge current is reduced to provide the system with all the current that is needed. If the charge current is reduced to 0mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode (see the *Dynamic Power Path Management* section for more details).

Once the battery is charged enough to where the system voltage begins to rise above V_{SYSREG} (depends on the charge current setting), the battery FET is turned on fully and the battery is charged with the charge current programmed using the ISET input, I_{CHARGE}. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. The charge current is programmed by connecting a resistor from ISET to GND. The value for R_{ISET} is calculated using Equation 1:

$$R_{ISET} = \frac{K_{ISET}}{I_{CHARGE}} \quad (1)$$

Where I_{CHARGE} is the programmed fast charge current and K_{ISET} is the programming factor found in the Electrical Characteristics table.

The charger's constant current (CC) loop regulates the charge current to I_{CHARGE} until the battery reaches close to the regulation voltage. Once the battery voltage is close to the regulation voltage, V_{BATREG}, the charge current step downs sharply as the constant voltage (CV) loop takes over, the internal battery FET turns on full, tying SYS to BAT and the charger tapers down the charge current as shown in Figure 1. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the BAT and PGND pins.

The bq24165/6/7 monitors the charging current during the voltage regulation phase. If the battery voltage is above the recharge threshold and the charge current has naturally tapered down to and remains below termination threshold, I_{TERM}, without disturbance from events like supplement mode for 32ms, the bq24165/6/7 terminates charge and turns off the battery charging FET. If $V_{SYS} > V_{MINSYS}$ and the charge current has been reduced due to V_{INDPM},the input current loop or thermal protection circuits or USB100mode, the charger disables termination. The system output is regulated to the $V_{BAT(REG)}$ voltage and supports the full current available from the input. Battery supplement mode (see the *Dynamic Power Path Management* section for more details) is still available for SYS load transients. Supplement mode events occurring repeatedly within the 32ms deglitch window will prevent termination and can cause the charger to exit termination.

Charging resumes when one of the following conditions is detected:

1. The battery voltage falls below the $V_{BAT(REG)}$-V_{RCH} threshold
2. V_{SUPPLY} Power-on reset (POR)
3. $\overline{CE1}$ $\overline{CE2}$ toggle or $\overline{CE}$ toggle
4. Toggle Hi-Impedance mode (using IUSB_)

A new charge cycle is initiated only in the event of V_{SUPPLY} POR or the battery being removed and replaced. If the battery voltage, V_{BAT}, is ever greater than V_{BATREG} (for example, when an almost fully charged battery enters the JEITA WARM state per the TS pin or $\overline{CE1}$ and $\overline{CE2}$ are configured to reduce V_{BATREG}) but less than V_{BOVP}, the reverse boost protection circuitry may activate as explained later in this datasheet. If the battery is ever above V_{BOVP}, the buck converter turns off and the internal battery FET is turned on. This prevents further overcharging the battery and allows the battery to discharge to safe operating levels.

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BATTERY DETECTION

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from VBAT for t_{DETECT} to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of t_{DETECT}, a battery is determined to present and the IC enters “Charge Done”. If VBAT falls below V_{DETECT}, battery detection continues. The next cycle of battery detection, the bq2416x turns on $I_{BATSHORT}$ for t_{DETECT}. If VBAT rises to V_{DETECT}, the current source is turned offand after t_{DETECT}, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Figures 6 and 7 show the oscillation on VBAT prior to battery insertion and after battery removal. Battery detection is disabled when termination is disabled.

DYNAMIC POWER PATH MANAGEMENT

The bq24165/6/7 features a SYS output that powers the external system load connected to the battery. This output is active whenever a source is connected to IN, USB or BAT. The following sections discuss the behavior of SYS with a source connected to the supply (IN or USB) or a battery source only.

INPUT SOURCE CONNECTED

When a source is connected to IN or USB, and the bq24165/6/7 is enabled, the buck converter starts up. If charging is enabled using $\overline{CE1}$ and $\overline{CE2}$(bq24165) or $\overline{CE}$ (bq24166/7), the charge cycle is initiated. When V_{BAT} > 3.5V, the internal battery FET is turned on and the SYS output is connected to V_{BAT}. If the SYS voltage falls to $V_{SYS(REG)}$, it is regulated to that point to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET is linearly regulated to regulate the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power path management (DPPM) circuitry of the bq24165/6/7 monitors the SYS voltage continuously. If V_{SYS} falls to V_{MINSYS}, the DPPM circuit adjusts charge current to maintain the load on SYS while preventing the system voltage from crashing. If the charge current is reduced to zero and the load increases further, the bq24165/6/7 enters battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load. When the charge current is reduced by the DPPM regulation loop, the safety timer runs at half speed, so that it is twice a long. This prevents false safety timer faults. See the *Safety Timer* section for more details.

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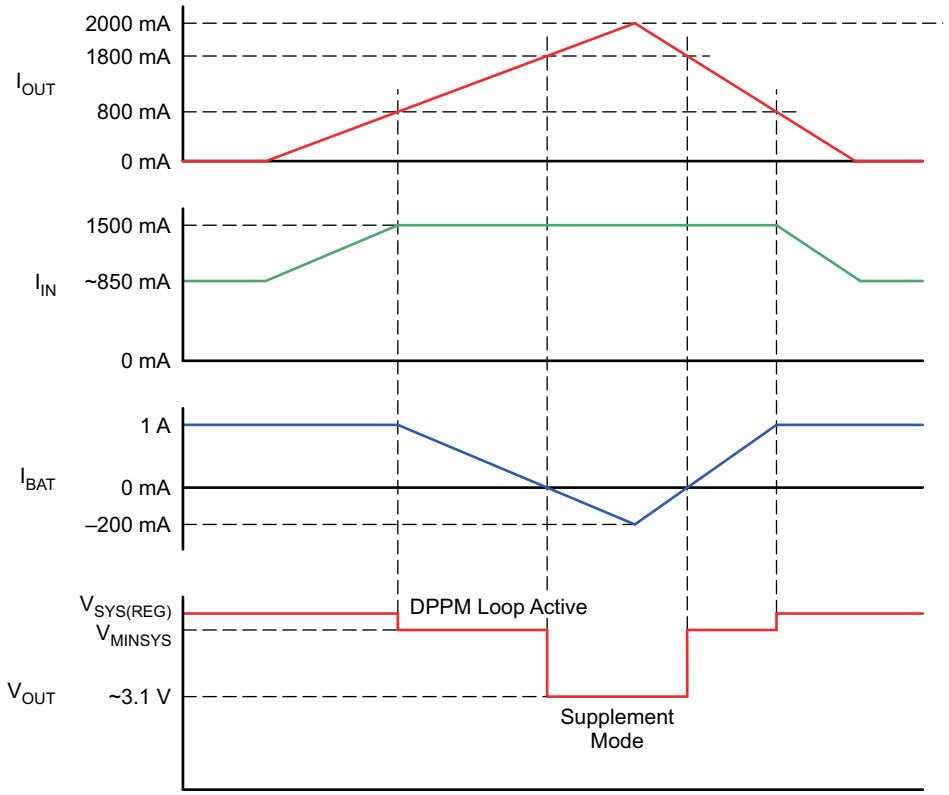

Figure 21. Example DPPM Response (V_{Supply} = 5 V, V_{BAT} = 3.1V, 1.5A Input current limit)

If the $V_{BAT(REG)}$ threshold is ever less than the battery voltage, the battery FET is turned off and the SYS output is regulated to $V_{SYSREG(FETOFF)}$. If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels.

The input current limit for the USB input is set by the IUSB1, IUSB2, and IUSB3 inputs. The bq24165/6/7 incorporates all of the necessary input current limits to support USB2.0 and USB3.0 standards as well as 1.5A to support wall adapters. Driving IUSB1, IUSB2, and IUSB3 all high places the bq24165/6/7 in High Impedance mode where the buck converter is shutdown regardless if an input is connected to USB or IN. Table 1 shows the configuration for IUSB1 – IUSB3. When USB100 mode is selected, termination is disabled.

Table 1. USB1, USB2 and USB3 Input Table

IUSB3	IUSB2	IUSB1	Input Current Limit	V_{INDPM} Threshold
0	0	0	100 mA	4.28 V
0	0	1	500 mA	4.44 V
0	1	0	1.5 A	4.44 V
0	1	1	High Impedance Mode	None
1	0	0	150 mA	4.28 V
1	0	1	900 mA	4.44 V
1	1	0	800 mA	4.44 V
1	1	1	High Impedance Mode	None

The input current limit for IN is programmable using the ILIM input. Connect a resistor from ILIM to GND to set the maximum input current limit. The programmable range for the IN input current limit is 1000mA to 2.5A. R_{ILIM} is calculated using Equation 2:

$$R_{ILIM} = \frac{K_{ILIM}}{I_{IN_LIM}} \quad (2)$$

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Where I_{IN_LIM} is the programmed input current limit and K_{ILIM} is the programming factor found in the Electrical Characteristics table.

The bq24165/6/7 manages the dual input supply paths as well. The IN input has precedence when valid supplies are connected to both inputs. The two inputs are always isolated from one another. The bq24165/6/7 always seeks to charge from a valid source. For example, if a valid source is connected to USB and a source is connected to IN that is greater than the OVP threshold, the USB source is used to charge the battery. In this case, both the USB source and the battery would be isolated from the OVP source connected to the IN input.

BATTERY ONLY CONNECTED

When the battery is connected with no input source, the internal battery FET is turned on similar to supplement mode. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time. After the deglitch time, the battery FET is turned on in order to determine if the short has been removed. If not, the FET turns off and the process repeats until the short is removed.

EXTERNAL BATTERY DISCHARGE FET (BGATE)

The bq24165/6/7 contains a MOSFET driver to drive an external P-Channel MOSFET between the battery and the system output. This external FET provides a low impedance path to supply the system from the battery. Connect BGATE to the gate of the external discharge MOSFET. BGATE is on under the following conditions:

1. No valid input supply connected.
2. IUSB1=IUSB2=IUSB3=high (High Impedance Mode)

This FET is optional and runs in parallel with the internal charge FET during discharge. Note that this FET is not protected by the short circuit current limit.

SAFETY TIMER

At the beginning of charging process, the bq24165/6/7 starts the 6 hour safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, the charge cycle is terminated and the battery FET is turned off. To clear the safety timer fault, charging must be resumed by using $\overline{CE1}$ and $\overline{CE2}$ (bq24165) or $\overline{CE}$(bq24166/7) or High Impedance mode or a new charge cycle started by V_{SUPPLY} POR or battery remove and replace.

During the fast charge (CC) phase, several events increase the timer duration by 2X.

1. The system load current reduces the available charging current.
2. The input current needed for the fast charge current is limited by the input current loop.
3. The input current is reduced because the V_{INDPM} loop is preventing the supply from crashing.
4. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$.
5. The CEx bits are reducing I_{CHARGE} or VBAT.
6. The battery voltage is less than $V_{BATSHORT}$.
7. The battery has entered the JEITA WARM or COLD state via the TS pin (bq24166/6) or $\overline{CE1}$/$\overline{CE2}$ (bq24165)configuration.

During these events, the timer is slowed by half to extend the timer and prevent any false timer faults. Starting a new charge cycle by VSUPPLY POR or removing/replacing the battery or resuming a charge by toggling the $\overline{CE1}$/$\overline{CE2}$(bq24165) or $\overline{CE}$(bq24166/7) pins, resets the safety timer. Additionally, thermal shutdown events cause the safety timer to reset.

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LDO OUTPUT (DRV)

The bq24165/6/7 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.45V so it is ideal to protect voltage sensitive USB circuits. The LDO is on whenever a supply is connected to the IN or USB inputs of the bq24165/166. The DRV is disabled under the following conditions:

1. V_{SUPPLY} < UVLO
2. V_{SUPPLY} - V_{BAT}< V_{SLP}
3. Thermal Shutdown

CHARGE PARAMETER SELECTOR INPUTS ($\overline{CE1}$, $\overline{CE2}$, bq24165)

The $\overline{CE1}$ and $\overline{CE2}$ inputs allow the user to easily implement the JEITA standard for systems where the battery pack temperature is monitored by the host. JEITA requires that several temperatures be monitored and the maximum charge voltage or charge current be modified based on the battery voltage. A graphical representation of the JEITA specification is shown in Figure 22.

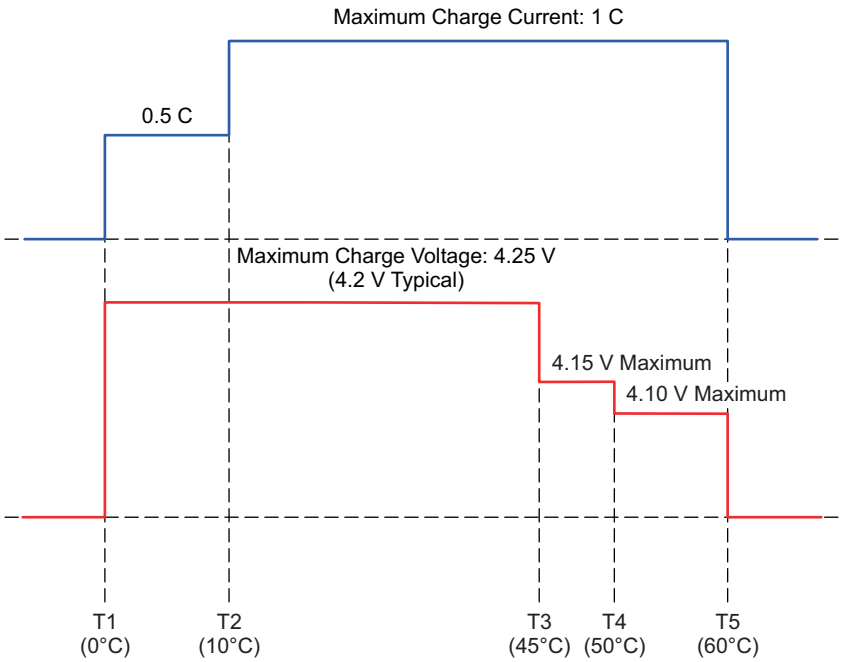

Figure 22. Charge Current During TS Conditions in Default Mode

In many systems, the battery temperature is monitored by the host and the information is used for several different operations. For these systems, the bq24165 method is ideal because it does not require the NTC in the battery to be shared amongst several different ICs. Instead, the $\overline{CE1}$ and $\overline{CE2}$ pins are driven by host GPIOs to reduce the charging current or charge voltage as required. This allows the host to decide which temperatures to change the charging profile and gives the ultimate flexibility to the user. Additionally, $\overline{CE1}$ and $\overline{CE2}$ are used to disable charging while not interfering with the main buck converter operation. The configuration table for $\overline{CE1}$ and $\overline{CE2}$ is shown in Table 2.

Table 2. $\overline{CE1}$, $\overline{CE2}$ Input Table

$\overline{CE1}$	$\overline{CE2}$	FUNCTION
0	0	Normal Charging
0	1	Charge current reduced by half
1	0	$V_{BAT(REG)}$ reduced to 4.06 V
1	1	Charging Suspended

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EXTERNAL NTC MONITORING (TS, bq24166/7)

The bq24166 and bq24167 provide a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. For the bq24166, two temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD} and V_{HOT} thresholds. Charging is suspended and timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$.

To satisfy the JEITA requirements, the bq24167 monitors four temperature thresholds; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < TNTC < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds. As with the bq24166, charging is suspended and timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{HOT} < V_{TS} < V_{WARM}$, the battery regulation voltage is reduced by 140mV from the programmed regulation threshold. When $V_{COOL} < V_{TS} < V_{COLD}$, the charging current is reduced to half of the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 24. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (3)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (4)$$

Where:

$V_{COLD} = 0.60 \times V_{DRV}$
$V_{HOT} = 0.30 \times V_{DRV}$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

For the bq24167, the WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using the following equations:

$$RCOOL = \frac{RLO \times 0.564 \times RHI}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (5)$$

$$RWARM = \frac{RLO \times 0.383 \times RHI}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (6)$$

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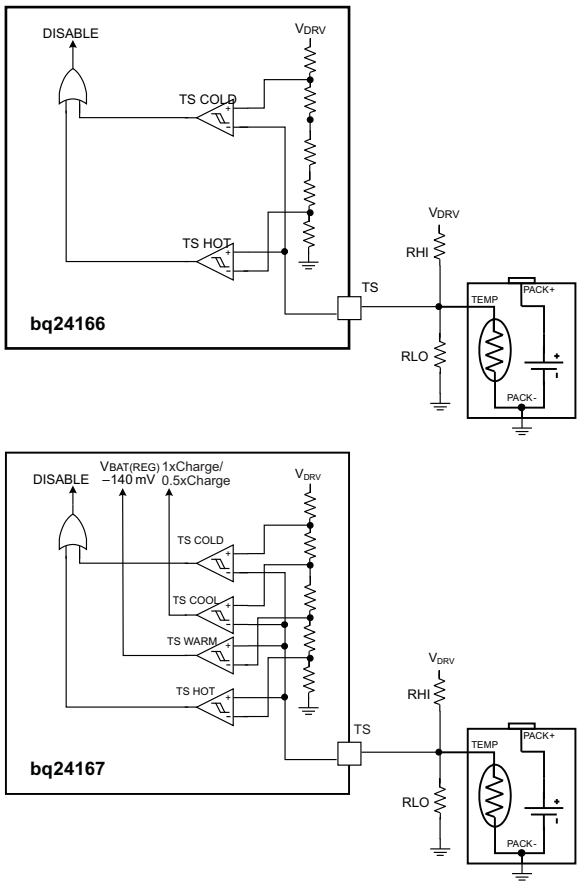

Figure 23. TS Circuits

THERMAL REGULATION AND PROTECTION

During the charging process, to prevent the IC from overheating, bq24165/6/7 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{CF}. The charge current is reduced to zero when the junction temperature increases about 10°C above T_{CF}. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the bq24165/6/7 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24165/6/7 suspends charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, and the timer is reset. The charging cycle resets when T_J falls below T_{SHTDWN} by approximately 10°C.

INPUT VOLTAGE PROTECTION IN CHARGE MODE

Sleep Mode

The bq24165/6/7 enters the low-power sleep mode if the voltage on V_{SUPPLY} falls below sleep-mode entry threshold, $V_{BAT}+V_{SLP}$, and V_{SUPPLY} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{SUPPLY}. When $V_{SUPPLY} < V_{BAT}+V_{SLP}$, the bq24165/6/7 turns off the PWM converter, and turns the battery FET and BGATE on. Once $V_{SUPPLY} > V_{BAT}+ V_{SLP}$, the device initiates a new charge cycle.

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Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage decreases. Once the supply drops to V_{IN_DPM} (set by IUSB_ for USB input or VDPM for IN input), the input current limit is reduced down to prevent the further drop of the supply. This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 24 shows the V_{IN}-DPM behavior to a current limited source. In this figure the input source has a 750mA current limit and the charging is set to 750mA. The SYS load is then increased to 1.2A.

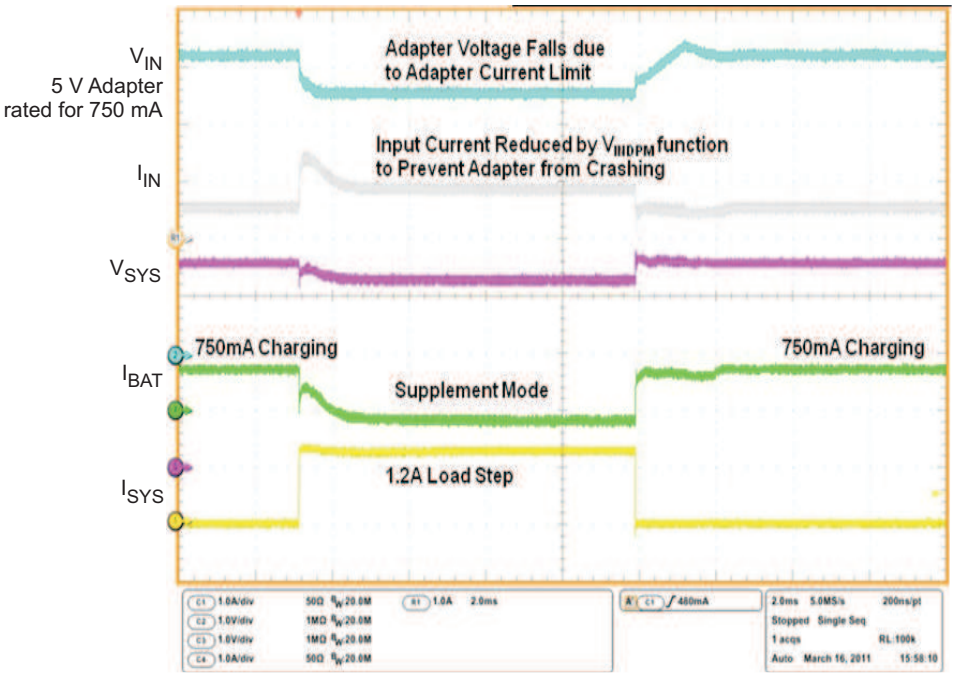

Figure 24. bq2416x V_{IN}-DPM

The V_{IN}-DPM threshold for the IN input is set using a resistor divider with VDPM connected to the center tap. Select 10kΩ for the bottom resistor. The top resistor is selected using the following equation:

$$RTOP = \frac{10\ k\Omega \times \left(V_{INDPM} - V_{DPM}\right)}{V_{DPM}} \quad (7)$$

Where V_{INDPM} is the desired V_{INDPM} threshold and V_{DPM} is the regulation threshold specified in the Electrical Characteristics table. For the QFN packaged ICs, a small capacitance (10pF-100pF) from the VDPM pin to ground may be added if the resistor divider from VIN to VDPM is not placed close to the IC pins, thereby causing significant noise on the VDPM pin.

Bad Source Detection

When a source is connected to IN or USB, the bq2416x runs a Bad Source Detection procedure to determine if the source is strong enough to provide some current to charge the battery. A current sink is turned on (30mA for USB input, 75mA for the IN input) for 32ms. After the 32ms, if the input source is above $V_{BADSOURCE}$ plus hysteresis, where $V_{BADSOURCE}$ is the user set VINDPM threshold, the buck converter starts up and normal operation continues. If the supply voltage falls below $V_{BADSOURCE}$ less hysteresis during the detection, the current sink shuts off for two seconds and then retries. The detection circuit retries continuously until either a new source is connected to the other input or a valid source is detected after the detection time. If during normal operation the source falls to V_{BAD_SOURCE}, the bq2416x turns off the PWM converter, turns the battery FET on. Once a good source is detected, the device returns to normal operation.

If two supplies are connected, the IN supply is checked first. If the supply detection fails once, the device switches to USB for two seconds and then retries IN. This allows the supply to settle if the connection was jittery or the supply ramp was too slow to pass detection. If the supply fails the detection twice, it is locked out and the USB supply is used. Once the bad supply is locked out, it remains locked out until the supply voltage falls below UVLO. This prevents continuously switching between a weak supply and a good supply.

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Input Over-Voltage Protection

The bq24165/6/7 provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from V_{USB} or V_{IN} to PGND). When $V_{SUPPLY} > V_{OVP}$, the bq24165/6/7 turns off the PWM converter, suspends the charging cycle and turns the battery FET and BGATE on. Once the OVP fault is removed, the device returns to the operation it was in prior to the OVP fault.

Reverse Boost (Boost Back) Prevention Circuit

Figure 25. Reverse Boost

A buck converter has two operating states, continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In DCM, the inductor current ramps down to zero during the switching cycle while in CCM the inductor maintains a DC level of current. Transitioning from DCM to CCM during load transients, slows down the converter's transient response for those load steps, which can result in the SYS rail drooping. To achieve the fastest possible transient reponse for this charger, this charger's synchronous buck converter is forced to run in CCM even at light loads when the buck converter would typically revert to DCM. The challenge that presents itself when forcing CCM with a charger is that the output of the buck converter now has a power source. Thus, if the battery voltage, V_{BAT}, is ever greater than V_{BATREG}, the inductor current goes fully negative and pushes current back to the input supply. This effect causes the input source voltage to rise if the input source cannot sink current. The input over-voltage protection circuit protects the IC from damage however some input sources may be damaged if the voltage rises. To prevent this, this charger has implemented a reverse boost prevention circuit. When reverse current is sensed that is not a result of the supplement comparator tripping, this circuit disables the internal battery FET and changes the feedback point to V_{SYSREG} for 1ms. After the 1ms timeout, the BATFET is turned on again and the battery is tested to see if it is higher than V_{BATREG} (negative current). The reverse current protection is only active when $V_{BOVP} > VBAT > VBATREG - V_{RCH}$. Having $V_{BOVP} > V_{BAT} > V_{BATREG} - V_{RCH}$ and termination disabled (e.g., when $\overline{CE1}$ = 1 and $\overline{CE2}$ = 0 but VBAT > 4.06V) results in an approximately 100mV, 1000Hz ripple on SYS as seen in Figure 25. With termination enabled and ITERM > 150mA or with a high line impedance to the battery, the likelihood of activating reverse boost protection circuit is greatly reduced even if $V_{BAT} > VBATREG - V_{RCH}$. The IC stops charging and can exit charge done after entering reverse boost due to a SYS load transient causing a battery supplement event. Charging resumes after V_{BAT} drops below $V_{BATREG} - V_{RCH}$. Therefore, large SYS load transients may result in the battery reaching slightly less than full charge.

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STATUS INDICATORS ($\overline{CHG}$, $\overline{PG}$)

The bq24165/6/7 contains two open-drain outputs that signal its status. The $\overline{PG}$ output indicates that a valid input source is connected to USB or IN. $\overline{PG}$ is low when $V_{SUPPLY}>V_{UVLO}$ AND $(V_{BAT}+V_{SLP}) < V_{SUPPLY} < V_{OVP}$. When there is no supply connected to either input within this range, $\overline{PG}$ is high impedance. Table 3 illustrates the $\overline{PG}$ behavior under different conditions.

During new charge cycles, the $\overline{CHG}$ output goes low to indicate a new charge cycle is in progress or that charge has been suspended due to a TS pin fault or the thermal protection circuit. A new charge cycle is initiated by removing and replacing the battery or toggling the input power. $\overline{CHG}$ remains low until charge termination unless the battery is removed, there is a timer fault or the input supply is no longer valid. After termination of the new charge cycle, $\overline{CHG}$ remains high impedance until a new charge cycle is initiated. $\overline{CHG}$ does not go low during recharge cycles. Table 4 illustrates the $\overline{CHG}$ behavior under different conditions.

Connect $\overline{PG}$ and $\overline{CHG}$ to the DRV output through an LED for visual indication, or connect through a 100kΩ pullup to the required logic rail for host indication.

Table 3. $\overline{PG}$ Status Indicator

CHARGE STATE	$\overline{PG}$ BEHAVIOR
$V_{SUPPLY} < V_{UVLO}$	High-Impedance
$V_{SUPPLY} < (V_{BAT}+V_{SLP})$	High-Impedance
$(V_{BAT}+V_{SLP}) < V_{SUPPLY} < V_{OVP}$	Low
$VS_{UPPLY} > V_{OVP}$	High-Impedance

Table 4. $\overline{CHG}$ Status Indicator

CHARGE STATE	$\overline{CHG}$ BEHAVIOR
New Charge Cycle in progress Charging suspend by TS fault Charging suspended by thermal loop	Low (first charge cycle) High-Impedance (recharge cycles)
New Cycle Charge Done	High-Impedance
Recharge Cycle after Termination	
Timer Fault	
No Valid Supply	
No Battery Present	

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APPLICATION INFORMATION

OUTPUT INDUCTOR AND CAPACITOR SELECTION GUIDELINES

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq2416x is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 8 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (8)$$

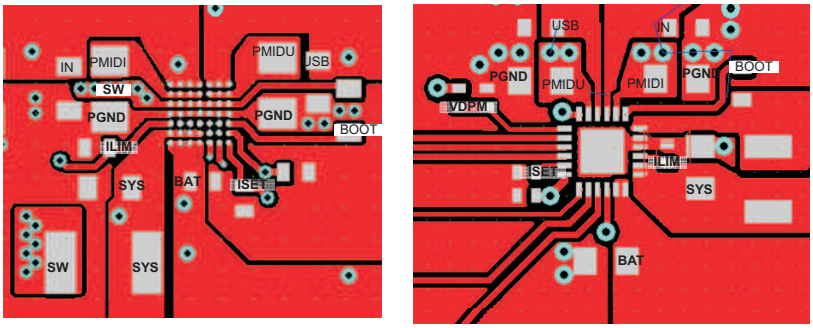
The inductor selected must have a saturation current rating higher than the calculated I_{PEAK}. Due to the high currents possible with the bq2416x, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A for 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times (I_{PEAK} - I_{LOAD}) = 1.5\ A + 0.2 \times (2.5\ A - 1.5\ A) = 1.7\ A$$

The bq2416x provides internal loop compensation. Using this scheme, the bq2416x is stable with 10µF to 200µF of local capacitance. The capacitance on the SYS rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to SYS. A 47µF bypass capacitance on SYS is recommended to optimize the transient response.

PCB LAYOUT GUIDELINES

It is important to pay special attention to the PCB layout. Figure 26 provides a sample layout for the high current paths of the bq2416x.



WCSP Layout QFN Layout

Figure 26. Recommended bq2416x PCB Layout

The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq2416x
- The layout between BAT and the positive connector of the battery should be as short as possible to minimize resistance and inductance. If the parasitic inductance is expected to be significant, the bypass capacitance on BAT should be increased.
- Place 4.7µF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1µF input capacitor GNDs as close to the respective PMID cap GND and PGND pins as possible to minimize the ground difference between the input and PMID_.
- The local bypass capacitor from SYS to GND should be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place ISET and ILIM resistors very close to their respective IC pins.
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into IN, USB, BAT, SYS and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

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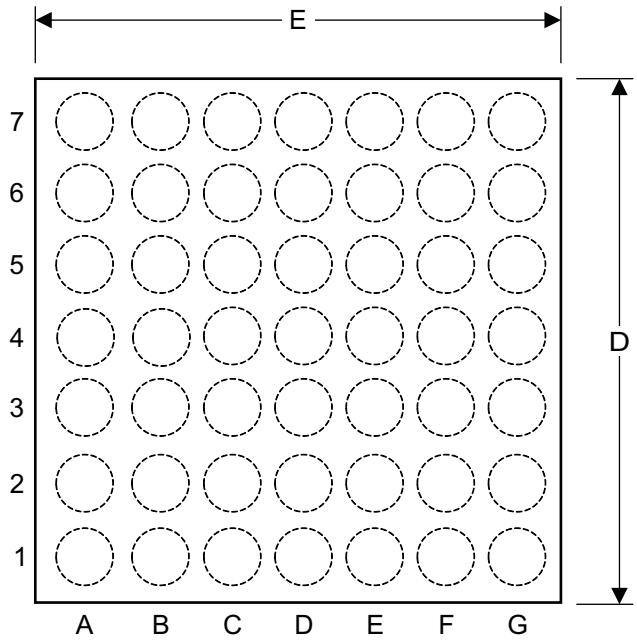
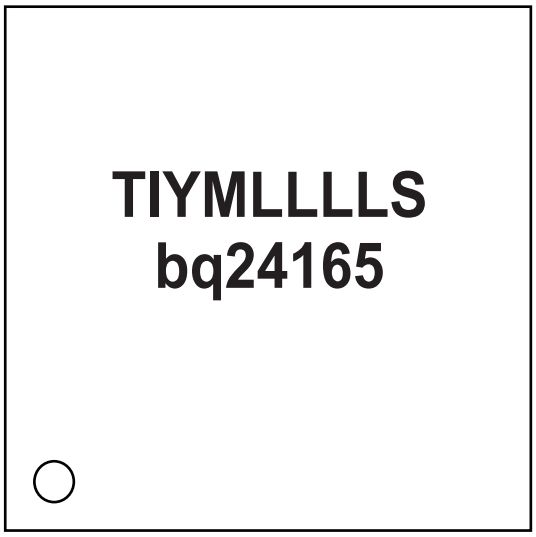
PACKAGE SUMMARY

WCSP PACKAGE
(Top View)



CHIP SCALE PACKAGE
(Top Side Symbol For bq24165)



O - Pin A1 Marker
TI -Texas Instruments Letters
YM - Year Month Date Code
LLLL - Lot Trace Code
S - Assembly Site Code

CHIP SCALE PACKAGING DIMENSIONS

The bq2416x devices are available in a 49-bump chip scale package (YFF, NanoFree™). The package dimensions are:

- D = 2.78mm ±0.05mm
- E = 2.78mm ±0.05mm

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REVISION HISTORY

Changes from Original (December 2011) to Revision A	Page
• Changed in ELECTRICAL CHARACTERISTICS, in row $V_{IN_DPM_USB}$, min, typ, max columns, from 4.55 to 4.35, 4.68 to 4.44 and 4.77 to 4.52 (had been changed)	5
• Changed I_{LIMIT} max from 2.5 A to 5.6 A	5
• Changed Table 1, last column, all 4.68 V to 4.44 V	17

Changes from Revision A (March 2012) to Revision B	Page
• Added Figure 25	23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24165RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24165	Samples
BQ24165RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24165	Samples
BQ24165YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24165	Samples
BQ24165YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24165	Samples
BQ24166RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24166	Samples
BQ24166RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24166	Samples
BQ24166YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24166	Samples
BQ24166YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24166	Samples
BQ24167RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24167	Samples
BQ24167RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24167	Samples
BQ24167YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24167	Samples
BQ24167YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24167	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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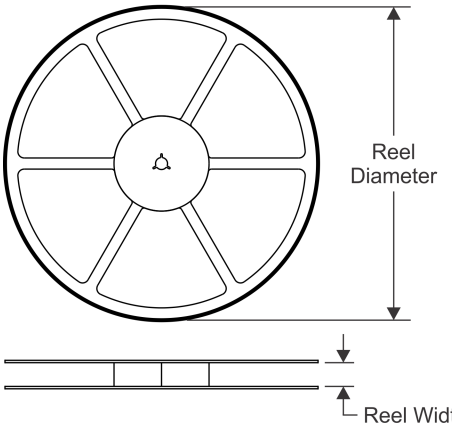
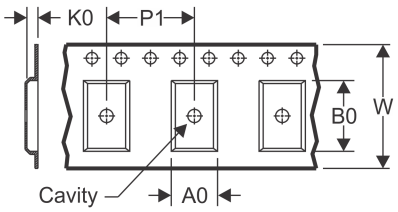
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

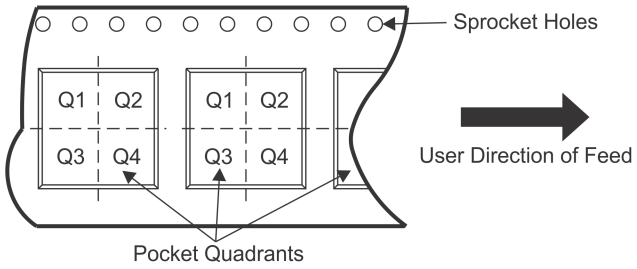


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

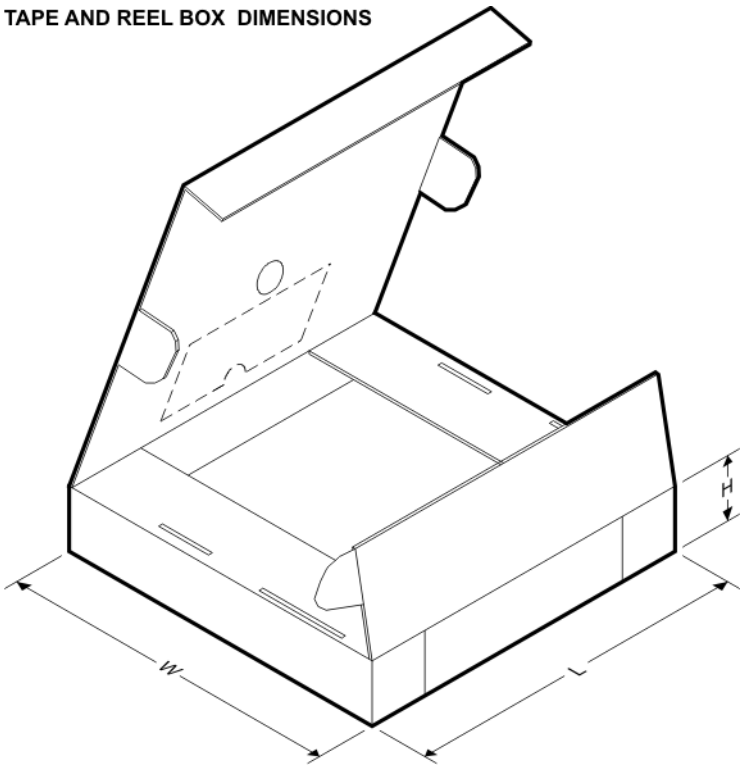
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24165RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24165RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24165YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24165YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24166RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24166RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24166YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24166YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24167RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24167RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24167YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24167YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1

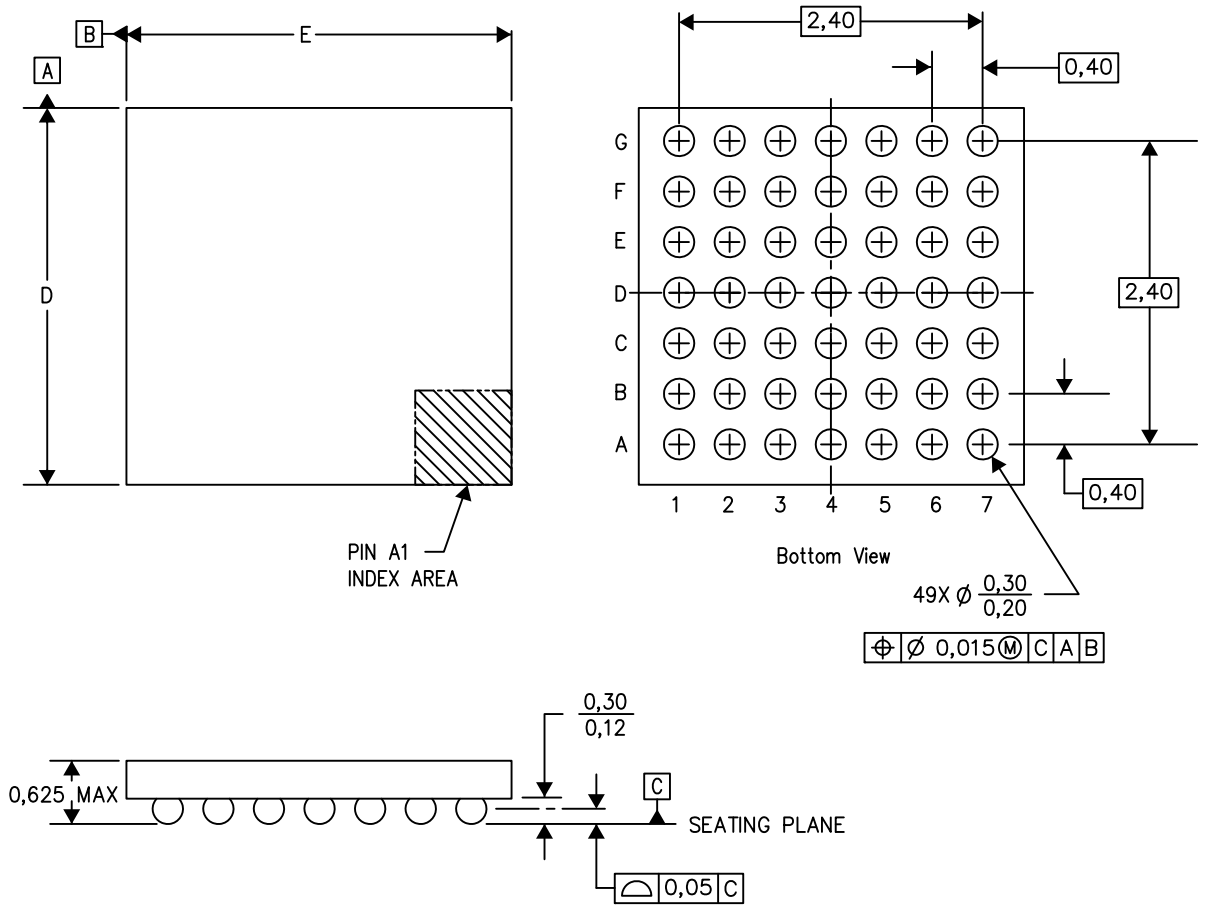
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24165RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24165RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24165YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
BQ24165YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0
BQ24166RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24166RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24166YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
BQ24166YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0
BQ24167RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24167RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24167YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
BQ24167YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



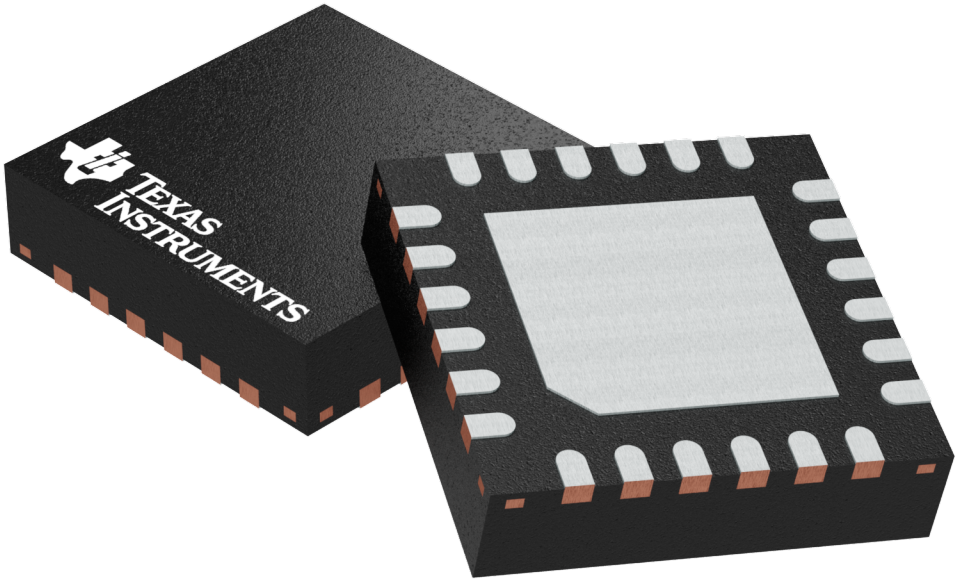
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



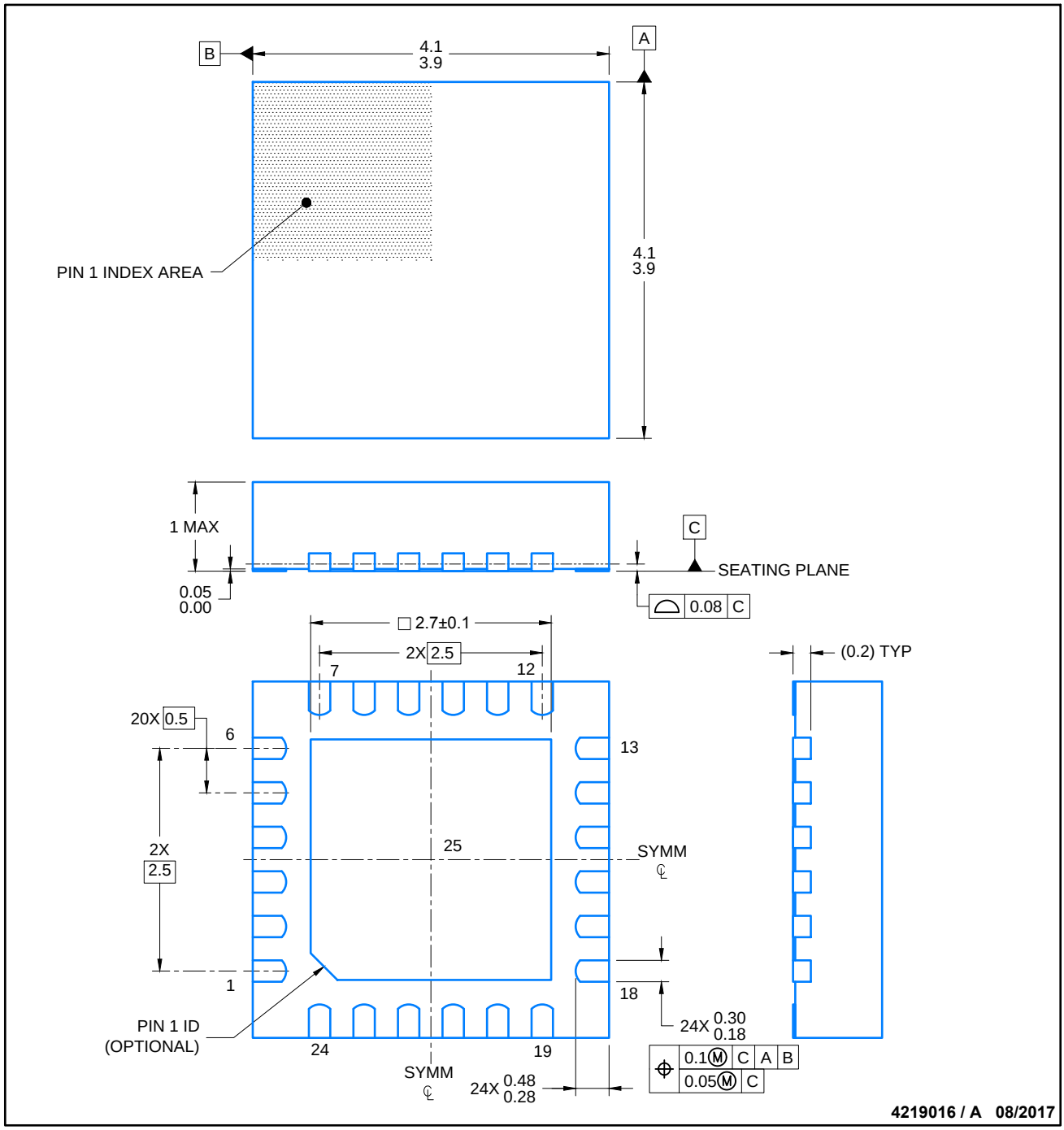
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024H

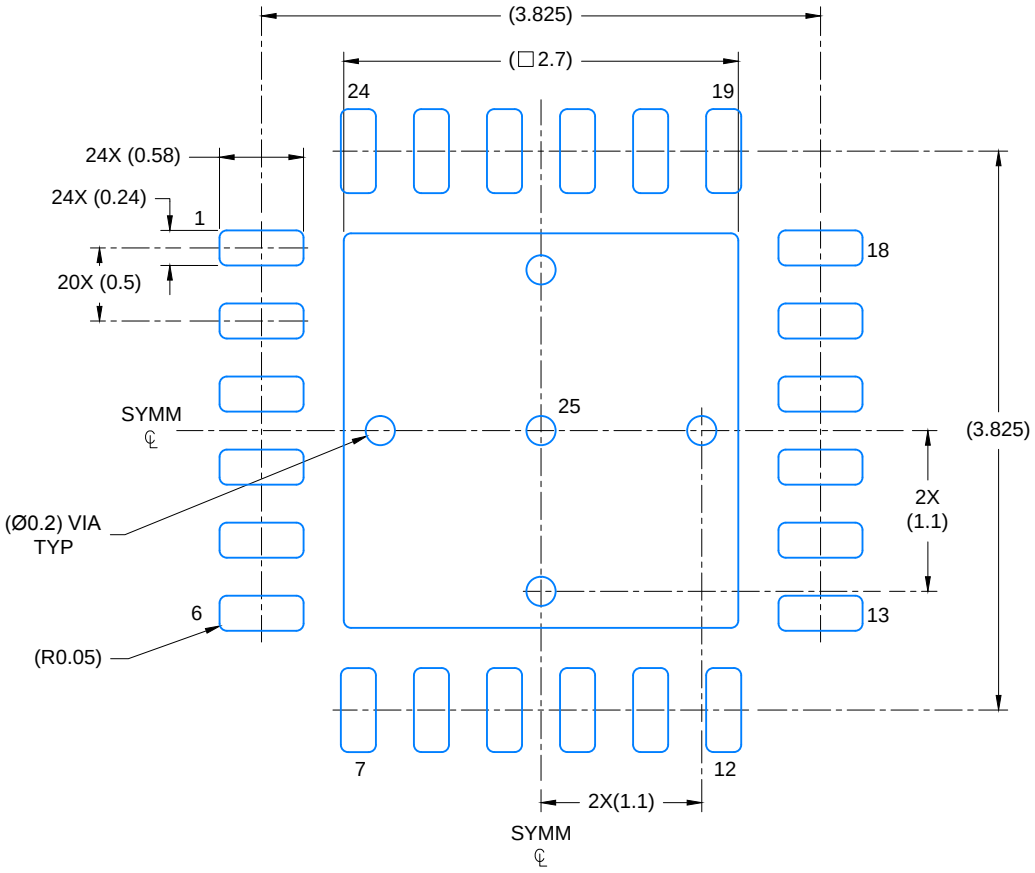
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



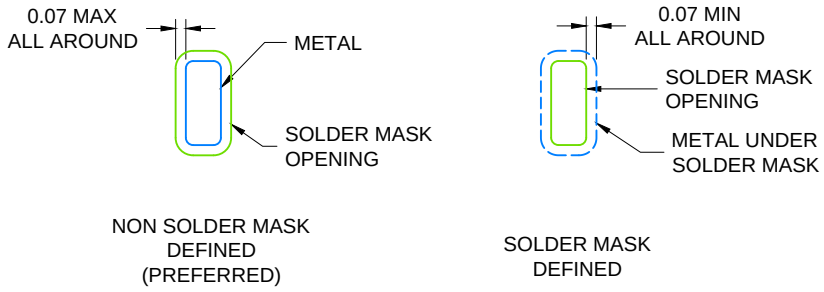
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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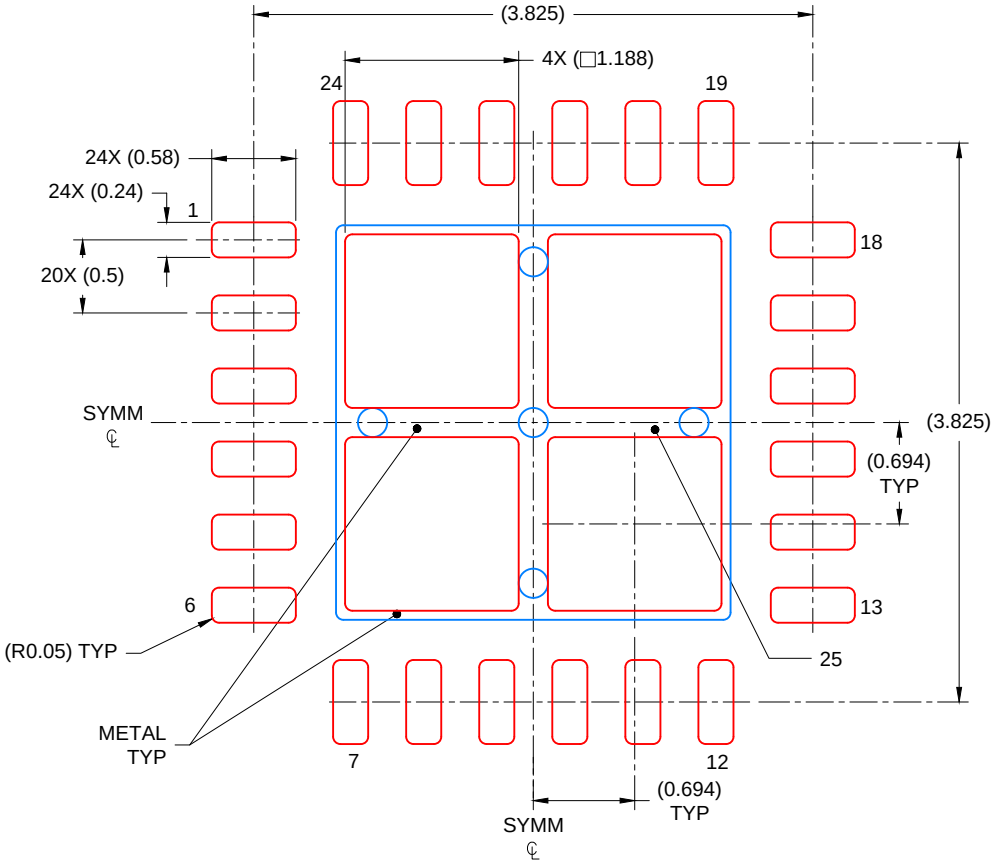
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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