

Optical Image Stabilization (OIS) Controller and Driver

Features

- Core:
 - ARM 32-bit STARCUC with FPU and DSP
 - Frequency up to 56MHz
 - 84 DMIPS, 1.5DMIPS/MHz
- Memories:
 - 64KByte Flash Memory,
 - 4KByte ROM for boot loader,
 - 40KByte Program SRAM
 - 8KByte Data SRAM
- 12-bit AD Converter, Input 4-ch
- 10-bit DA Converter, Output 2-ch
- Hall Bias Circuit, 2-ch
- 2 Programmable Gain Amplifiers
 - Gain(10x,25x,30x,35x,40x,45x,50x,
 - 55x,60x,65x,70x,75x,80x,85x,90x,100x)
- SPI Master/Slave/Monitor I/F
- 2 I²C Master/Slave I/F
 - Slave address: 0xD2/0xD3(Default)
- 2 General Timers and a Watch Dog Timer
- Driver: Constant Current Linear Driver
 - Output 2-ch for OIS, $I_{max}=200mA$
 - Output 1-ch for AF(bi-direction), $I_{max}=130mA$
- Shutdown mode with 10 μ A consumption
- WLCSP 4.2mm × 1.3mm × 0.3mm - 27B package

Applications

Mobile Camera
Digital Still Camera
Camcorder
Security Camera
Web camera

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General Description

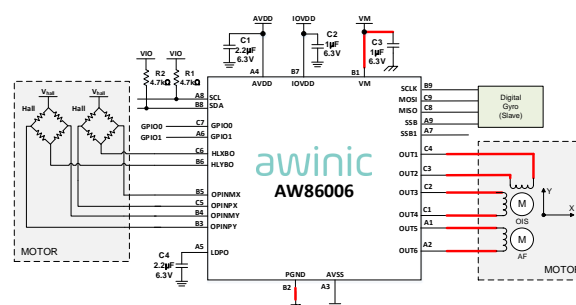
The AW86006 is an optical image stabilization (OIS) controller and driver which also support open-auto focus driving. It is always used in a camera module of smart mobile phone or other camera equipment.

The AW86006 integrates an on-chip 32-bit CPU as controller, a flash memory for program and user data, an ADC with 4 channels, 2 DAC for calibrating hall sensor's offset, 2 hall bias circuit and 3 H-Bridge drivers for OIS and AF.

There is a SPI I/F module which supports master, slave and monitor on chip. The monitor function makes it possible for multiple OIS drivers to exist one camera module. Two I²C are available, one of them is always slave.

The STARCUC is Harvard structure and has own DSP and FPU. The bus for code connects flash, ROM and code SRAM and the bus for data connects data SRAM and APB bridge. With the 56 MHz clock, STARCUC can provide 84DMIPS computing power for algorithm.

Typical Application Circuits



Pin Configuration And Top Mark

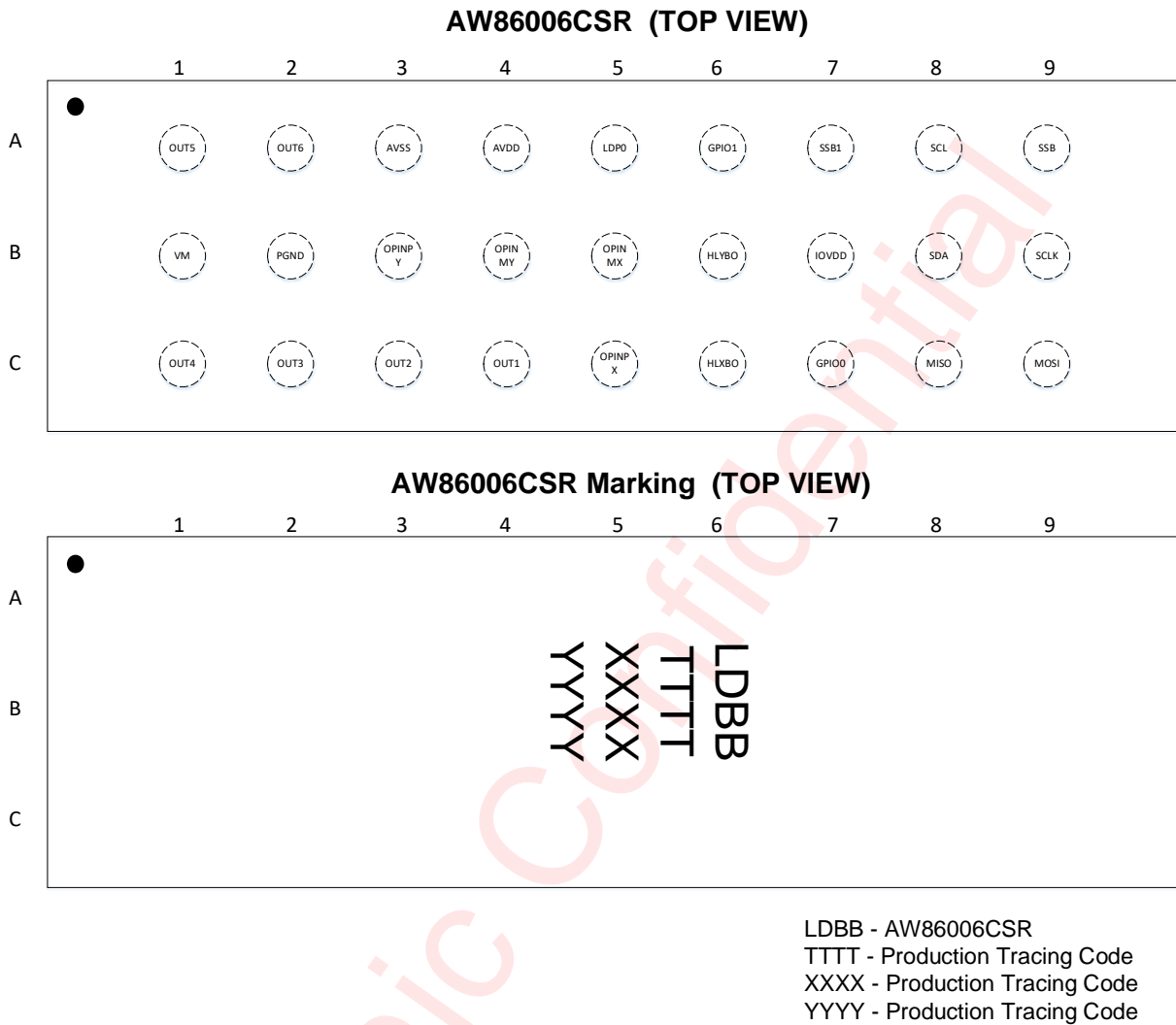


Figure 2 Pin Configuration

Pin Definition

No.	NAME	DESCRIPTION
A1	OUT5	AF drive current output
A2	OUT6	AF drive current output
A3	AVSS	Analog ground
A4	AVDD	Power supply for analog
A5	LDPO	Internal LDO power output
A6	GPIO1	GPIO, also support to be data cable of I ² C and analog signal input
A7	SSB1	Interrupt input, also support to be SPI chip select cable
A8	SCL	I ² C interface clock
A9	SSB	SPI chip select
B1	VM	Power supply for driver
B2	PGND	Driver ground
B3	OPINPY	Positive input of PGA Y
B4	OPINMY	Negative input of PGA Y
B5	OPINMX	Negative input of PGA X
B6	HLYBO	Hall Y BIAS output
B7	IOVDD	Power supply for digital IO
B8	SDA	I ² C interface data
B9	SCLK	SPI interface clock
C1	OUT4	OIS drive current output
C2	OUT3	OIS drive current output
C3	OUT2	OIS drive current output
C4	OUT1	OIS drive current output
C5	OPINPX	Positive input of PGA X
C6	HLXBO	Hall X BIAS output
C7	GPIO0	GPIO, also support clock cable of I ² C, interrupt input and analog output
C8	MISO	SPI interface data in
C9	MOSI	SPI interface data out

Functional Block Diagram

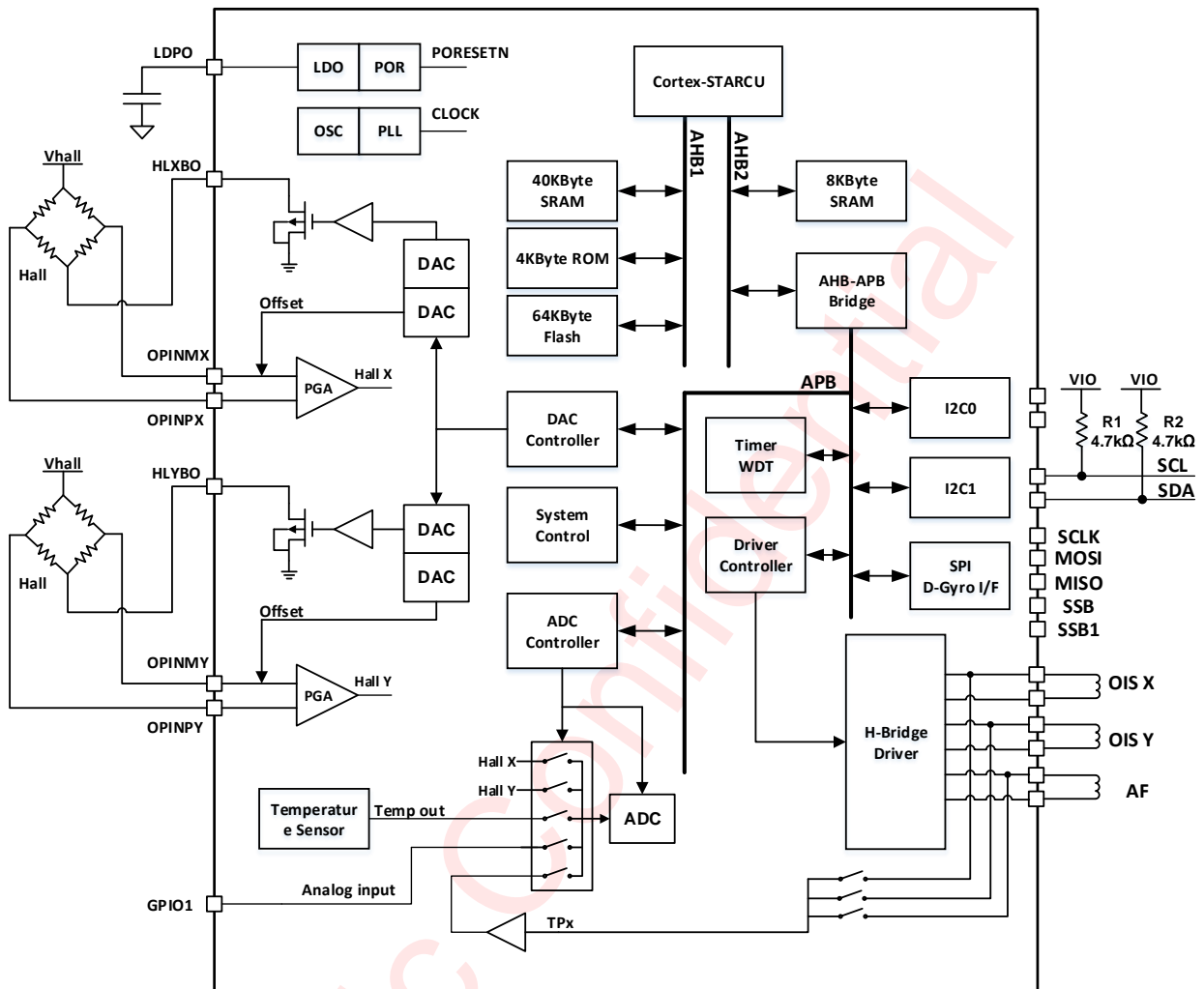


Figure 3 FUNCTIONAL BLOCK DIAGRAM

Typical Application Circuits

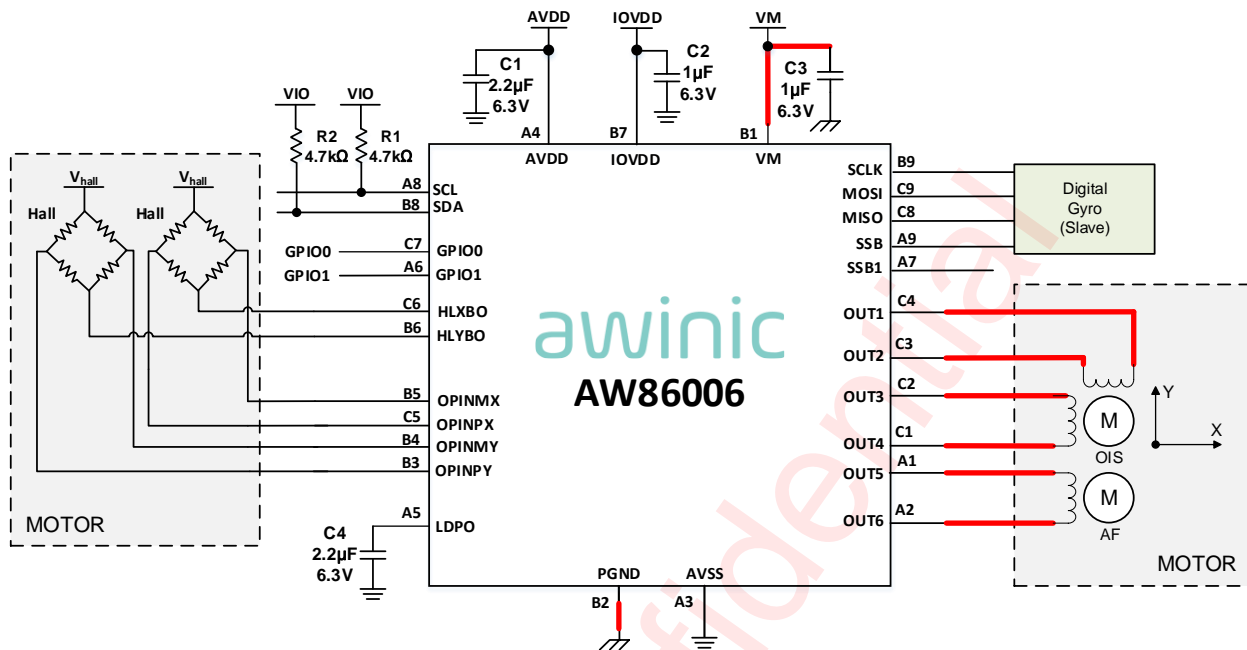


Figure 4 AW86006 Application Circuit

Notice for Typical Application Circuits:

1. If there is no specialized V_{hall} for hall device, it can be replaced by AVDD.
2. The 4.7kΩ pull-up resistor of I2C is for 400KHz application. For 1MHz application, it should be 1kΩ.
3. It is recommended that the voltage of VIO be equal to the IOVDD.

Recommended Operating Condition

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Analog power supply voltage	V_{AVDD}	2.7	2.8	3.3	V
Input voltage range	V_{INA}	0		V_{AVDD}	V
Driver power supply voltage	V_{VM}	2.7	2.8	3.3	V
Driver pin input voltage range	V_{INM}	0		V_{VM}	V
GPIO power supply voltage	V_{IOVDD}	1.8	1.8	3.3	V
GPIO input voltage	V_{GPIO}	0		V_{IOVDD}	V

Notice: Devices working under the conditions in those ranges listed in "Recommended Operating Condition" can show the best performance.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86006CSR	-40°C~85°C	WLCSP 4.2mm×1.3mm-27B	LDBB	MSL1	ROHS+HF	6000 units/ Tape and Reel

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Absolute Maximum Ratings^(NOTE1)

PARAMETERS	SYMBOL	RANGE
Power Supply Voltage	V _{AVDD}	-0.3 to 4.5V
	V _{VM}	-0.3 to 4.5V
	V _{LDPO}	-0.3 to 2V
	V _{IOVDD}	-0.3 to 4.5V
Input / Output voltage	V _{GPIO}	-0.3 to IOVDD+0.3V
OIS Input / Output Current		±220mA
AF Input / Output Current		±165mA
HALL BIAS Output Current		+10mA
Operating Temperature		-40 ~ 85°C
Storage Temperature		-55 ~ 125°C
ESD(Including CDM HBM) ^(NOTE 2)		
ALL PIN(HBM) ^(NOTE 2)		±2000V
ALL PIN(CDM) ^(NOTE 3)		±1500V
Latch-Up		
Test method: JESD78E		+IT: 200mA -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: Test method: ESDA/JEDEC JS -002-2014.

Electrical Characteristics

AVDD=VM=2.8V, IOVDD=1.8V, AVSS=PGND=0V, environment temperature 25°C.

Characteristics	Symbol	conditions	Min.	Typ.	Max.	Unit
General Section						
UVLO						
UVLO High Level	V _{UVLOH}	VDDA ramp-up		2		V
Hysteresis	V _{HYS}			0.1		V
Operating Current						
Analog / Digital IO Supply	I _{VDDA}	System Clock = 56MHz		30		mA
Motor Supply	I _{VDDM}	No load	-1		10	μA
Standby Current						
Analog Supply	I _{SBA}	System Clock = 2MHz		5.0		mA
Motor Supply	I _{SBM}		-1		10	μA
Shutdown Current	I _{SD}		-1		10	μA
Analog Block						
Hall Bias DAC						
Minimum Output Current	I _{HB_MIN}		0			mA
Maximum Output Current	I _{HB_MAX}			4		mA
Resolution	RES _{HB}			8		Bits
Programmable Gain Amplifier						
Low Input Leakage Current High	I _{PGA_LKGL}	V _{IN} = 0V	-1		1	μA
Input Leakage Current Input	I _{PGA_LKGH}	V _{IN} = VDDA	-1		1	μA
Minimum Input Gain	V _{PGA_GAIN}			10		-
Maximum Input Gain	V _{PGA_GAIN}			100		-
Hall Offset DAC						
Resolution	RES _{HOFF}			8		Bits
Full Scale Output Voltage	V _{HOFFDAC}		-50		50	mV
Hall ADC						
Resolution	RES _{ADC}			12		Bits
OIS Driver (X,Y)						
OIS linear current DAC resolution	RES _{OIS_D AC}			12		Bits
On Resistance Output	R _{XYON}			2.5		Ω
Current Compliance	I _{XYMAX}	Full code	190	200	210	mA
Current	I _{XYOFFLKG}	Output set to Hi-Z	-10		10	μA
AF Driver (Z) Linear						
AF linear current DAC resolution	RES _{AF_D AC}			10		Bits

On Resistance Minimum	R _{ZON}			2.5		Ω
Current Compliance	I _{ZMAX}	Full code	120	130	140	mA
Current	I _{ZOFFLKG}	Output set to Hi-Z	-10		10	μA
Logic I/O Interface						
SPI (SCLK, SSB, SSB1, MOSI, MISO)						
Low Level Input Voltage	V _{IL1}				0.3IOVDD	V
High Level Input Voltage	V _{IH1}		0.7IOVDD			V
Low Level Input Current	I _{IL1}	VIN = IOVDD	-1		1	μA
High Level Input Current	I _{IH1}	VIN = VSSA	-1		1	μA
Low Level Output Voltage	V _{OL1}	Sink current = 2mA			0.2IOVDD	V
High Level Output Voltage	V _{OH1}	Source current = -2mA	0.8IOVDD			V
Pull Up Resistor	R _{UP1}		20	60	200	kΩ
I2C (SCL, SDA)						
Low Level Input Voltage	V _{IL2}				0.54	V
High Level Input Voltage	V _{IH2}		1.26			V
Low Level Input Current	I _{IL2}	VIN = VDDA	-1		1	μA
High Level Input Current	I _{IH2}	VIN = VSSA	-1		1	μA
Glitch Rejection	T _{GR}	Measured at 70%		50		ns
Low Level Output Voltage	V _{OL2}	Sink current = 2mA			0.3	V
GPIO (GPIO0, GPIO1)						
Low Level Input Voltage	V _{IL3}				0.3IOVDD	V
High Level Input Voltage	V _{IH3}		0.7IOVDD			V
Low Level Input Current	I _{IL3}	VIN = IOVDD	-1		1	μA
High Level Input Current	I _{IH3}	VIN = VSSA	-1		1	μA
Low Level Output Voltage	V _{OL3}	Sink current = 2mA			0.2IOVDD	V
High Level Output Voltage	V _{OH3}	Source current = -2mA	0.8IOVDD			V
Pull Up Resistor	R _{PU3}		20	60	200	kΩ
Pull Down Resistor	R _{DN3}		20	60	200	kΩ

Power Supply Timing

Following is power on and power off timing, more information about timing and power supply sequence shown in “AN-009_Power_Supply_Guide_EN”.

Parameter			Value			UNIT
No.	Symbol	Name	MIN	TYP	MAX	
1	t_{rising}	Rising time of power supply			3	ms
2	t_{falling}	Falling time of power supply	0			ms
3	IPUR	Instant Power-up rate			100	mV/us
4	t_{low}	Time between power off and power on	20*			ms

Note: There should be no step during power-up, and instant IPUR does not exceed 100mV/us.

* The t_{low} is to make sure the power supply below 100mV after power off.

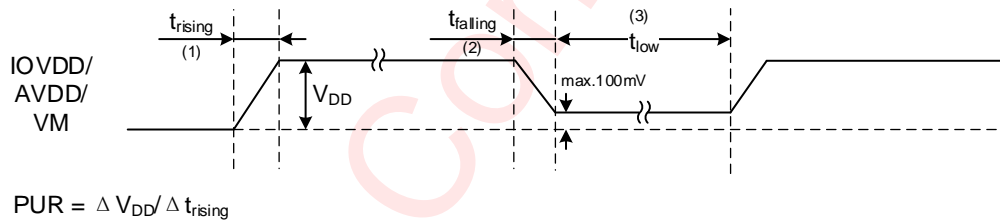


Figure 5 Power on timing and power off timing

I2C Timing Feature

Parameter			Fast mode			Super-fast mode			UNIT
No.	Symbol	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f _{SCL}	SCL Clock frequency			400			1000	kHz
2	t _{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t _{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t _{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t _{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	t _{SU:STA}	Setup time SCL to START state	0.6			0.3			μs
7	t _{HD:STA}	(repeat-start) start condition hold time	0.6			0.3			μs
8	t _{SU:STO}	Stop condition setup time	0.6			0.26			μs
9	t _{BUF}	Time between start and stop condition	1.3			0.5			μs
10	t _{SU:DAT}	SDA setup time	0.1			0.05			μs
11	t _{HD:DAT}	SDA hold time	0			0			ns

NOTE: This timing feature is tested on the basis of the system clock frequency of 56MHz.

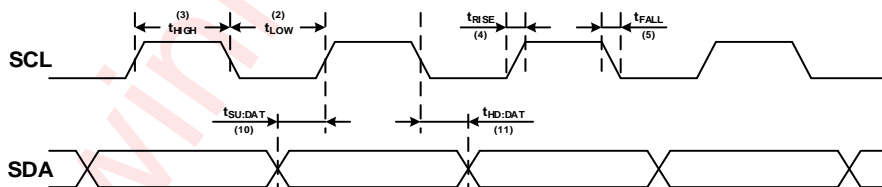


Figure 6 SCL and SDA timing relationships in the data transmission process

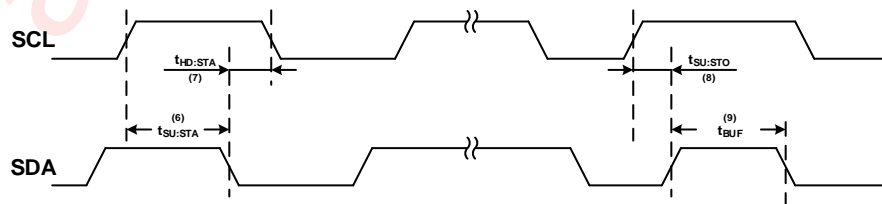


Figure 7 The timing relationship between START and STOP state

SPI Timing Feature(for slave)

Parameter			Fast mode			UNIT
No.	Sym	Name	MIN	TYP	MAX	
1	f _{sck}	SCLK Clock frequency			7	MHz
2	t _{DS}	MOSI data setup time	10			ns
3	t _{DH}	MOSI data hold time	60			ns
4	t _{DO}	Time of SCLK falling edge to MISO data update			60	ns
5	t _{CSH}	Time of SSB rising edge to the last edge of SCLK	50			ns
6	t _{CS2}	Time of SSB being high between 2 transmissions	120			ns
7	t _{CSS}	Time of SSB falling edge to the first edge of SCLK	210			ns
8	t _{CH}	SCLK high level Duration	70			ns
9	t _{CL}	SCLK low level Duration	70			ns

NOTE: This timing feature is tested on the basis of the system clock frequency of 56MHz.

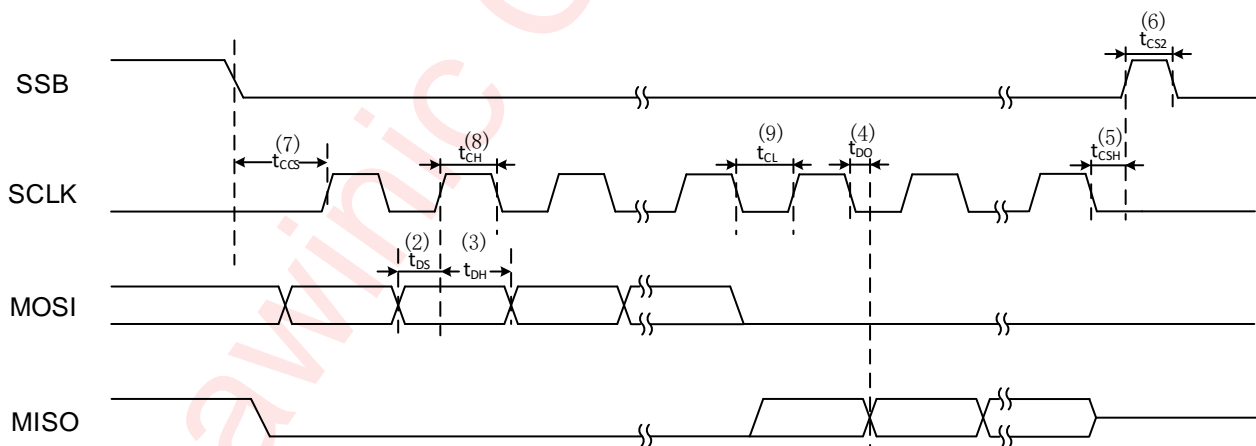
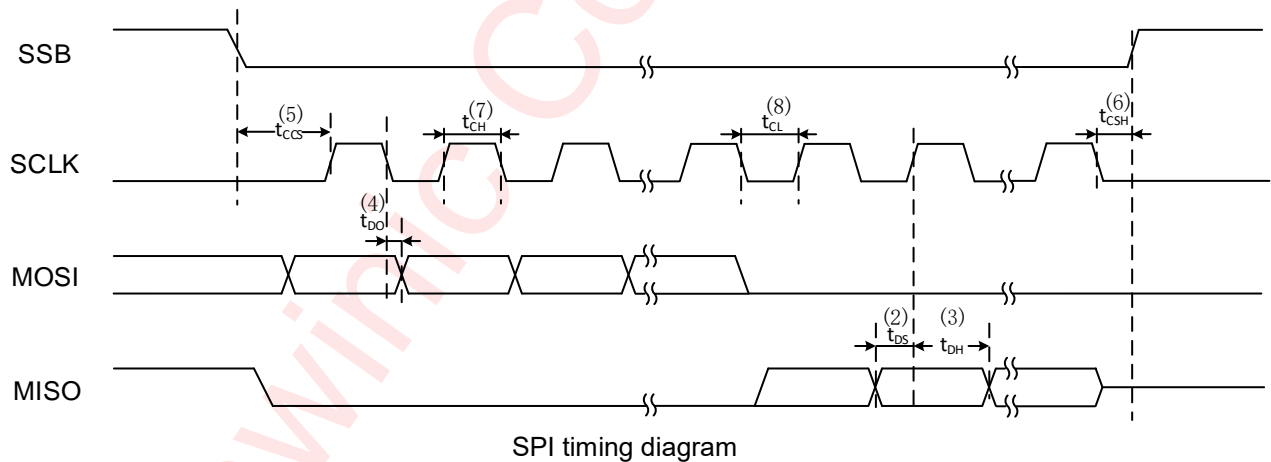


Figure 8 SPI timing diagram

SPI Timing Feature(for master)

Parameter			Fast mode			UNIT
No.	Sym	Name	MIN	TYP	MAX	
1	f _{SCK}	SCLK Clock frequency			7	MHz
2	t _{DS}	MISO data setup time	10			ns
3	t _{DH}	MISO data hold time	60			ns
4	t _{DO}	Time of SCLK falling edge to MISO data update		5		ns
5	t _{CS}	Time of SSB falling edge to the first edge of SCLK		210		ns
6	t _{CSH}	Time of SSB rising edge to the last edge of SCLK		140		ns
7	t _{CH}	SCLK High level Duration	70			ns
8	t _{CL}	SCLK Low level Duration	70			ns

NOTE: This timing feature is tested on the basis of the system clock frequency of 56MHz.



Detailed Functional Description

AW86006 is a OIS controller and driver, for OIS application, it contains a 12-bit ADC with 437.5KHz sample rate and 4 independent channels, 4 channel DACs to produce BIAS current for hall and calibrate hall's offset and 2 H-Bridge drivers with 200mA maximum drive current for OIS and 1 driver with 130mA for AF. For stronger computing power, we choose a Cortex-STARCU, a CPU with ARMv8 architecture which can provide 1.5DMIPS computing power pre MHz, to be chip's control unit. Independent oscillator and PLL provide a stable clock , which make this system could work at the frequency 56MHz.

LOW POWER MODE

This chip has 3 working stages after powered on: Power-On, Boot and Operate. In Power-On stage, the chip is hold in reset status until some necessary initialization done automatically in background. After Power-On stage, by default, the chip would enter Boot stage for ISP firmware upgrading purpose.

If there is already an application program located in Flash and user doesn't issue any transmission(through I2C or SPI), Awinic Boot Loader would jump to and run that application program after 6ms. However, if no firmware upgrading is required and user wish to enter Operate stage as soon as possible, it is always able to skip the Boot stage by sending a special command to boot loader by either I2C or SPI. For more information about Awinic boot loader and ISP(In-System-Programmable) firmware upgrading, please refer to "Awinic boot loader Spec V1.0".

Application program would run in Operate stage to achieve most functions provided by the chip. For the purpose of supporting low-power scenarios, this chip provides 3 working modes in Operate stage which are: Active mode, Standby mode and Shutdown mode. In Active mode, all system sub modules are enabled and the chip is operating in full-functional-full-speed status. In Standby mode:

1. ADC stops sample and quantization
2. All 2 Hall sensors shut down
3. All 3 H-Bridge drivers shut down
4. Internal temperature sensor shuts down
5. Working status of oscillator, PLL and LDO are independent with Standby mode

In Shutdown mode almost all sub modules, including LDO, oscillator and PLL, are closed for maximum power consumption reduction. These 3 working modes are mutual switchable in the following way:

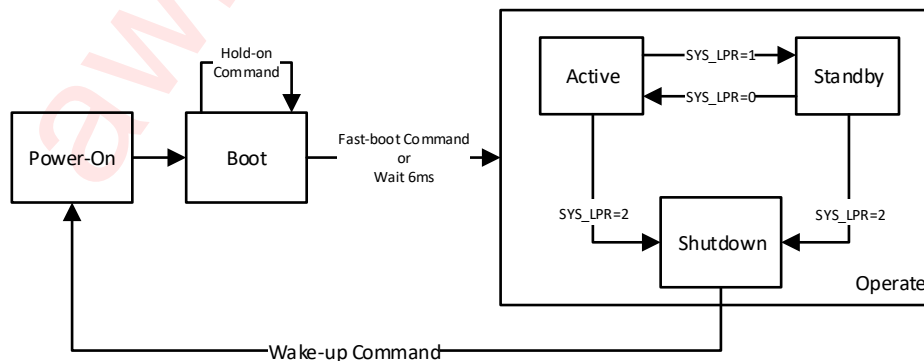


Figure 9 Working stages and modes

STARCU CORE

The main controller of this system is a 32-bit CPU, Cortex-STARCU. Please read the “STARCU User Guide” for more information.

SPI INTERFACE

There is a SPI interface which support 3/4 wire master/slave/monitor mode. The speed of interface is up to 7MHz when HCLK is equal to 56MHz. There are four possible combinations for the serial clock phase and polarity. It is a full-duplex serial protocol when set to 4 wire mode.

MASTER

When SPI is working as a master, there are 3 CS output can select. The MISO can also be used as CS but it is feasible only in 3 wire mode. Because of having 3 CS, this master can connect up to 3 slaves and if an AW86006 is one of them this master can even set it to be a monitor or a slave through just changing the level on CS line.

This SPI support 4 transfer modes: transmit & receive mode, transmit only mode, receive only mode and EEPROM read mode. The transmit & receive mode is a full duplex transferring, there will always be a valid data is received after every frame transmit done. In the transmit(receive) only mode the receive(transmit) function will be disabled. The EEPROM read mode is just familiar to the protocol when reading a EEPROM chip, there is no data to be received when transmitting data and no data to be transmitted when receiving data. The EEPROM read mode is unavailable possible when salver(monitor) mode.

There are two FIFOs in SPI module, which are the basic of transferring. Data should be send to the TX FIFO when transmitting data and received data could be read from RX FIFO. How many frames the transferring will hold is determined by amount of data in TX FIFO in transmit & receive mode and transmit only mode. In the EEPROM read modes, after all the data in TX FIFO is transmitted, the number of data frames to be continuously received is determined by registers CTRL1.

SLAVE&MONITOR

When programming the SPI slave(monitor), the base address(0x40003100) is just different from the SPI master's(0x40003000). The register IS_MST determines this SPI is a master or not, and is this SPI a slave or a monitor just depend on external CS input. When it is set to slave mode, it is just a standard SPI slave. When programming, it should be considered that if the time interval between two data frames is long enough for CPU processing the receive data and sending transmitted data to TX FIFO.

In OIS case, the OIS chip need to get gyro chip's data, the monitor can get the same data on SPI bus and does not affect the transferring on the bus during a SPI master is reading data from the gyro chip. Figure 10 shows that there are two OIS chips and only one gyro chip in the system. Each OIS chip could be the SPI master and the other one could be a slave or monitor. If it is just a monitor, the SSB1 may be not connected and there are more OIS chip can be connected in, what is needed to do is connecting all SSB together. If the SSB1 is connected in, the master can set the other chip to be a slave or monitor by changing the level of two CS.

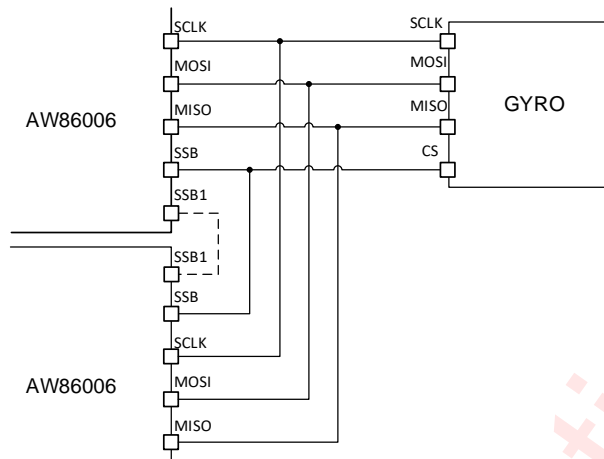


Figure 10 Two OIS Chips in a System

If 3 OIS chip is in the system, Figure 11 shows the connection method. In this case, every OIS chip could be the master and control others to be slave or monitor, by just changing the level of CS, or more accurately, selecting different CS line to access. The MISO is used for being a CS line instead of data line so it is feasible only in 3 wire mode. Inside the chip, the SSB, SSB1, and MISO could be mapped to CS0, CS1, CS2. The CS0 of three chips should be always connected and every CS1(CS2) should be connected with another chip's CS1 or CS2.

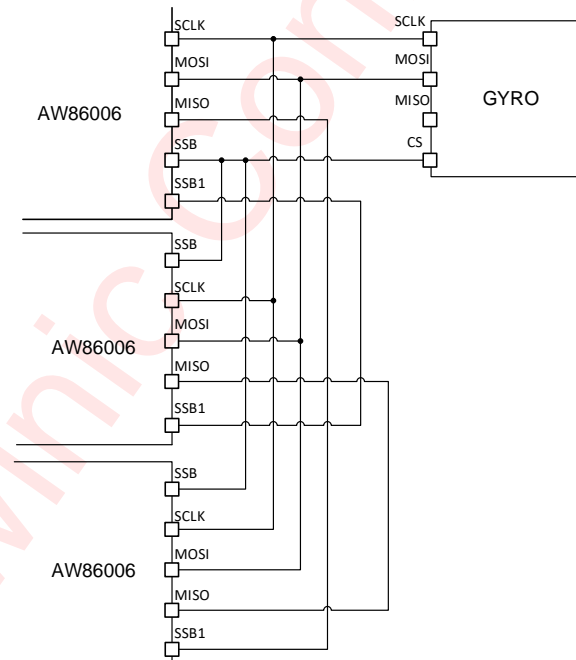


Figure 11 Three OIS Chips in a System

The chip's status is controlled as table 1 shows. There is only one CS could be active at the same time, the master can control it through the register CS_ENR.

Table 1 Chip Status of SPI

CS0	CS1 & CS2	STSTATUS
0	1	Monitor
1	0	Slave
1	1	Idle
0	0	Forbidden

I2C INTERFACE

There are two I²C modules in the chip. One(base address 0x40005000) is always a slave and the other can be a master and also a slave. These two are both support the fast mode(1 MHz). The CPU interact with the I²C through a FIFO, CPU write data to the FIFO then I²C transmit the data out and read data from FIFO when receive data from bus. When the I²C receive a read instruction and there is no data in TX FIFO, the SCL cable will be pull down until there is valid data in FIFO. During this process, the master should wait for the SCL to become high again.

The length of deglitch can be set longer by the registers if the bus is not very stable but the speed of I²C will be affect.

AFE CONTROL

There is a 12-bit SAR ADC whose sampling rate is up to 437.5KHz on chip. This ADC can support 5 channels sample in order and each channel can set different signal to sample. It also support that several channels sample the same signal and get result separately. For OIS application, the signal need to be sampled include the hall signal from two channels and internal temperature sensor. For every channel, it can support up to 8 times average but it is limited by the highest sampling rate. The highest sampling rate is 437.5KHz which mean that it takes about 2.3us to sample one signal one time. If the period of control loop is 50us, in each period the ADC can sample 21 times so the sum of average that is set to each channel cannot bigger than 21.

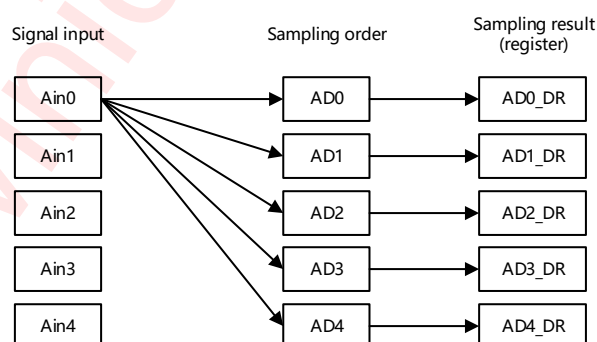


Figure 12 Sampling in Order

ADC support single sampling, timed sampling and continuous sampling. Which signal and how many times will be sampled in these modes all follows the register configuration. The ADC control module will produce a interrupt when sample all channels done once if interrupt was enabled. CPU can start sampling by write 1 to TRANS_EN bit and know if it is sampling through this bit because this bit will become 0 automatically if sampling is finished. The trigger for sampling beginning is from interrupt of TIMER1 in timed sampling mode.

When sample one signal several times for average, there are two sampling ways. One is that samples one

signal continuously and get average then samples the next signal. Another way is samples the signal once and samples the next signal immediately and get average at last.

Except the hall and temperature sensor, some internal signal and the signal from GPIO1 can also be sampled by ADC in some case like FRA measurement. Figure 13 shows the hall signal path to ADC in OIS case. The offset of hall can be calibrated by a 10-bit DAC.

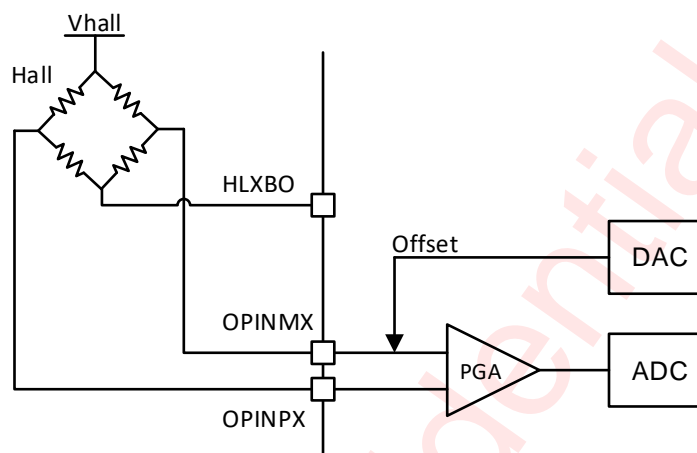


Figure 13 Hall Signal Path to ADC

To get the correct hall signal, a suitable BIAS current will be needed. Pin HLXBO and HLYBO can produce output current up to 5mA for hall. It is controlled by a 8-bit DAC and the code of DAC is just from register. Figure 14 shows the BIAS current output circuit.

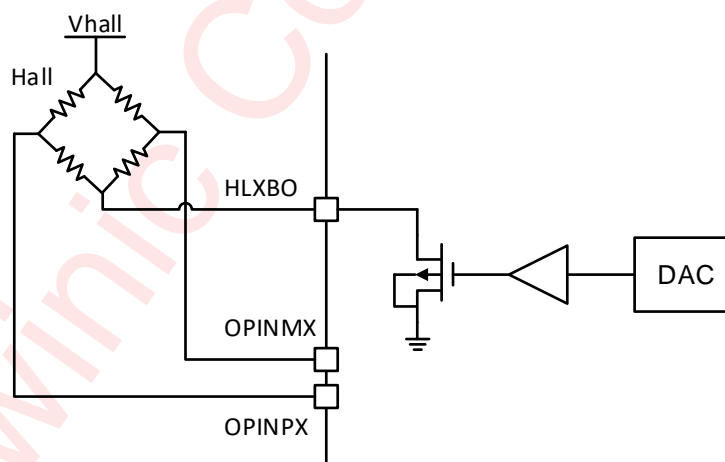


Figure 14 Hall BIAS Output

DRIVER CONTROL

There are 3 independent H bridge driver for 3 motors and they can drive 3 motors at the same time. The motor X and motor Y is under close loop control, the hall can indicate the position of motor and this close loop control is continuous in the CPU so the code in register is send to DAC directly. The motor Z does not have a hall so it is an open loop control and the code in register is send to the AF driver control module and the code will be processed by an algorithm then arrives DAC finally.

There are 4 open loop control algorithms and a programmable control algorithm on chip. These algorithm can

make the motor enter a stable state faster. The open loop algorithm will take several ms and in this process the DAC code in register cannot be modified.

The motor X and Y driver is all 12bit, the motor Z driver is 10bit. The MSB is always the sign bit and indicate the direction of current. The MSB is 1, indicating that the current from odd to even. The MSB is 0, indicating that the current from even to odd. The circuit is shown in Figure 15 and 16.

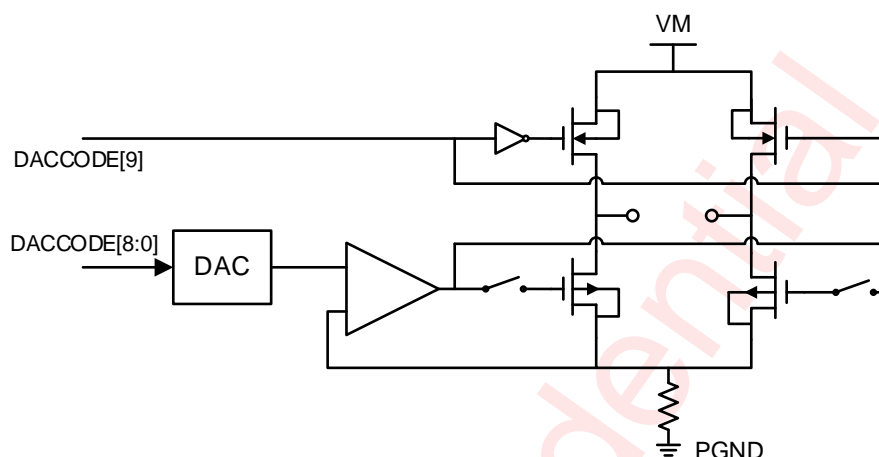


Figure 15 H-Bridge Driver Circuit

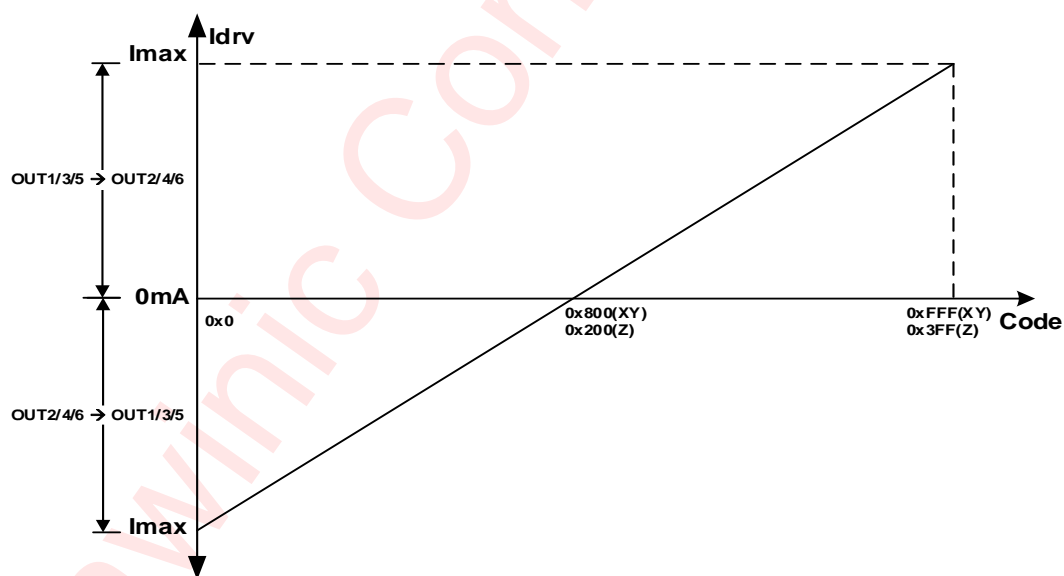


Figure 16 H-Bridge Driver Current direction

TIMER

This chip contain three 32-bit timers: 2 general timers and a watch dog timer.

WATCH DOG TIMER

This timer is used for reset the CPU and peripherals when program running error. This watch dog has two work modes, one is that CPU must feed dog before timeout and the other is that CPU could feed dog in the interrupt

of watch dog. No matter which mode the reset will always happen if CPU did not deed dog and the difference is happening at first timeout or second timeout. Almost all modules are under the control of watch dog except the system control module.

GENERAL TIMER

There are two general timers can be used for algorithm or other functions. These timers support timeout interrupt and get the current counter value, both count down. The timers' clocks always follow the HCLK.

GPIO

The chip has 9 GPIO pins which all have different function. They all have one thing in common that can be set to general-purpose IO. When as a general-purpose IO, they all support output, input and interrupt detection. Because the SCL and SDA only support open-drain output, the output level and register value are opposite. Input value has no effect.

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PCB Layout Consideration

EXTERNAL COMPONENTS PLACEMENT

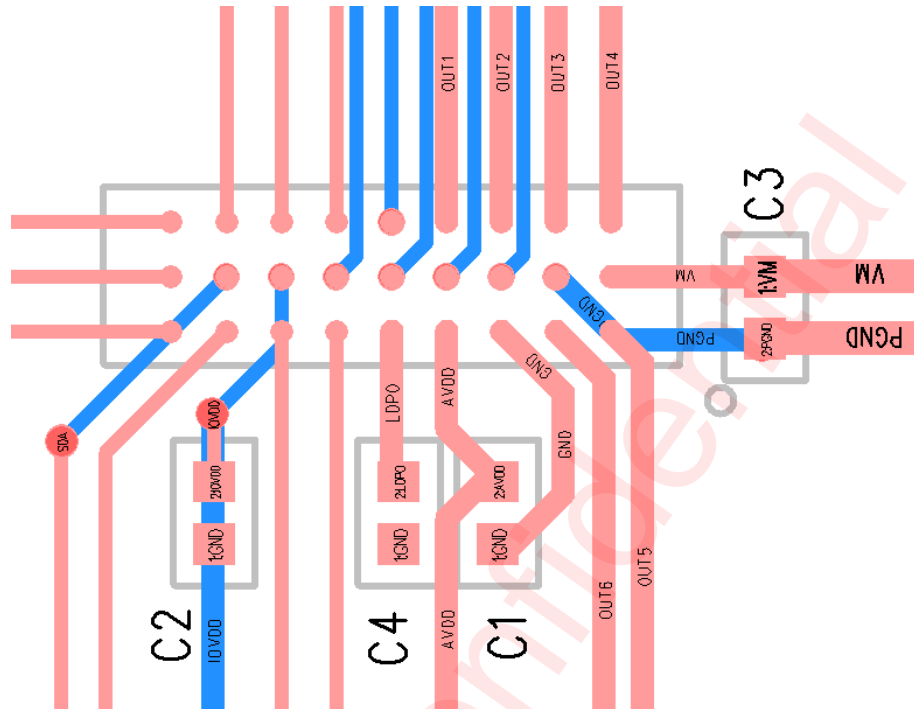
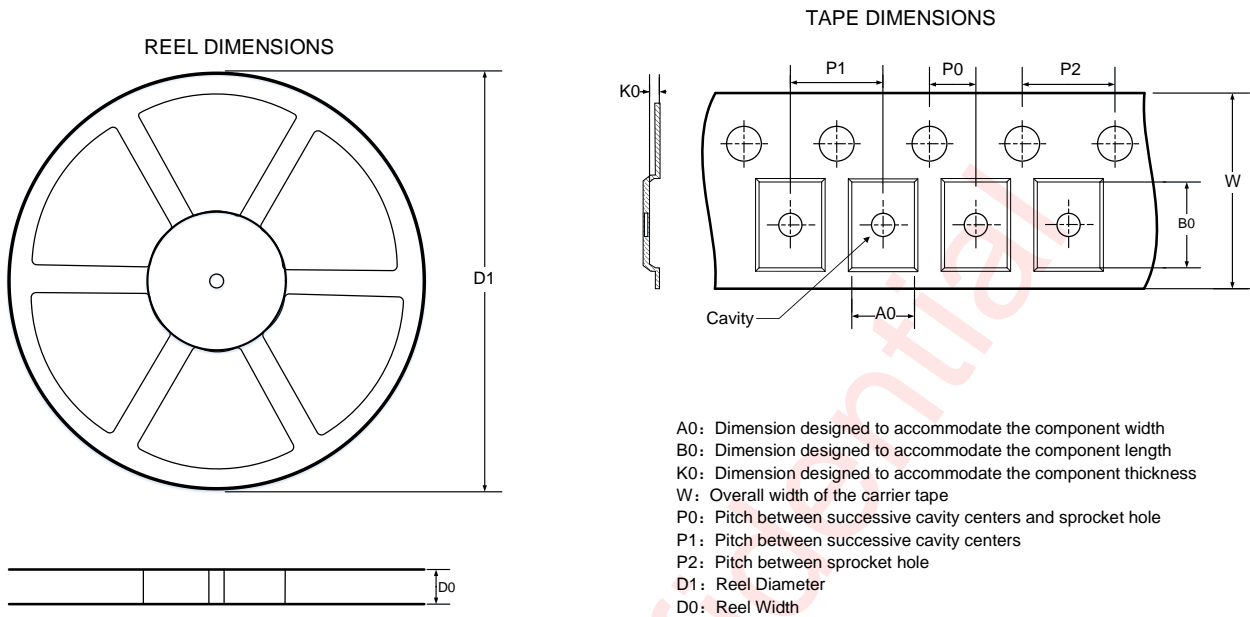


Figure 17 AW86006CSR External Components Placement

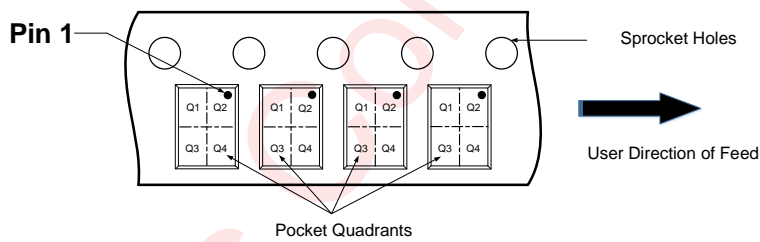
AW86006 is a OIS driver chip, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All peripheral components should be placed as close to the chip as possible. C₁, C₂, C₃, C₄ should be close to AVDD, IOVDD, VM, LDPO pins respectively. Avoid to connect device and chip pins with two different layers of copper, use the same layer of copper instead. And the connection lines should be as short and wide as possible, to reduce noise and EMI interference.
2. The red line in typical application circuit mean these are large current in these lines. The current of OUT1, OUT2, OUT3, OUT4 is 200mA, OUT5's and OUT6's is 130mA. VM is the power supply for drivers.
3. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient via below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.
4. The PCB wire length of SPI bus should be equal and there should be appropriate shielding for clock and data wire to avoid interference between signals.

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

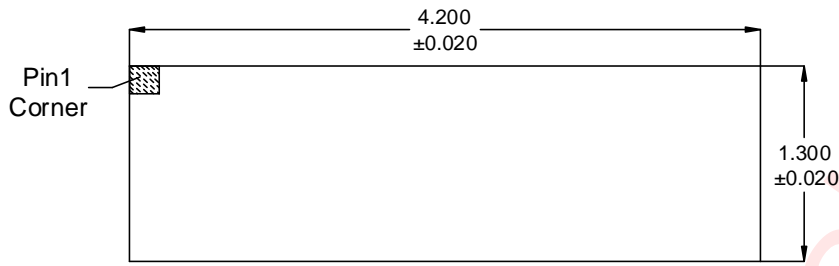


DIMENSIONS AND PIN1 ORIENTATION

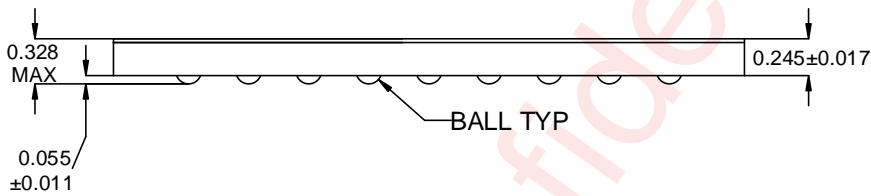
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	1.40	4.44	0.40	2.00	8.00	4.00	12.00	Q2

All dimensions are nominal

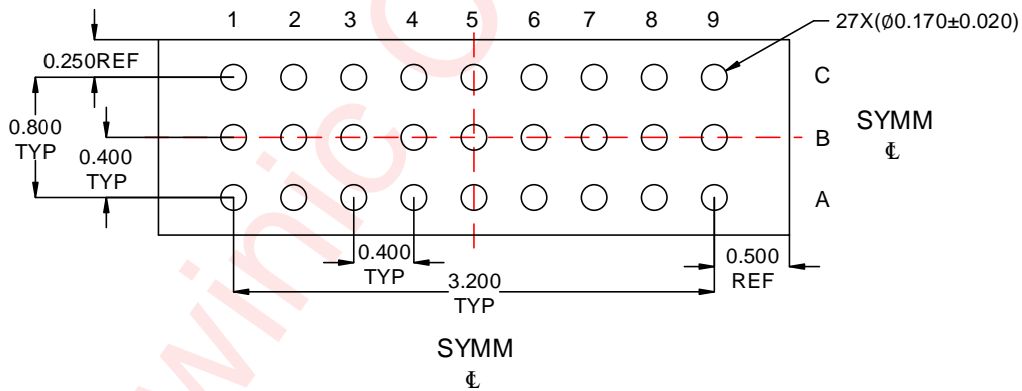
Package Description



Top View



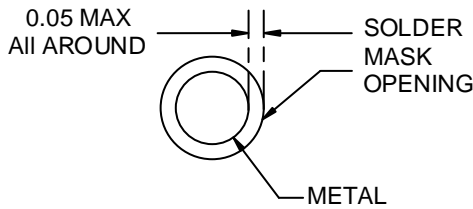
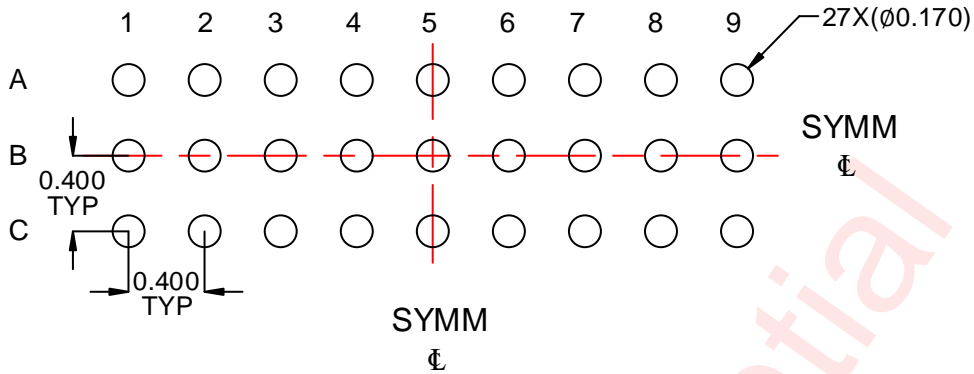
Side View



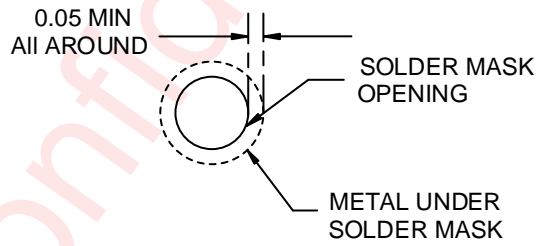
Bottom View

Unit: mm

Land Pattern Data



NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0.1	MAR 2020	Officially Released
V1.0.2	OCT 2020	Change the slave address of I2C
V1.0.3	JAN 2021	Modify the description of power-up timing and fix some mistype
V1.0.4	DEC 2022	Modify the description of power-up timing
V1.0.5	JAN 2024	Modify the description of power-up timing, fix some mistype, typical application circuit, XY H-bridge dac resolution and add description of pull-up voltage for I2C, H-bridge driver current direction, detailed description of the Gain and PCB layout. Delete the maximum of UVLO.

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