NEC

MOS Integrated Circuit

V850ES/JG2

32-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The V850ES/JG2 is a 32-bit single chip microcontroller of the V850ES series. 32-bit CPU, ROM, RAM, timer/counters, serial interface, A/D converter, D/A converter and so on are integrated on a single chip.

FEATURES

- V850ES core, 32-bit RISC architecture
- Instruction execution time: 50ns(min.) @20MHz , Integrated PLL(x4) circuit
- On-chip high-capacity ROM , RAM

Type / Part Number	Program Memory (Flash Memory Size)	Data Memory (RAM Size)
μPD70F3715	**128KB**	**12KB**
μPD70F3716	**256KB**	**24KB**
μPD70F3717	**384KB**	**32KB**
μPD70F3718	**512KB**	**40KB**
μPD70F3719	**640KB**	**48KB**

- Timer:
  - 16-bit timer(Type TMP) : 6 channels
  - 16-bit timer(Type TMQ) : 1 channel
  - 16-bit timer(Type TMM) : 1 channel
  - Watch timer : 1 channel
  - Watchdog timer : 1 channel
- Real-time output port : 6 bits x 1 channel
- Serial interface :
  - UART/I^2C : 2 channels
  - UART/CSI : 1 channel
  - CSI/I^2C : 1 channel
  - CSI : 3 channels
- A/D converter : 10-bit resolution : 12channels
- D/A converter : 8-bit resolution : 2channels
- DMA controller : 4 channels
- On-chip debug function : JTAG interface (N-wire type)
- Operation Voltage :
  - 2.85V to 3.6V : 20MHz max. (OSC=5MHz x4)
- Package : 100-pin QFP (14 x 14mm, 0.5mm pitch)
  - 100-pin QFP (14 x 20mm, 0.65mm pitch)

Please note: The information in this document is subject to change without notice

Function Table

Device name		V850ES/JG2					V850ES/JJ2
		μPD 70F3715	μPD 70F3716	μPD 70F3717	μPD 70F3718	μPD 70F3719	
CPU core		V850ES					V850ES
CPU performance		29MIPS(@20MHz)					29MIPS(@20MHz)
Internal flash memory		128KB	256KB	384KB	512KB	640KB	128/256/384/512/640KB
Internal RAM		12KB	24KB	32KB	40KB	48KB	12/24/32/40/48KB
External bus interface	Bus type	Multiplexed/separate					Multiplexed/separate
	Address bus	22 bits					24 bits
	Data bus	8/16 bits					8/16 bits
	Chip select signal	-					4
Interrupt sources	Internal	48					61
	External	9					10
Timer/counter		16-bit interval timer(TMM) x 1 ch 16-bit timer/event counter(TMP) x 6 ch 16-bit timer/event counter(TMQ) x 1 ch Watch timer x 1 ch Watchdog timer x 1 ch					16-bit interval timer(TMM) x 1 ch 16-bit timer/event counter(TMP)x9ch 16-bit timer/event counter(TMQ)x1ch Watch timer x 1 ch Watchdog timer x 1 ch
Serial interface		CSI x 3 ch UART(LIN compatible)/CSI x 1 ch CSI/I^2C x 1 ch UART(LIN compatible)/I^2C x 2 ch					CSI x 4 ch UART(LIN compatible)/CSI x 1 ch CSI/I^2C x 1 ch UART(LIN compatible)/I^2C x 2 ch UART(LIN compatible) x 1 ch
A/D converter		10-bit x 12 ch					10-bit x 16 ch
D/A converter		8-bit x 2 ch					8-bit x 2 ch
DMA controller		4 ch					4 ch
Ports	I/O	84					128
Debug control unit		Provided (RUN/break)					Provided (RUN/break)
Other peripheral functions		Real-time output 6-bit x 1 ch Key interrupt LVI/clock monitor					Real-time output 6-bit x 2 ch Key interrupt LVI/clock monitor
Operating frequency		When using main clock : 2.5 to 20MHz When using subclock : 32.768kHz Internal oscillation clock : 200kHz					When using main clock : 2.5 to 20MHz When using subclock : 32.768kHz Internal oscillation clock : 200kHz
Power supply voltage		2.85 to 3.6V (@20MHz)					2.85 to 3.6V (@20MHz)
Package		100-pin LQFP (14 x 14 mm) 100-pin QFP (14 x 20mm)					144-pin LQFP (20 x 20 mm)
Operating ambient temperature		-40°C to +85°C					-40°C to +85°C

Serial interface functions overview

Function	Overviw
CSI	➢ Transfer rate: 8Mbps to 4.9kbps (fxx=20MHz, using internal clock) ➢ Master mode and slave mode selectable ➢ 8-bit to 16-bit transfer, 3-wire serial interface ➢ interrupt request signals (INTCBnT, INTCBnR) ➢ Serial clock and data phase switchable ➢ Transfer data length selectable in 1-bit units between 8 and 16 bits ➢ Transfer data MSB-first/LSB-first swichable ➢ 3-wire transfer SOBn : Serial data output SIBn : Serial data input SCKBn : Serial clock input/output Transmission mode, reception mode, and transmission/reception mode specifiable **Remark** n = 0 to 4
UART	➢ Transfer rate : 300 bps to 312.5 kbps (using internal system clock of 20MHz and dedicated baud rate generator) ➢ Full-duplex communication: Internal UARTAn receive data register(UAnRX) Internal UARTAn transmit data register(UAnTX) ➢ 2-pin configuration: TXDAn: Transmit data output pin RXDAn: Receive data input pin ➢ Reception error output function ✓ Parity error ✓ Framing error ✓ Overrun error ➢ Interrupt sources: 2 ✓ Reception complete interrupt(INTUAnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status. ✓ Transmission enable interrupt(INTUAnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status. ➢ Character length: 7, 8 bits ➢ Parity function: Odd, even, 0, none ➢ Transmission stop bit: 1, 2 bits ➢ On-chip dedicated baud rate generator ➢ MSB-/LSB-first transfer selectable ➢ Transmit/receive data inverted input/output possible ➢ SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format ✓ 13 to 20 bits selectable for the SBF transmission ✓ Recognition of 11 bits or more possible for SBF reception ✓ SBF reception flag provided **Remark** n = 0 to 2
I^2C	➢ Operation stopped mode In this mode, serial transfers are not performed, thus enabling a reduction in power consumption. ➢ I^2C bus mode (multimaster support) This mode is used for 8-bit data transfers with several devices via two lines: a serial clock pin (SCL0n) and a serial data bus pin (SDA0n). This mode complies with the I^2C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device via the serial data bus. The slave device automatically detects the received statuses and data by hardware. This function can simplify the part of an application program that controls the I^2C bus. **Remark** n = 0 to 2

Timer functions overview

Function	Overviw
16-bit interval timer (TMM)	➢ Interval function ➢ 8 clocks selectable ➢ 16-bit counter x 1 (The 16-bit counter cannot be read during timer count operation.) ➢ Compare register x 1 (The compare register cannot be written during timer counter operation.) ➢ Compare match interrupt x 1
16-bit timer/event counter (TMP)	➢ Clock selection: 8 ways ➢ Capture/trigger input pins: 2 ➢ External event count input pins: 1 ➢ External trigger input pins: 1 ➢ Timer/counters: 1 ➢ Capture/compare registers: 2 ➢ Capture/compare match interrupt request signals: 2 ➢ Timer output pins: 2 ➢ TMPn has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output ✓ One-shot pulse output ✓ PWM output ✓ Free-running timer ✓ Pulse width measurement **Remark** n = 0 to 5
16-bit timer/event counter (TMQ)	➢ Clock selection: 8 ways ➢ Capture/trigger input pins: 4 ➢ External event count input pins: 1 ➢ External trigger input pins: 1 ➢ Timer/counters: 1 ➢ Capture/compare registers: 4 ➢ Capture/compare match interrupt request signals: 4 ➢ Timer output pins: 4 ➢ TMQ0 has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output ✓ One-shot pulse output ✓ PWM output ✓ Free-running timer ✓ Pulse width measurement
Watch timer	➢ Watch timer An interrupt request signal (INTWT) is generated at intervals of 0.5 or 0.25 seconds by using the main clock or subclock. ➢ Interval timer An interrupt request signal (INTWTI) is generated at set intervals. **Remark** The watch timer and interval timer functions can be used at the same time.
Watchdog timer 2	➢ Default-start watchdog timer ✓ Reset mode: Reset operation upon overflow of watchdog timer 2 (generation of WDT2RES signal) ✓ Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer 2 (generation of INTWDT2 signal) ➢ Input selectable from main clock, internal oscillation clock, and subclock as the source clock.

Other functions overview(1/2)

Function	Overview
A/D converter	➢ 10-bit resolution ➢ 12 channels ➢ Successive approximation method ➢ Operating voltage: AV_{REF0} = 3.0 to 3.6 V ➢ Analog input voltage: 0 V to AV_{REF0} ➢ The following functions are provided as operation modes. ✓ Continuous select mode ✓ Continuous scan mode ✓ One-shot select mode ✓ One-shot scan mode ➢ The following functions are provided as trigger modes. ✓ Software trigger mode ✓ External trigger mode (external, 1) ✓ Timer trigger mode ➢ Power-fail monitor function (conversion result compare function)
D/A converter	➢ 8-bit resolution x 2 channels (DA0CS0, DA0CS1) ➢ R-2R ladder method ➢ Settling time: 3μs max. (when AV_{REF1} is 3.0 to 3.6 V and external load is 20 pF) ➢ Analog output voltage: AV_{REF1} x m/256 (m = 0 to 255; value set to DA0CSn register) ➢ Operation modes: Normal mode, real-time output mode **Remark** n = 0, 1
DMA	➢ 4 independent DMA channels ➢ Transfer unit: 8/16 bits ➢ Maximum transfer count: 65,536 (2^{16}) ➢ Transfer type: Two-cycle transfer ➢ Transfer mode: Single transfer mode ➢ Transfer requests ✓ Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, A/D converter) or interrupts from external input pin ✓ Request by software trigger ➢ Transfer targets ✓ Internal RAM ↔ Peripheral I/O ✓ Peripheral I/O ↔ Peripheral I/O ✓ Internal RAM ↔ External memory ✓ External memory ↔ Peripheral I/O ✓ External memory ↔ External memory
Interrupt/exception Processing	➢ Interrupts ✓ Non-maskable interrupts: 2 sources ✓ Maskable interrupts: External: 8, Internal: 47 sources ✓ 8 levels of programmable priorities (maskable interrupts) ✓ Multiple interrupt control according to priority ✓ Masks can be specified for each maskable interrupt request. ✓ Noise elimination, edge detection, and valid edge specification for external interrupt request signals. ➢ Exceptions ✓ Software exceptions: 32 sources ✓ Exception trap: 2 sources (illegal op code exception and debug trap)

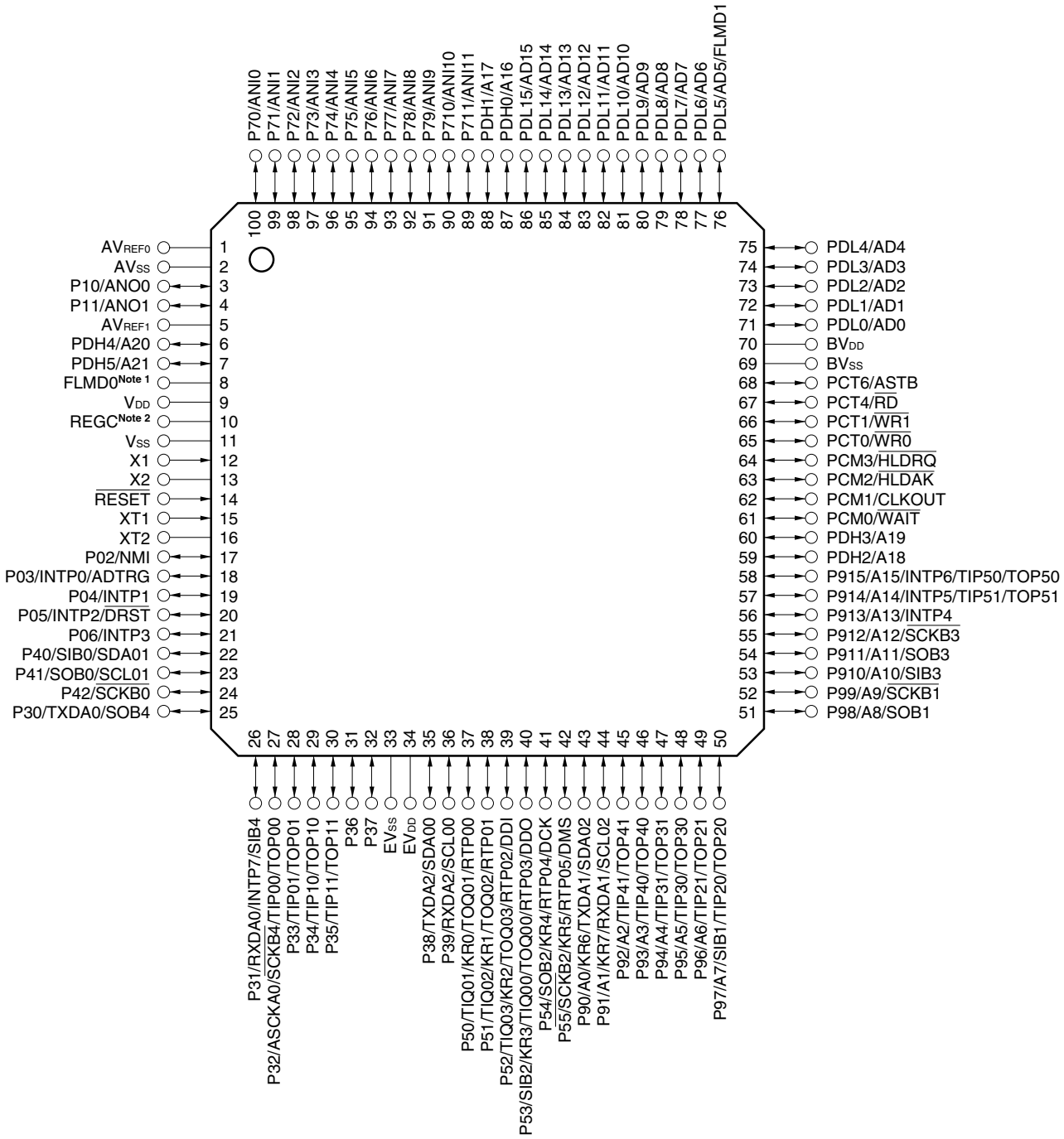
Other functions overview(2/2)

Function	Overview
Key interrupt	➢ A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7) by setting the KRM register.
Standby	➢ The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. ✓ HALT mode: Mode in which only the operating clock of the CPU is stopped ✓ IDLE1 mode: Mode in which all the operations of the internal circuits except the oscillator, PLL, and flash memory are stopped ✓ IDLE2 mode: Mode in which all the internal operations of the chip except the oscillator are stopped ✓ STOP mode: Mode in which all the internal operations of the chip except the subclock oscillator are stopped ✓ Subclock operation mode: Mode in which the subclock is used as the internal system clock ✓ Sub-IDLE mode: Mode in which all the internal operations of the chip except the oscillator are stopped, in the subclock operation mode
Bus control	➢ Output is selectable from a multiplexed bus with a minimum of 3 bus cycles and a separate bus with a minimum of 2 bus cycles. ➢ 8-bit/16-bit data bus selectable ➢ Wait function ✓ Programmable wait function of up to 7 states ✓ External wait function using $\overline{\text{WAIT}}$ pin ➢ Idle state function ➢ Bus hold function ➢ Up to 4 MB of physical memory connectable (of which 1 MB is internal ROM space) ➢ The bus can be controlled at a voltage that is different from the operating voltage when $BV_{DD} \leq EV_{DD} = V_{DD}$. However, in separate bus mode or when the A20 and A21 pins are used, set $BV_{DD} = EV_{DD} = V_{DD}$.
Clock monitor	➢ The clock monitor samples the main clock by using the internal oscillation clock and generates a reset request signal when oscillation of the main clock is stopped. ➢ Once the operation of the clock monitor has been enabled by an operation enable flag, it cannot be cleared to 0 by any means other than reset. ➢ When a reset by the clock monitor occurs, the RESF.CLMRF bit is set. ➢ The clock monitor automatically stops under the following conditions. ✓ During oscillation stabilization time after STOP mode is released ✓ When the main clock is stopped (from when the PCC.MCK bit = 1 during subclock operation, until the PCC.CLS bit = 0 during main clock operation) ✓ When the sampling clock (internal oscillation clock) is stopped ✓ When the CPU operates with the internal oscillation clock
Low-voltage Detector (LVI)	➢ Compares the supply voltage (V_{DD}) and detected voltage (V_{LVI}) and generates an internal interrupt signal or internal reset signal when $V_{DD} < V_{LVI}$. ➢ The level of the supply voltage to be detected can be changed by software (in two steps). ➢ Interrupt or reset signal can be selected by software. ➢ Can operate in STOP mode.

Pin Configuration (Top View)

100-pin plastic LQFP (fine pitch) (14 x 14)

μPD70F3715GC-8EA-A
μPD70F3716GC-8EA-A
μPD70F3717GC-8EA-A
μPD70F3718GC-8EA-A
μPD70F3719GC-8EA-A



Notes **1.** FLMD0 pin: Connect to V_{SS} in normal operation mode.

2. Connect the REGC pin to V_{SS} via a 4.7 ⌈F capacitor.

Caution Make EV_{DD} the same potential as V_{DD}.

BV_{DD} can be used when $V_{DD} = EV_{DD} \geq BV_{DD}$.

100-pin plastic QFP (14 x 20)

μPD70F3715GF-JBT-A

μPD70F3716GF-JBT-A

μPD70F3717GF-JBT-A

(1) Port pins

(1/3)

Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
P02	19	17	I/O	Port 0 5-bit I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units. 5 V tolerant.	NMI
P03	20	18			INTP0/ADTRG
P04	21	19			INTP1
P05	22	20			INTP2/$\overline{\text{DRST}}$
P06	23	21			INTP3
P10	5	3	I/O	Port 1 2-bit I/O port Input/output can be specified in 1-bit units.	ANO0
P11	6	4			ANO1
P30	27	25	I/O	Port 3 10-bit I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units. 5 V tolerant.	TXDA0/SOB4
P31	28	26			RXDA0/INTP7/SIB4
P32	29	27			ASCKA0/$\overline{\text{SCKB4}}$/TIP00/TOP00
P33	30	28			TIP01/TOP01
P34	31	29			TIP10/TOP10
P35	32	30			TIP11/TOP11
P36	33	31			
P37	34	32			
P38	37	35			TXDA2/SDA00
P39	38	36			RXDA2/SCL00
P40	24	22	I/O	Port 4 3-bit I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units. 5 V tolerant.	SIB0/SDA01
P41	25	23			SOB0/SCL01
P42	26	24			$\overline{\text{SCKB0}}$
P50	39	37	I/O	Port 5 6-bit I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units. 5 V tolerant.	TIQ01/KR0/TOQ01/RTP00
P51	40	38			TIQ02/KR1/TOQ02/RTP01
P52	41	39			TIQ03/KR2/TOQ03/RTP02/DDI
P53	42	40			SIB2/KR3/TIQ00/TOQ00/RTP03/DDO
P54	43	41			SOB2/KR4/RTP04/DCK
P55	44	42			$\overline{\text{SCKB2}}$/KR5/RTP05/DMS

Remark GF: 100-pin plastic QFP (14 × 20)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

(2/3)

Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
P70	2	100	I/O	Port 7 12-bit I/O port Input/output can be specified in 1-bit units.	ANI0
P71	1	99			ANI1
P72	100	98			ANI2
P73	99	97			ANI3
P74	98	96			ANI4
P75	97	95			ANI5
P76	96	94			ANI6
P77	95	93			ANI7
P78	94	92			ANI8
P79	93	91			ANI9
P710	92	90			ANI10
P711	91	89			ANI11
P90	45	43	I/O	Port 9 16-bit I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units. 5 V tolerant.	A0/KR6/TXDA1/SDA02
P91	46	44			A1/KR7/RXDA1/SCL02
P92	47	45			A2/TIP41/TOP41
P93	48	46			A3/TIP40/TOP40
P94	49	47			A4/TIP31/TOP31
P95	50	48			A5/TIP30/TOP30
P96	51	49			A6/TIP21/TOP21
P97	52	50			A7/SIB1/TIP20/TOP20
P98	53	51			A8/SOB1
P99	54	52			A9/$\overline{\text{SCKB1}}$
P910	55	53			A10/SIB3
P911	56	54			A11/SOB3
P912	57	55			A12/$\overline{\text{SCKB3}}$
P913	58	56			A13/INTP4
P914	59	57			A14/INTP5/TIP51/TOP51
P915	60	58			A15/INTP6/TIP50/TOP50

Remark GF: 100-pin plastic QFP (14 × 20)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

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Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
PCM0	63	61	I/O	Port CM 4-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1	64	62			CLKOUT
PCM2	65	63			$\overline{\text{HLDAK}}$
PCM3	66	64			$\overline{\text{HLDRQ}}$
PCT0	67	65	I/O	Port CT 4-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WR0}}$
PCT1	68	66			$\overline{\text{WR1}}$
PCT4	69	67			$\overline{\text{RD}}$
PCT6	70	68			ASTB
PDH0	89	87	I/O	Port DH 6-bit I/O port Input/output can be specified in 1-bit units.	A16
PDH1	90	88			A17
PDH2	61	59			A18
PDH3	62	60			A19
PDH4	8	6			A20
PDH5	9	7			A21
PDL0	73	71	I/O	Port DL 16-bit I/O port Input/output can be specified in 1-bit units.	AD0
PDL1	74	72			AD1
PDL2	75	73			AD2
PDL3	76	74			AD3
PDL4	77	75			AD4
PDL5	78	76			AD5/FLMD1
PDL6	79	77			AD6
PDL7	80	78			AD7
PDL8	81	79			AD8
PDL9	82	80			AD9
PDL10	83	81			AD10
PDL11	84	82			AD11
PDL12	85	83			AD12
PDL13	86	84			AD13
PDL14	87	85			AD14
PDL15	88	86			AD15

Remark GF: 100-pin plastic QFP (14 × 20)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

(2) Non-port pins

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Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
A0	45	43	Output	Address bus for external memory (when using separate bus) N-ch open-drain output selectable. 5 V tolerant.	P90/KR6/TXDA1/SDA02
A1	46	44			P91/KR7/RXDA1/SCL02
A2	47	45			P92/TIP41/TOP41
A3	48	46			P93/TIP40/TOP40
A4	49	47			P94/TIP31/TOP31
A5	50	48			P95/TIP30/TOP30
A6	51	49			P96/TIP21/TOP21
A7	52	50			P97/SIB1/TIP20/TOP20
A8	53	51			P98/SOB1
A9	54	52			P99/SCKB1
A10	55	53			P910/SIB3
A11	56	54			P911/SOB3
A12	57	55			P912/$\overline{\text{SCKB3}}$
A13	58	56			P913/INTP4
A14	59	57			P914/INTP5/TIP51/TOP51
A15	60	58			P915/INTP6/TIP50/TOP50
A16	89	87	Output	Address bus for external memory	PDH0
A17	90	88			PDH1
A18	61	59			PDH2
A19	62	60			PDH3
A20	8	6			PDH4
A21	9	7			PDH5
AD0	73	71	I/O	Address bus/data bus for external memory	PDL0
AD1	74	72			PDL1
AD2	75	73			PDL2
AD3	76	74			PDL3
AD4	77	75			PDL4
AD5	78	76			PDL5/FLMD1
AD6	79	77			PDL6
AD7	80	78			PDL7
AD8	81	79			PDL8
AD9	82	80			PDL9
AD10	83	81			PDL10
AD11	84	82			PDL11
AD12	85	83			PDL12
AD13	86	84			PDL13
AD14	87	85			PDL14
AD15	88	86			PDL15

Remark GF: 100-pin plastic QFP (14 × 20)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

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Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
ADTRG	20	18	Input	A/D converter external trigger input. 5 V tolerant.	P03/INTP0
ANI0	2	100	Input	Analog voltage input for A/D converter	P70
ANI1	1	99			P71
ANI2	100	98			P72
ANI3	99	97			P73
ANI4	98	96			P74
ANI5	97	95			P75
ANI6	96	94			P76
ANI7	95	93			P77
ANI8	94	92			P78
ANI9	93	91			P79
ANI10	92	90			P710
ANI11	91	89			P711
ANO0	5	3	Output	Analog voltage output for D/A converter	P10
ANO1	6	4			P11
ASCKA0	29	27	Input	UARTA0 baud rate clock input. 5 V tolerant.	P32/$\overline{\text{SCKB4}}$/TIP00/TOP00
ASTB	70	68	Output	Address strobe signal output for external memory	PCT6
AV_{REF0}	3	1	–	Reference voltage input for A/D converter/positive power supply for port 7	–
AV_{REF1}	7	5		Reference voltage input for D/A converter/positive power supply for port 1	–
AV_{SS}	4	2	–	Ground potential for A/D and D/A converters (same potential as V_{SS})	–
BV_{DD}	72	70	–	Positive power supply pin for bus interface and alternate-function ports	–
BV_{SS}	71	69	–	Ground potential for bus interface and alternate-function ports	–
CLKOUT	64	62	Output	Internal system clock output	PCM1
DCK	43	41	Input	Debug clock input. 5 V tolerant.	P54/SOB2/KR4/RTP04
DDI	41	39	Input	Debug data input. 5 V tolerant.	P52/TIQ03/KR2/TOQ03/RTP02
DDO	42	40	Output	Debug data output. N-ch open-drain output selectable. 5 V tolerant.	P53/SIB2/KR3/TIQ00/TOQ00/RTP03
DMS	44	42	Input	Debug mode select input. 5 V tolerant.	P55/$\overline{\text{SCKB2}}$/KR5/RTP05
$\overline{\text{DRST}}$	22	20	Input	Debug reset input. 5 V tolerant.	P05/INTP2
EV_{DD}	36	34	–	Positive power supply for external (same potential as V_{DD})	–
EV_{SS}	35	33	–	Ground potential for external (same potential as V_{SS})	–
FLMD0	10	8	Input	Flash memory programming mode setting pin	–
FLMD1	78	76			PDL5/AD5

Remark GF: 100-pin plastic QFP (14 × 20)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

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Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
$\overline{\text{HLDAK}}$	65	63	Output	Bus hold acknowledge output	PCM2
$\overline{\text{HLDRQ}}$	66	64	Input	Bus hold request input	PCM3
INTP0	20	18	Input	External interrupt request input (maskable, analog noise elimination). Analog noise elimination or digital noise elimination selectable for INTP3 pin. 5 V tolerant.	P03/ADTRG
INTP1	21	19			P04
INTP2	22	20			P05/$\overline{\text{DRST}}$
INTP3	23	21			P06
INTP4	58	56			P913/A13
INTP5	59	57			P914/A14/TIP51/TOP51
INTP6	60	58			P915/A15/TIP50/TOP50
INTP7	28	26			P31/RXDA0/SIB4
KR0	39	37	Input	Key interrupt input (on-chip analog noise eliminator). 5 V tolerant.	P50/TIQ01/TOQ01/RTP00
KR1	40	38			P51/TIQ02/TOQ02/RTP01
KR2	41	39			P52/TIQ03/TOQ03/ RTP02/DDI
KR3	42	40			P53/SIB2/TIQ00/TOQ00/ RTP03/DDO
KR4	43	41			P54/SOB2/RTP04/DCK
KR5	44	42			P55/$\overline{\text{SCKB2}}$/RTP05/DMS
KR6	45	43			P90/A0/TXDA1/SDA02
KR7	46	44			P91/A1/RXDA1/SCL02
NMI	19	17	Input	External interrupt input (non-maskable, analog noise elimination). 5 V tolerant.	P02
$\overline{\text{RD}}$	69	67	Output	Read strobe signal output for external memory	PCT4
REGC	12	10	–	Connection of regulator output stabilization capacitance	–
$\overline{\text{RESET}}$	16	14	Input	System reset input	–
RTP00	39	37	Output	Real-time output port. N-ch open-drain output selectable. 5 V tolerant.	P50/TIQ01/KR0/TOQ01
RTP01	40	38			P51/TIQ02/KR1/TOQ02
RTP02	41	39			P52/TIQ03/KR2/TOQ03/DDI
RTP03	42	40			P53/SIB2/KR3/TIQ00/TOQ00/ DDO
RTP04	43	41			P54/SOB2/KR4/DCK
RTP05	44	42			P55/$\overline{\text{SCKB2}}$/KR5/DMS

Remark GF: 100-pin plastic QFP (14 × 20)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

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Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
RXDA0	28	26	Input	Serial receive data input (UARTA0 to UARTA2) 5 V tolerant.	P31/INTP7/SIB4
RXDA1	46	44			P91/A1/KR7/SCL02
RXDA2	38	36			P39/SCL00
$\overline{\text{SCKB0}}$	26	24	I/O	Serial clock I/O (CSIB0 to CSIB4) N-ch open-drain output selectable. 5 V tolerant.	P42
$\overline{\text{SCKB1}}$	54	52			P99/A9
$\overline{\text{SCKB2}}$	44	42			P55/KR5/RTP05/DMS
$\overline{\text{SCKB3}}$	57	55			P912/A12
$\overline{\text{SCKB4}}$	29	27			P32/ASCKA0/TIP00/TOP00
SCL00	38	36	I/O	Serial clock I/O (I^2C00 to I^2C02) N-ch open-drain output selectable. 5 V tolerant.	P39/RXDA2
SCL01	25	23			P41/SOB0
SCL02	46	44			P91/A1/KR7/RXDA1
SDA00	37	35	I/O	Serial transmit/receive data I/O (I^2C00 to I^2C02) N-ch open-drain output selectable. 5 V tolerant.	P38/TXDA2
SDA01	24	22			P40/SIB0
SDA02	45	43			P90/A0/KR6/TXDA1
SIB0	24	22	Input	Serial receive data input (CSIB0 to CSIB4) 5 V tolerant.	P40/SDA01
SIB1	52	50			P97/A7/TIP20/TOP20
SIB2	42	40			P53/KR3/TIQ00/TOQ00/ RTP03/DDO
SIB3	55	53			P910/A10
SIB4	28	26			P31/RXDA0/INTP7
SOB0	25	23	Output	Serial transmit data output (CSIB0 to CSIB4) N-ch open-drain output selectable. 5 V tolerant.	P41/SCL01
SOB1	53	51			P98/A8
SOB2	43	41			P54/KR4/RTP04/DCK
SOB3	56	54			P911/A11
SOB4	27	25			P30/TXDA0
TIP00	29	27	Input	External event count input/capture trigger input/external trigger input (TMP0). 5 V tolerant.	P32/ASCKA0/$\overline{\text{SCKB4}}$/TOP00
TIP01	30	28		Capture trigger input (TMP0). 5 V tolerant.	P33/TOP01
TIP10	31	29		External event count input/capture trigger input/external trigger input (TMP1). 5 V tolerant.	P34/TOP10
TIP11	32	30		Capture trigger input (TMP1). 5 V tolerant.	P35/TOP11
TIP20	52	50		External event count input/capture trigger input/external trigger input (TMP2). 5 V tolerant.	P97/A7/SIB1/TOP20
TIP21	51	49		Capture trigger input (TMP2). 5 V tolerant.	P96/A6/TOP21
TIP30	50	48		External event count input/capture trigger input/external trigger input (TMP3). 5 V tolerant.	P95/A5/TOP30
TIP31	49	47		Capture trigger input (TMP3). 5 V tolerant.	P94/A4/TOP31
TIP40	48	46		External event count input/capture trigger input/external trigger input (TMP4). 5 V tolerant.	P93/A3/TOP40
TIP41	47	45		Capture trigger input (TMP4). 5 V tolerant.	P92/A2/TOP41

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GC: 100-pin plastic LQFP (fine pitch) (14 × 14)

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Pin Name	Pin No.		I/O	Function	Alternate Function
	GF	GC			
TIP50	60	58	Input	External event count input/capture trigger input/external trigger input (TMP5). 5 V tolerant.	P915/A15/INTP6/TOP50
TIP51	59	57		Capture trigger input (TMP5). 5 V tolerant.	P914/A14/INTP5/TOP51
TIQ00	42	40	Input	External event count input/capture trigger input/external trigger input (TMQ0). 5 V tolerant.	P53/SIB2/KR3/TOQ00/RTP03/DDO
TIQ01	39	37		Capture trigger input (TMQ0). 5 V tolerant.	P50/KR0/TOQ01/RTP00
TIQ02	40	38			P51/KR1/TOQ02/RTP01
TIQ03	41	39			P52/KR2/TOQ03/RTP02/DDI
TOP00	29	27	Output	Timer output (TMP0) N-ch open-drain output selectable. 5 V tolerant.	P32/ASCKA0/$\overline{\text{SCKB4}}$/TIP00
TOP01	30	28			P33/TIP01
TOP10	31	29		Timer output (TMP1) N-ch open-drain output selectable. 5 V tolerant.	P34/TIP10
TOP11	32	30			P35/TIP11
TOP20	52	50		Timer output (TMP2) N-ch open-drain output selectable. 5 V tolerant.	P97/A7/SIB1/TIP20
TOP21	51	49			P96/A6/TIP21
TOP30	50	48		Timer output (TMP3) N-ch open-drain output selectable. 5 V tolerant.	P95/A5/TIP30
TOP31	49	47			P94/A4/TIP31
TOP40	48	46		Timer output (TMP4) N-ch open-drain output selectable. 5 V tolerant.	P93/A3/TIP40
TOP41	47	45			P92/A2/TIP41
TOP50	60	58		Timer output (TMP5) N-ch open-drain output selectable. 5 V tolerant.	P915/A15/INTP6/TIP50
TOP51	59	57			P914/A14/INTP5/TIP51
TOQ00	42	40	Output	Timer output (TMQ0) N-ch open-drain output selectable. 5 V tolerant.	P53/SIB2/KR3/TIQ00/RTP03/DDO
TOQ01	39	37			P50/TIQ01/KR0/RTP00
TOQ02	40	38			P51/RTP01/KR1/TIQ02
TOQ03	41	39			P52/TIQ03/KR2/RTP02/DDI
TXDA0	27	25	Output	Serial transmit data output (UARTA0 to UARTA2) N-ch open-drain output selectable. 5 V tolerant.	P30/SOB4
TXDA1	45	43			P90/A0/KR6/SDA02
TXDA2	37	35			P38/SDA00
V_{DD}	11	9	–	Positive power supply pin for internal	–
V_{SS}	13	11	–	Ground potential for internal	–
$\overline{\text{WAIT}}$	63	61	Input	External wait input	PCM0
$\overline{\text{WR0}}$	67	65	Output	Write strobe for external memory (lower 8 bits)	PCT0
$\overline{\text{WR1}}$	68	66		Write strove for external memory (higher 8 bits)	PCT1
X1	14	12	Input	Connection of resonator for main clock	–
X2	15	13	–		–
XT1	17	15	Input	Connection of resonator for subclock	–
XT2	18	16	–		–

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GC: 100-pin plastic LQFP (fine pitch) (14 × 14)