

18V, 15A Synchronous Boost Converter with Load Disconnect Control

Features

- Input Voltage Range :2.7V to 16V
- Output Voltage Range: 4.5 to 18V
- Two 7mΩ FETs Integrated
- Adjustable switching frequency up to 2MHz
- Programmable Cycle-by-Cycle Current Limit up to 15A
- Hiccup Short Protection with Load Disconnect Drive
- DCM Operation under light load
- Input Under-Voltage Lockout
- Output Over-Voltage Protection at fixed 21V
- Over-Temperature Protection
- FCQFN 3.5*3-13L Package

Applications

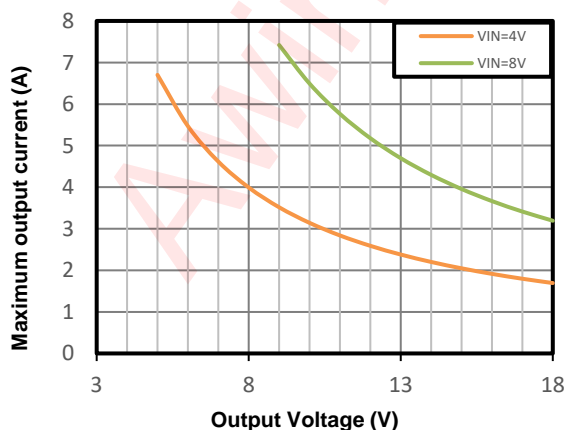
- Laptop and Desktop Computers
- Smart Speakers
- Tablets and Handhelds
- Wireless Speakers

General Description

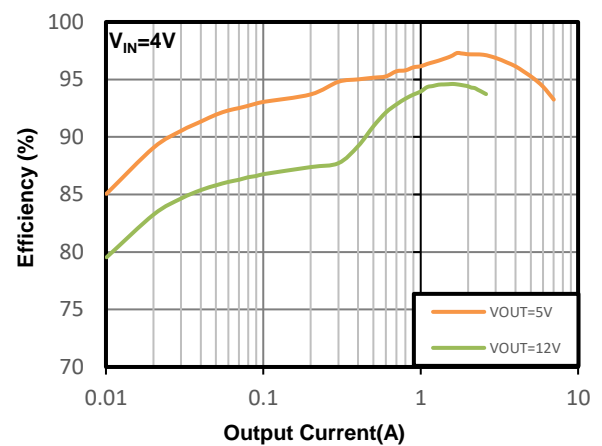
The AWP36220 is a 18-V synchronous Boost converter with the gate driver built-in for load disconnect. The AWP36220 integrates two low on resistance power FETs: A 7-mΩ switching FET and a 7-mΩ rectifier FET.

The AWP36220 uses the adaptive constant off time peak current mode control. AWP36220 has an internal feature to help improving light load efficiency. When output current is low, AWP36220 will go into DCM mode.

The AWP36220 could isolate the output from input side when shutdown. Once the output is shorted, it enters into the hiccup mode to lower the thermal stress and can recover automatically after the short condition releases. Additionally, the AWP36220 also has OVP and thermal protection to avoid the fault operation. The AWP36220 is in a 3.0 mm x 3.5 mm 13-pin FCQFN package with enhanced thermal dissipation.



Maximum Output Current vs Output Voltage



Efficiency vs Output Current

Typical Application Circuit

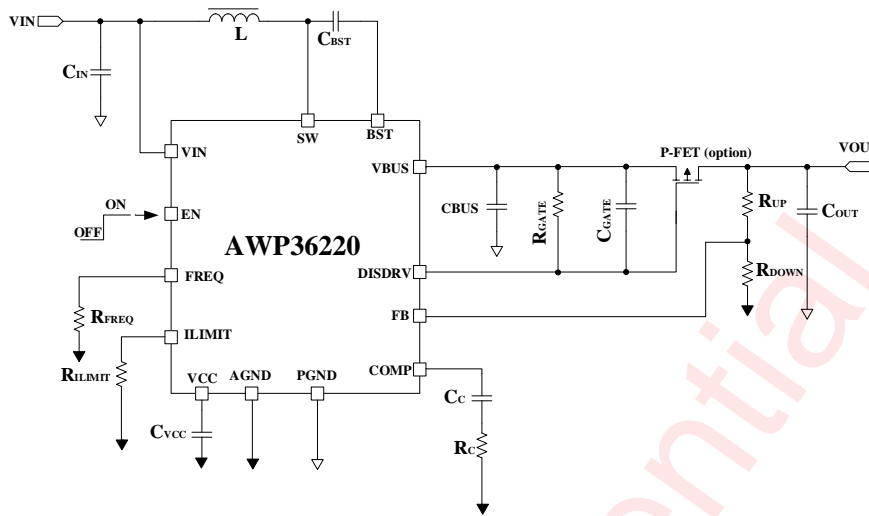


Figure 1 AWP36220 Typical Application Circuit

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Pin Configuration And Top Mark

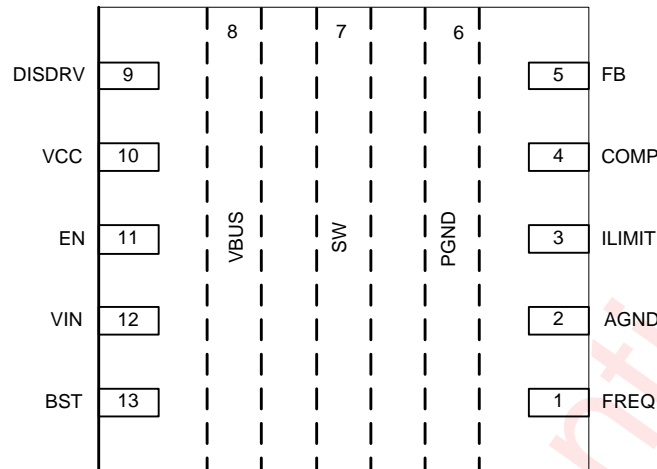


Figure 2 Pin Configuration

Pin Definition

No.	NAME	DESCRIPTION
1	FREQ	The switching frequency is programmed by a resistor between this pin and the AGND. This pin can't be float in application.
2	AGND	Analog ground.
3	ILIMIT	A Adjustable LSFET peak current limit. Connect a resistor to AGND.
4	COMP	Output of internal error amplifier, loop compensation network connect to COMP and AGND .COMP is a sensitive node, keep COMP away from SW and BST pin.
5	FB	Feedback Input. FB senses the output voltage, connect FB with a resistor divider connected between the output and ground. FB is a sensitive node, keep FB away from SW and BST pin.
6	PGND	Power ground. The source of LSFET connect to PGND internally.
7	SW	Power switching pin of boost converter, common node of LSFET drain and HSFET source. Connect the coil to this pin and power input.
8	VBUS	Output pin of boost converter, connect to the drain of HSFET internally.
9	DISDRV	A gate drive output for the external disconnect FET. Connect the DISDRV pin to the gate of the external FET. Leave it floating if not using the load disconnect function.
10	VCC	Output of internal regulator, A ceramic capacitor of more than 4.7 μ F is required between this pin and ground.
11	EN	Enable pin. Pull high to turn on the IC, don't float.
12	VIN	Input supply pin. Bypass Vin to GND with a large capacitor and at least another 0.1 μ F ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
13	BST	Boot strap pin Connect a 0.1 μ F or greater capacitor between SW and BST to power the high side gate driver.

Functional Block Diagram

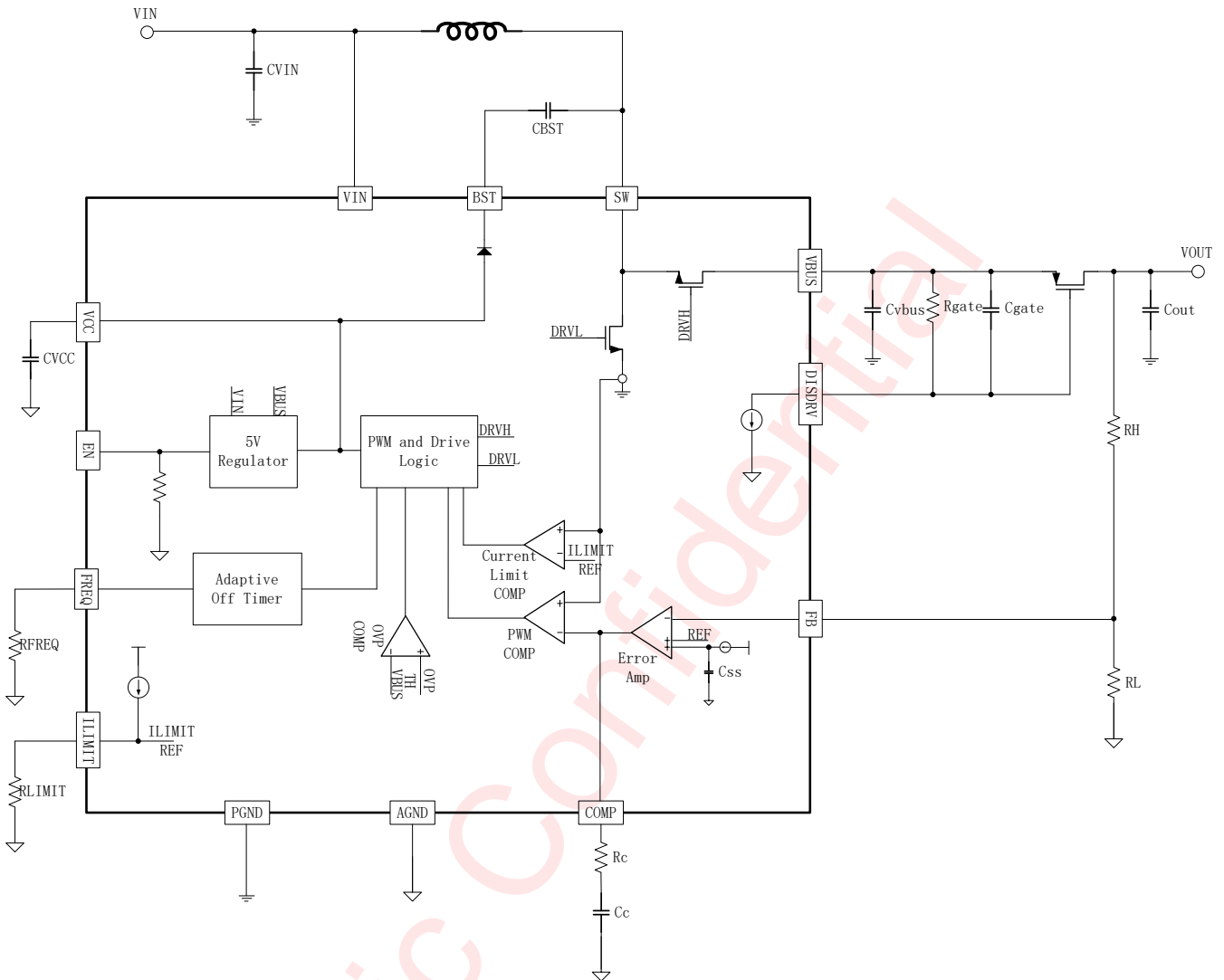


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWP36220QNR	-40°C~85°C	FCQFN 3.5*3-13L	AZJ3	MSL3	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings^(NOTE1)

PARAMETERS	RANGE
BST Voltage	-0.3V to SW+6.5V
V _{IN} , SW, DISDRV, V _{BUS} , EN voltage	-0.3V to 26V
FB, COMP, ILIMIT, VCC, FREQ voltage	-0.3V to 6.5V
Junction to ambient thermal resistance θ_{JA} ^(NOTE2)	50°C /W
Junction to case thermal resistance θ_{JC} ^(NOTE2)	10°C /W
Maximum operating junction temperature T _{JMAX}	150°C
Storage temperature T _{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD (Including CDM HBM)	
CDM	500V
HBM	2kV

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should be within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Measured on approximately 1" square of 1 oz copper.

Recommended Operating Conditions^(NOTE3)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IN}	Input Voltage	2.7		16	V
V _{OUT}	Output Voltage	4.5		18	V
V _{BST}	BST Voltage	0		SW+5	V
V _{EN}	EN Voltage	0		V _{IN}	V
V _{SW} , V _{DISDRV}	SW, DISDRV Voltage	0		V _{BUS}	V
Others	FB, COMP, ILIMIT, VCC, FREQ Voltage	0		5	V
T _A	Operating free-air temperature range	-40		85	°C

NOTE3: The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics

VIN = 2.7 V to 14 V and VOUT = 16 V, FSW=500 KHz, TJ = 25 °C , unless otherwise noted.

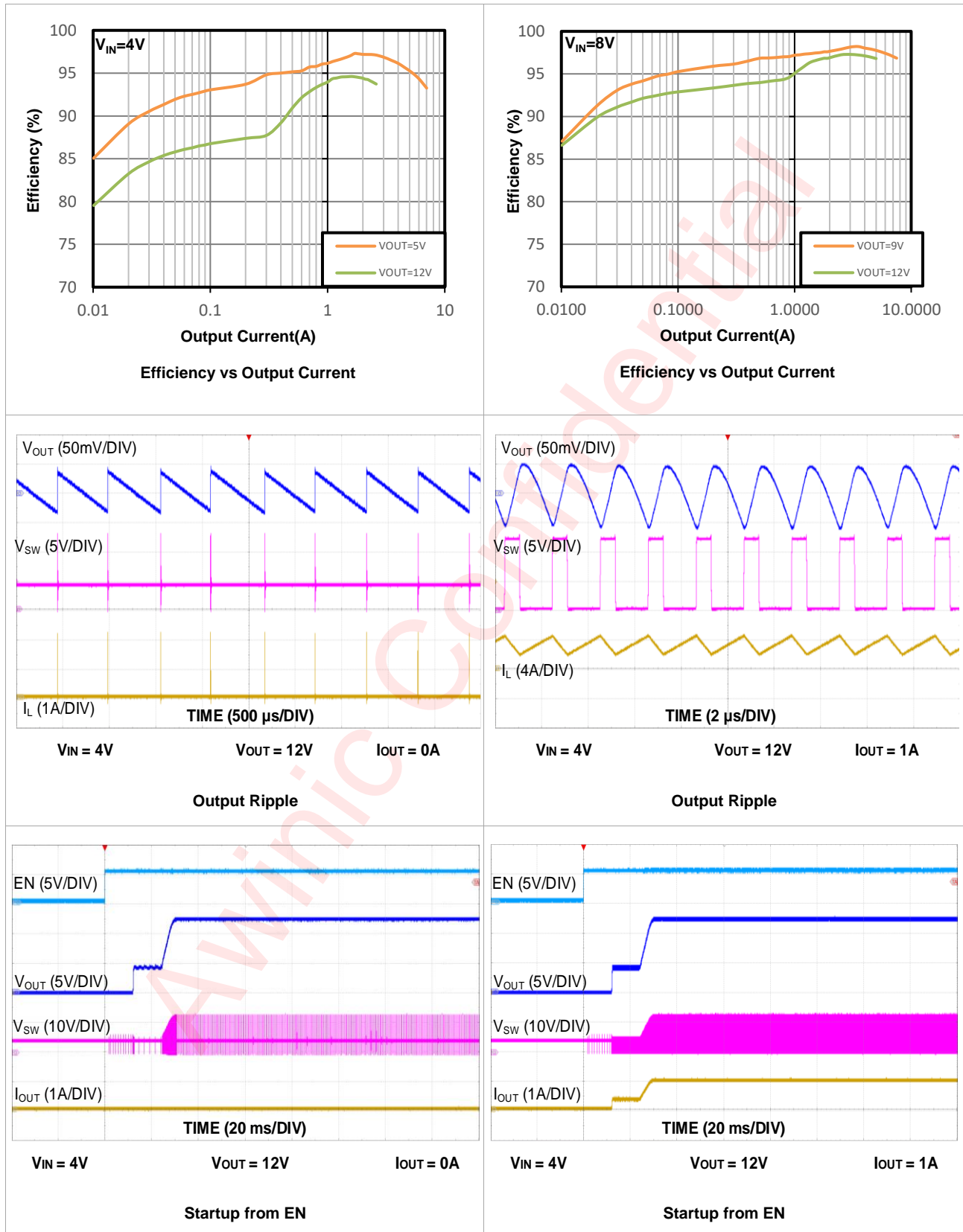
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN}	VIN operating range		2.7		16	V
V _{INUV}	VIN UVLO threshold voltage	when VIN < V _{INUV} , IC turn off, falling edge		2.35		V
V _{INUV_HYS}	VIN UVLO hysteresis voltage	after VIN > V _{INUV} + V _{INUV_HYS} , IC restore operation		0.35		V
V _{CC}	VCC regulation voltage	I _{VCC} =2mA, VIN=6V		5		V
V _{CCUV}	VCC UVLO threshold voltage	VCC falling edge		2.1		V
V _{CCUV_HYS}	VCC UVLO hysteresis voltage			0.8		V
I _{Q_VIN}	Standby current into VIN pin	VIN=EN=4V, VBUS=12V, FB=1.3V, no Ext. FET		23		μA
I _{Q_VBUS}	Standby current into VBUS pin	VIN=EN=4V, VBUS=12V, FB=1.3V, no Ext. FET		900		μA
I _{SD_VIN}	Shutdown current	EN=0V, VIN=4V		2		μA
V _{BUS}	VBUS operating range		4.5		18	V
V _{OVP}	VBUS OVP threshold voltage	Rising edge	20.5	21	21.5	V
V _{OVP_HYS}	VBUS OVP hysteresis voltage	Falling below VOVP		0.5		V
V _{FB}	Reference voltage at FB pin		1.182	1.2	1.218	V
I _{FB}	FB pin leakage current	FB=1.2V	-0.1		2.5	μA
G _M	Error amplifier trans-conductance(Note4)	FB=1.2V, COMP=1.5V		610		μS
I _{SOURCE}	COMP pin source current			54		μA
I _{SINK}	COMP pin sink current			54		μA
G _{CS}	COMP to current gain(Note4)			10		S
R _{ONLS}	Low side NFET on-resistance	I _{DS} =0.5A		7		mΩ
R _{ONHS}	High side NFET on-resistance	I _{DS} =0.5A		7		mΩ
I _{LKLS}	Low side FET leakage current	V _{SW} =18V		1		μA
I _{LKHS}	High side FET leakage current	VBUS=18V, V _{SW} =0V		1		μA

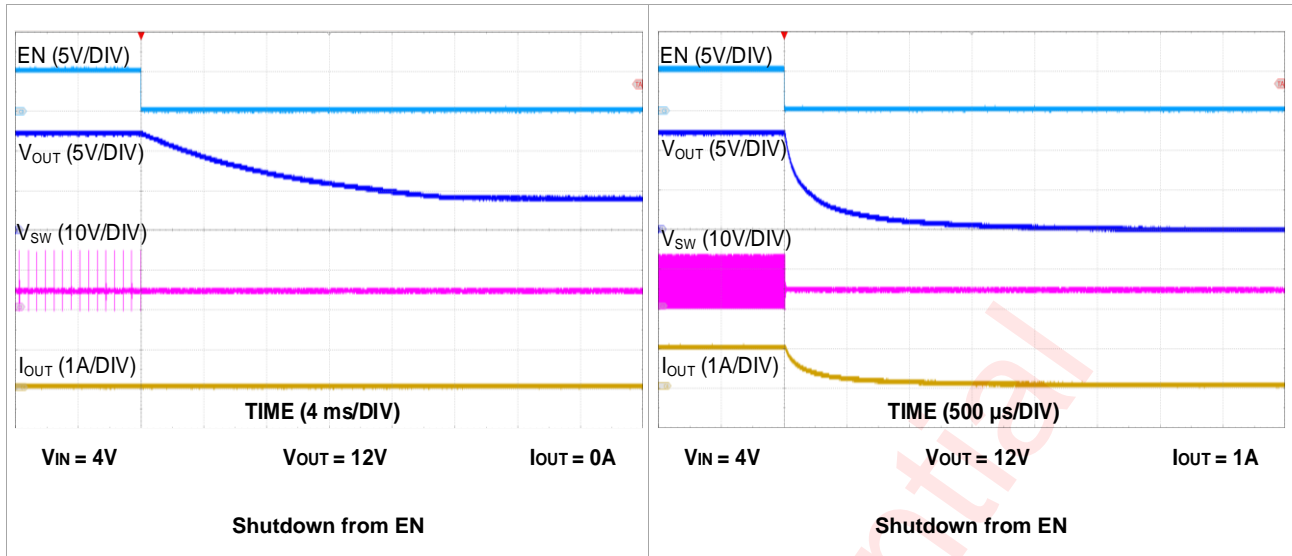
V _{BST}	High side driver supply voltage	BST-SW		5		V
V _{ILIM}	Reference voltage at ILIM			0.5		V
I _{LIM}	Peak LS NFET current limit	R _{LIMIT} =100k Ohm, I _{limit} =1M/RSET	8	10		A
		R _{LIMIT} =200k Ohm, I _{limit} =1M/RSET	4	5		A
f _{SW}	Switching frequency	R _{FREQ} =100k		476		kHz
t _{on_min}	Minimum LSFET on time(Note4)			300		ns
t _{off_min}	Minimum HSFET on time(Note4)			350		ns
V _{EN_H}	EN high threshold voltage	EN > V _{EN_H} , enable IC after t _{EN_ON}		1.2		V
V _{EN_L}	EN low threshold voltage	EN < V _{EN_L} , shutdown IC		1.0		V
I _{EN}	EN input current	V _{EN} =1V		500		nA
I _{SCP}	LS NFET current threshold for SCP			20		A
V _{SCP}	FB voltage threshold for SCP			0.4		V
T _{HICCUP}	Waiting time for restart in hiccup mode			300		mS
T _{POR}	POR time			2		mS
T _{PRE_CHG}	VBUS Pre-charge time			4		mS
T _{TURN_ON}	Disconnect MOS Turn on time			4		mS
T _{STARTUP}	FB Soft Startup time			4		mS
T _{SD}	Thermal shutdown temperature			150		°C
T _{SD_HYS}	Thermal shutdown hysteresis temperature			20		°C

Note4: Guaranteed by design, not tested in production.

TYPICAL CHARACTERISTICS

$T_A=25^{\circ}\text{C}$, $V_{IN}=4\text{V}$, $V_{OUT}=12\text{V}$, $C_{OUT}=10\mu\text{F} + 22\mu\text{F}\times 3$, $L=2.2\mu\text{H}$, $F_s=476\text{kHz}$, unless otherwise noted .





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Detailed Functional Description

Overview

The AWP36220 is a synchronous boost converter designed for delivering the switch peak current up to 15A and output voltage up to 18V.

AWP36220 has an internal feature to help improving light load efficiency. When output current is low, AWP36220 will go into DCM mode.

The AWP36220 provides the excellent line and load transient response with the minimal output capacitor. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

The AWP36220 supports the adjustable switching frequency up to 2MHz. The device implements a programmable cycle-by-cycle current limit to protect the device from overload during the boost operation phase. The AWP36220 triggers the hiccup short protection if the output current further increases and exceeds the short current threshold or the output voltage drops below the short threshold. And this device recovers automatically once the short condition releases.

Additionally, the AWP36220 provides the gate driver for the external FET to isolate the output from input during shutdown.

Under-voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.35 V (typical). A hysteresis of 350 mV (typical) is added so that the device cannot be enabled again until the input voltage exceeds 2.7 V (typical). This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.35V and 2.7V.

Enable and Disable

When the input voltage is above UVLO rising threshold of 2.7V and the EN pin is pulled high above 1.2 V, the AWP36220 is enabled. When the EN pin is pulled below 1V, the AWP36220 goes into the shutdown mode and stops switching.

Startup

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high as well, the AWP36220 starts to ramp up the output voltage. There is a switching pre-charge phase and the output voltage is charged up to input voltage ($1.0 \times V_{IN}$).

After the pre-charge phase ends (typical 4 ms), The AWP36220 gradually turns on the external FET at the output side, which completely disconnects the output from the input during shutdown or output short happens.

After the turn-on phase ends (typical 4 ms), The AWP36220 regulates the FB pin to the internal soft start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft start time is typical 4 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the startup stresses and surges.

Load Disconnect Gate Driver

The AWP36220 device provides a DISDRV pin to drive the external FET at the output side, which completely disconnects the output from the input during shutdown or output short happens. During the device's start-up phase, the disconnect FET is controlled by the gate driver voltage of the external disconnect FET, there is an internal 55 μ A (typical) sink current. The load disconnect FET connection is shown as Figure 4.

The driver voltage and turn on / off timing can be set via the resistor and capacitor connecting between the

DISDRV pin and the source of the external FET. See the Application and Implementation section for the details of how to select the gate resistor and capacitor.

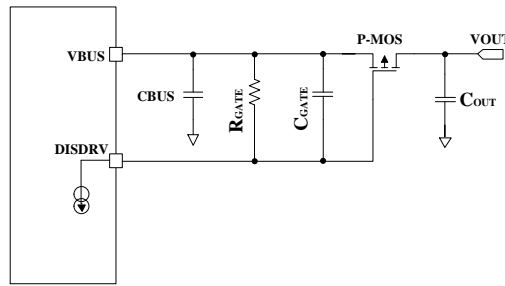


Figure 4 The Load Disconnect Connection

Adjustable Cycle-by-Cycle Switching Current Limit

The peak switch current limit can be set by a resistor connecting with the I_{LIMIT} pin. The relationship between the current limit and the resistor is determined by Equation 1.

$$R_{LIMIT} = \frac{1000}{I_{LIMIT}} \quad (1)$$

Where R_{LIMIT} is the resistor for setting the current limit, with the unit of $k\Omega$, I_{LIMIT} is switching peak current limit, with the unit of A. For instance, when the resistor value is $100 k\Omega$, the switch peak current limit is 10 A. It is worth noting that the maximum switch peak current limit is 15 A.

Output Short Protection (with load disconnected FET)

In addition to the cycle-by-cycle current limiting, the AWP36220 also has the output short protection. If the inductor current reaches the short protection limit threshold (typical 20A) or the output voltage drops below 33%(typical) of the normal output voltage, the device enters into the hiccup protection mode. In the hiccup mode, the device shuts down itself and restarts after 300 ms (typical) waiting time which helps to reduce the total thermal dissipation. After the short condition releases, the device can recover automatically and restart the start-up phase.

Adjustable Switching Frequency

The AWP36220 features of a wide adjustable switching frequency ranging up to 2MHz. The switching frequency is set by a resistor connecting with the $FREQ$ pin. This pin cannot be left floating in the application. Use Equation 2 to calculate the resistor value for a desired frequency.

$$\frac{1}{F_{req}} = T_{SW} = R_{F_{req}} \times 2 \times 10^{-5} + 1 \times 10^{-4} \quad (2)$$

Where $R_{F_{req}}$ is the resistor for setting the frequency, with the unit of $K\Omega$, F_{req} is switching frequency, with the unit of kHz. For instance, when the resistor value is $100K\Omega$, the switching frequency is 476kHz.

Error Amplifier

The AWP36220 has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifier is $610 \mu A / V$ typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

Start-up with the Output Pre-Biased

The AWP36220 has been designed to prevent the low-side FET from discharging a pre-biased output. During the pre-biased startup, both high-side and low-side FETs are not allowed to be turned on until the internal soft start voltage is higher than the sensed output voltage at FB pin.

Bootstrap Voltage (BST)

The AWP36220 has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 100 nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

Over-voltage Protection

If the voltage at the V_{bus} pin is detected above over-voltage protection threshold, typically 21 V, the AWP36220 stops switching immediately until the voltage at the V_{bus} pin drops lower than the output over voltage protection threshold (with 500mV hysteresis). This function prevents the devices against the over-voltage and secures the circuits connected to the output from excessive over voltage.

Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below 130°C(typical).

Device Functional Modes

AWP36220 operates at the adaptive constant off time peak current mode control (CMCOT). At the beginning of each switching cycle, the low-side FET switch turns on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. The PWM controller turns off the low-side FET when the peak inductor current reaches a threshold level set by the error amplifier output. After the low-side FET turns off, the high-side synchronous FET is turned on after a short dead time until the adaptive off timer end or until the inductor current reaches the reverse current sense threshold.

During the portion of the switching cycle when the low-side FET is on, the input voltage is applied across the inductor and stores the energy as the inductor current ramps up. Meanwhile only the output capacitor supplies the load current. When it turns off the low-side FET, the inductor transfers the stored energy via the high-side synchronous FET to replenish the output capacitor and also supply the load current. This operation repeats every switching cycle.

Application Information

Typical Application

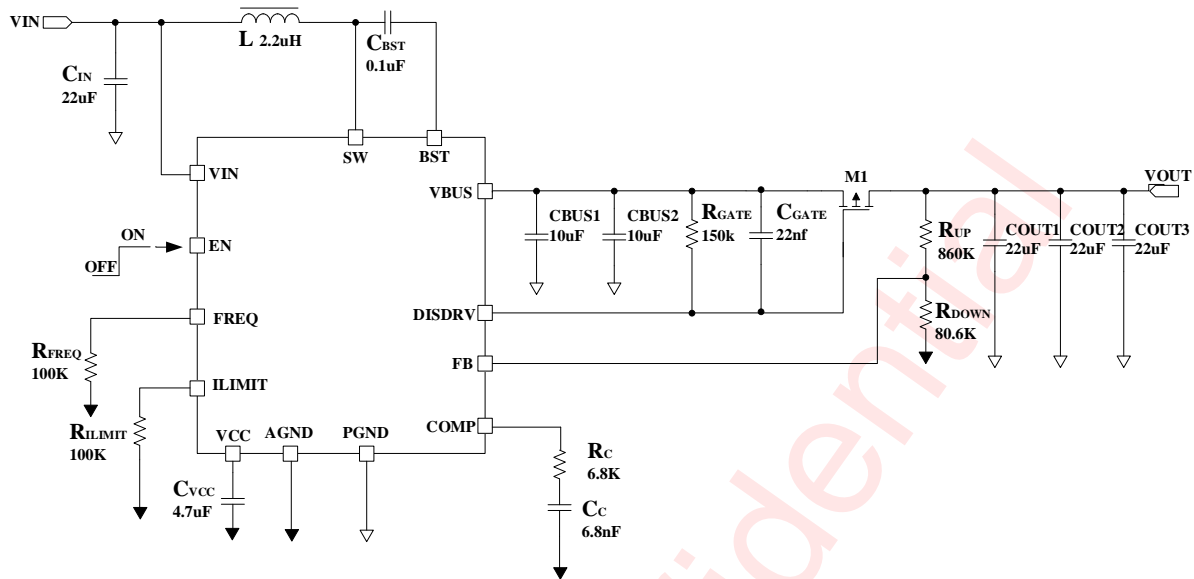


Figure 5 14V Output Voltage With Load Disconnect Function

The Figure 5 is the typical application schematic for 2.7 V to 4.4 V input (single cell Li+ battery) to output 14-V output converter. The inductor can be lower to 1.8 μ H for the 14 V output.

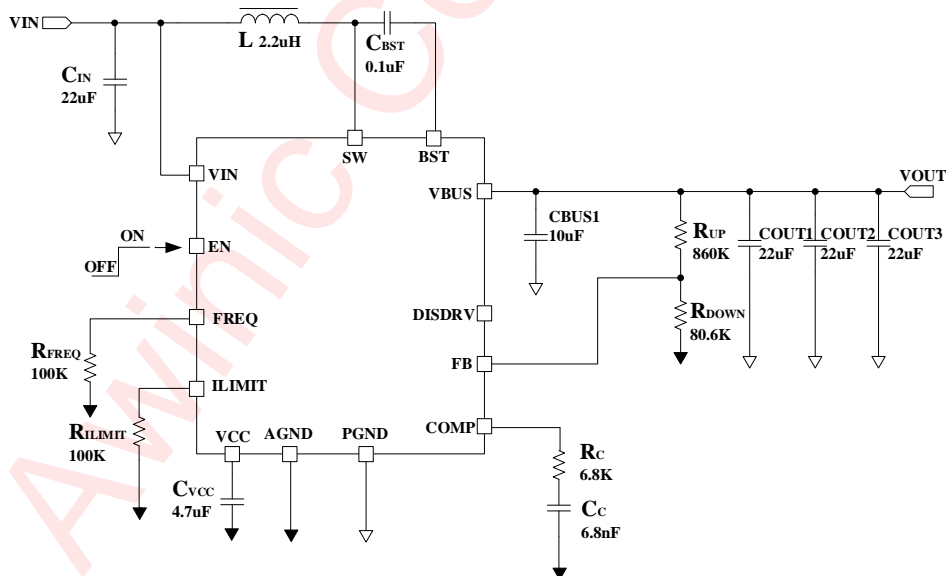


Figure 6 14V Output Voltage Without Load Disconnect Function

The Figure 6 is the typical application schematic for 2.7 V to 4.4 V input (single cell Li+ battery) to output 14-V output converter. With removing the load disconnect FET, it simplifies the design and minimizes the external components.

Setting the switching Frequency

The switching frequency of the AWP36220 is set at 476 kHz. Use Equation 2 to calculate the required resistor value. For a target switching frequency of 476 kHz, The calculated value is 100 kΩ.

Setting the Cycle-By-Cycle Current Limit

The current limit of the AWP36220 could be programmed by an external resistor. Use Equation 1 to calculate the required resistor value. For a target current limit of 10 A, the calculated resistor value is 100 kΩ.

Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R1 and R2. If R1=200k is chosen, then R2 can be calculated to be:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

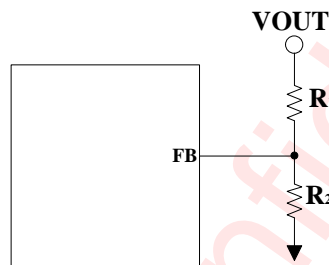


Figure 7 Setting the Output Voltage

Selecting the Inductor

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{0.4 \times F_{SW} \times I_{OUT_MAX}} \quad (4)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

AWP36220 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT_MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{OUT_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{2 \times F_{SW} \times L} \quad (5)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 10mohm to achieve a good overall efficiency.

Selecting the Maximum Output current

Under different conversion ratios, the maximum load capability should follow the guidelines in Figures 8 and 9. Exceeding the recommended current may cause chip damage.

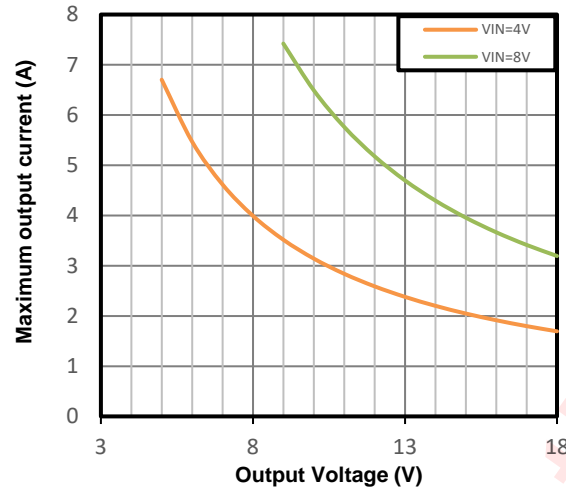


Figure 8 Maximum Output Current vs Output Voltage

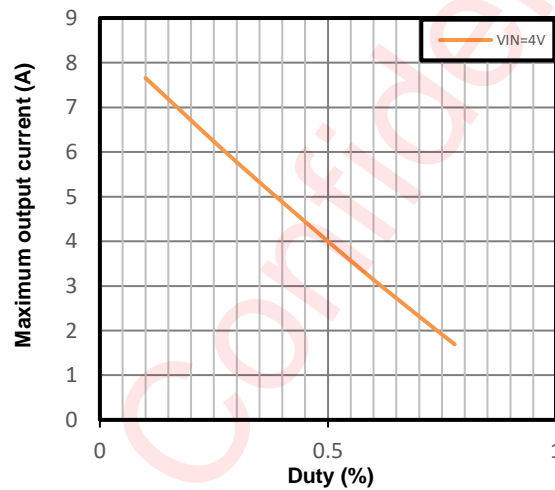


Figure 9 Maximum Output Current vs Duty

Selecting the Output Capacitors

The Boost Output capacitor CBD and disconnection FET Output capacitor COUT are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken in to account when selecting these capacitors. It is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than 44 μ F capacitors. Depending on the specific ripple and transient performance requirements, the output capacitance value should be appropriately increased to ensure compliance with design specifications.

Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22 μ F input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed

between CIN and the power source lead to reduce ringing that can occur between the inductance of the power source leads and CIN.

Selecting the Disconnect FET

The AWP36220 provides a gate driver to control an external FET to disconnect the output from the input at shutdown or output short conditions, shown in Figure 4.

The V_{DS} , I_{DS} and safe operation area (SOA) should be taken into consideration when selecting the FET:

- The drain-to-source voltage rating should be higher than the output max. voltage, $V_{DS_DIS_MAX} = V_{OUT}$,
- The drain-to-source RMS current rating is the maximum output current. $I_{DS_DIS_RMS} = I_{OUT}$,
- The SOA should be considered when the output short occurs, and there is heat caused by the short protection response time and surge current, $SOA > Q_{SHORT}$.

$$Q_{SHORT} = 0.5 \times V_{OUT} \times I_{SHORT} \times T_{SHORT} \quad (6)$$

where

- $V_{DS_DIS_MAX}$ is the maximum drain-source voltage
- I_{DS_DIS} is the drain-source RMS current
- I_{SHORT} is the short current
- T_{SHORT} is the response time before the short protection triggered
- Q_{SHORT} is the heat produced for the output short

For instance: $V_{OUT} = 16\text{ V}$, $I_{SHORT} = 20\text{ A}$, $T_{SHORT} = 30\text{ }\mu\text{s}$.

$SOA \geq 4.8\text{ mJ}$, $V_{DS_DIS_MAX} \geq 16\text{ V}$.

An additional capacitor between the gate and source of the external FET is required to slow the turn-on speed.

$$T_{ON_PFET} = \frac{V_{TH_PFET} \times C_{GS_PFET}}{I_{DIS_PFET}} \quad (7)$$

where

- T_{ON_PFET} is the on time of external FET
- V_{TH_PFET} is the gate threshold of external FET
- C_{GS_PFET} is the total gate capacitance of connected between gate and source external FET. (including the gate-source capacitance of the FET)
- I_{DIS_PFET} is the discharge current inside of AWP36220, it is $55\mu\text{A}$ typically

Given 1.5 V threshold, C_{GS_PFET} is 10 nF , the T_{ON_PFET} is around $300\mu\text{s}$. Please be aware that the maximum turn on time should not exceed 4 ms , and the maximum capacitance C_{GS_PFET} should be $< 100\text{ nF}$. Otherwise, the AWP36220 could not startup normally if the disconnect FET could not be turn on within the 4 ms .

The gate resistor depends on the gate-source voltage of the external FET,

$$R_{GATE} = \frac{V_{GATE}}{I_{DIS_PFET}} \quad (8)$$

Given the 5-V V_{GATE} , the $R_{GATE} = 100\text{ k}\Omega$.

Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is $0.1\mu\text{F}$ to $1\mu\text{F}$. CBST should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of $0.1\mu\text{F}$ was selected for this design example.

Selecting the VCC Capacitor

The primary purpose of the VCC capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the VCC regulator. The value of CVCC should be at least 10 times greater than the value of CBST, and should be a good quality, low ESR, ceramic capacitor. CVCC should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7 μF was selected for this design example.

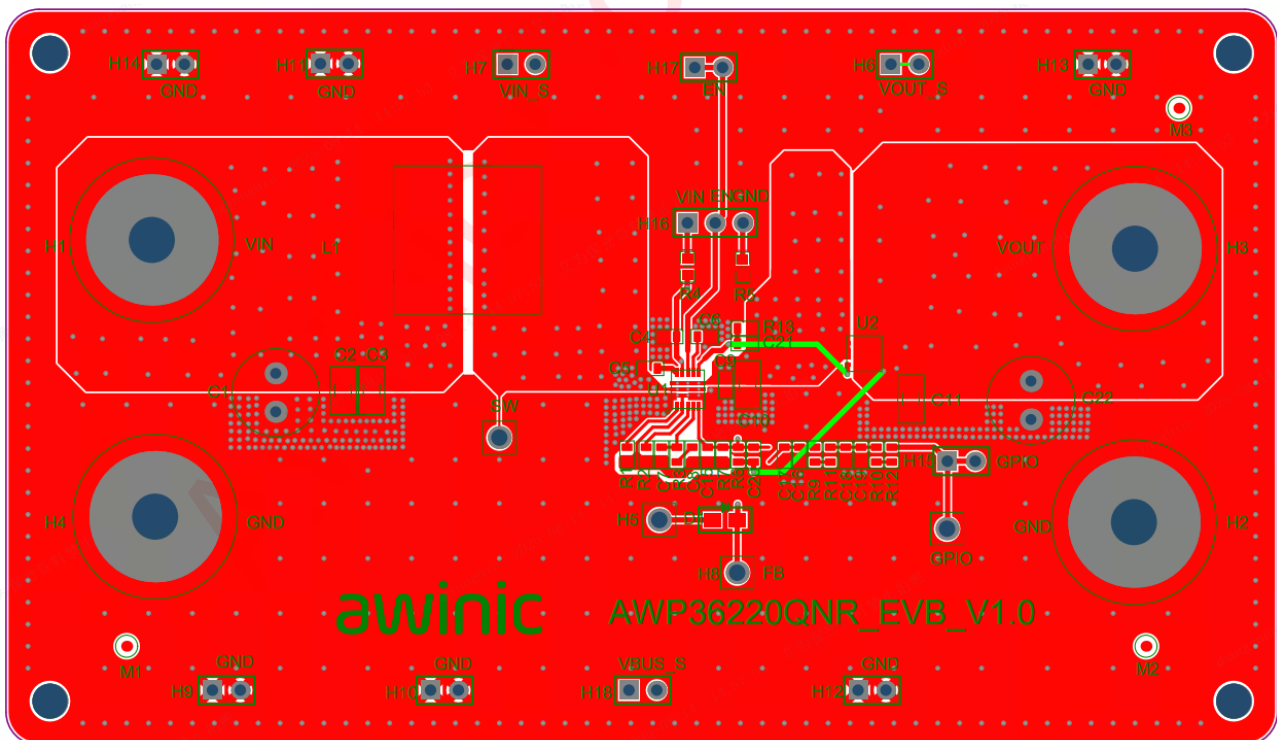
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PCB Layout Consideration

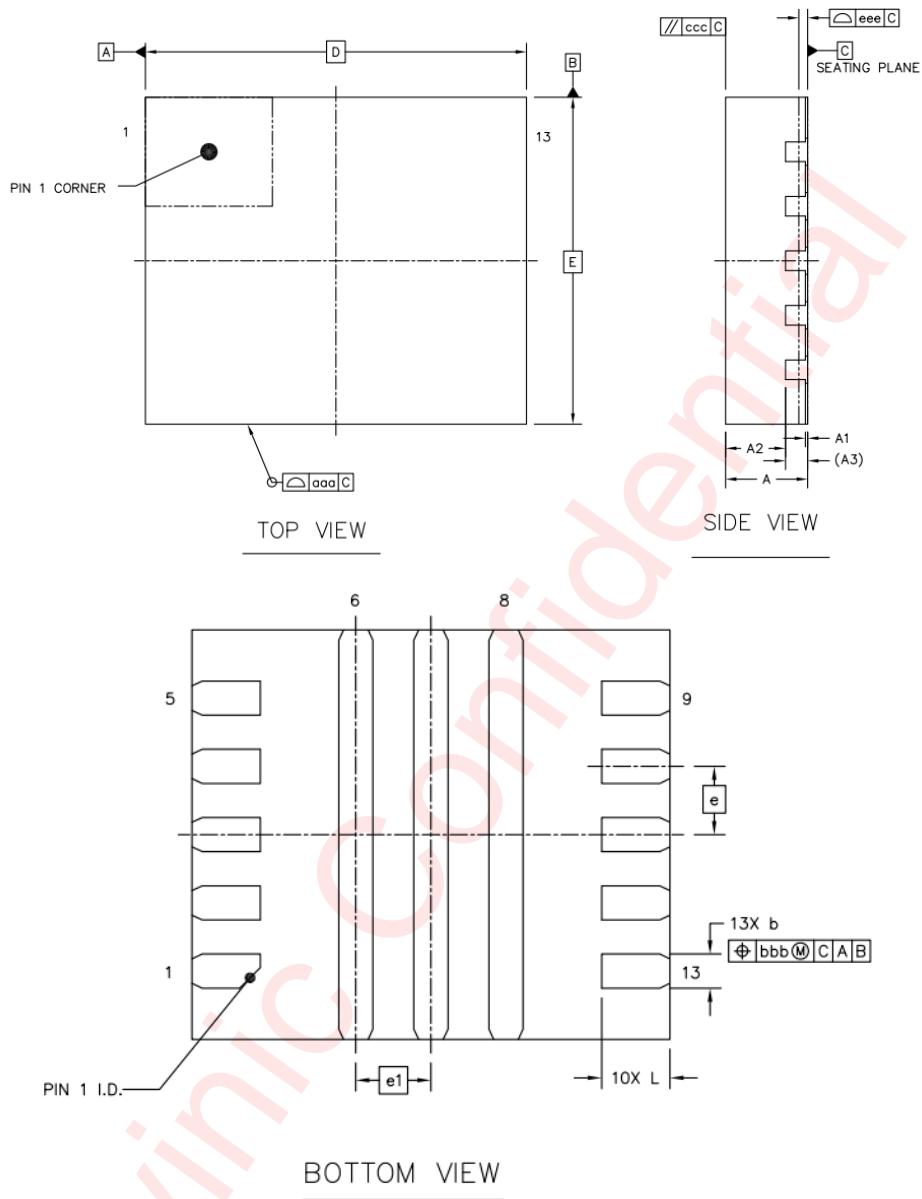
The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems.

The checklist below is suggested that be followed to get good performance for a well-designed board:

1. Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di/dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;
2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling;
3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise;
4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (e.g., VOUT, SW, GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation;
5. Place the input capacitor being close to the VIN pin and the PGND pin in order to reduce the input supply ripple;
6. Place the noise sensitive network like the feedback and compensation being far away from the SW trace;
7. Use a separate ground trace to connect the feedback, compensation, frequency set, and the current limit set circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.



Package Description



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	0.5 BSC		
	e1	0.55 BSC		
LEAD LENGTH	L	0.4	0.5	0.6
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.08		
LEAD OFFSET	bbb	0.1		

Revision History

Version	Date	Change Record
V1.0	Aug. 2025	Officially released

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