12V 1A Dual H-bridge Motor driver

Features

- 2.5V to 12V Supply Power Voltage
- 1A Maximum Drive Current
- Low-Power Sleep Mode With 500-nA Maximum Sleep Current
- Rdson HS + LS: Typical 1.14Ω
- Dual H-Bridge Motor Driver
  1 Stepper Motor or 2 DC Motors
  1 DC Motor on Parallel Mode
- Decay Modes Supported:
  – Slow Decay
  – Fast Decay
- Over Current Protection (OCP)
- Thermal Shutdown (TSD)
- Under Voltage Lockout (UVLO)
- Supported Package and Footprint:
  WBQFN 3mm×3mm-16L package
  WBETSSOP-16L package

Applications

- Video Security Cameras
- Robotics
- Point-of-Sale Printers
- Portable Printers
- Office Automation Machines
- Battery-Powered Toys

General Description

The AWD8833C provides a dual H-bridge motor driver solution for Point-of-Sale printer, Video Security Cameras, Robotics, and other mechatronic applications.

The device has two H-bridges that can drive one bipolar stepper motor, two brush DC motors, solenoids or other inductive loads.

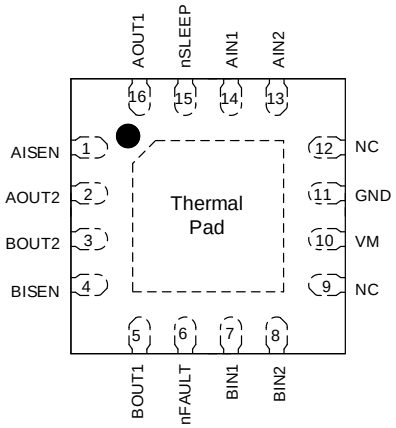
Each H-bridge output consists of a pair of N-channel and P-channel MOSFETs that regulate the winding current. The device can support peak currents of up to 1A per bridge. Current capability is slightly reduced at lower VM voltages.

Internal shutdown functions are provided for over-current protection, short-circuit protection, Under-voltage lockout and Over-temperature protection.

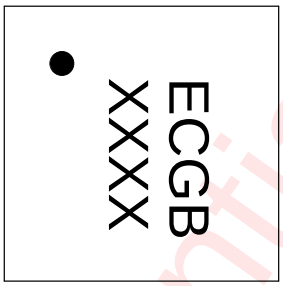
Pin Configuration And Top Mark

AWD8833CQNR

AWD8833CQNR
(Top View)



AWD8833CQNR Marking
(Top View)



ECGB - AWD8833CQNR
XXXX - Production Tracing Code

Pin Definition

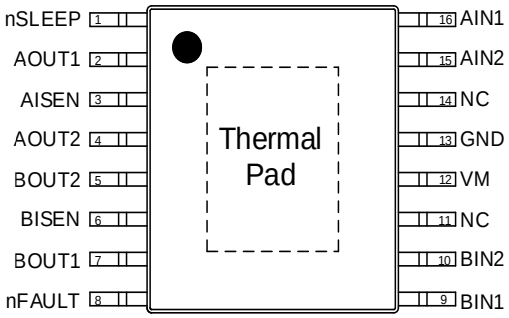
AWD8833CQNR

No.	NAME	DESCRIPTION
1	AISEN	Sense output of bridge A. If current regulation is not required it must connect to GND
16	AOUT1	H-bridge A output
2	AOUT2	
5	BOUT1	H-bridge B output
3	BOUT2	
4	BISEN	Sense output of bridge B. If current regulation is not required it must connect to GND
6	nFAULT	Fault indication pin. Pulled logic low with fault condition; open-drain output requires an external pull-up
7	BIN1	H-bridge B PWM input. Controls the state of BOUT1 and BOUT2; internal pulldown
8	BIN2	
9	NC	No Connection
10	VM	Power supply. Connect to motor supply voltage; Bypass to GND with a 10-μF(MIN) capacitor rated for V_M
11	GND	Ground
12	NC	No Connection
13	AIN2	H-bridge A PWM input. Controls the state of AOUT1 and AOUT2; internal pulldown
14	AIN1	
15	nSLEEP	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown

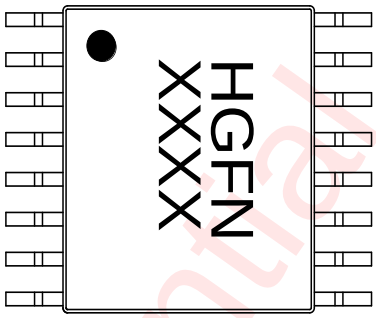
Pin Configuration And Top Mark

AWD8833CTSR

AWD8833CTSR
(Top View)



AWD8833CTSR Marking
(Top View)



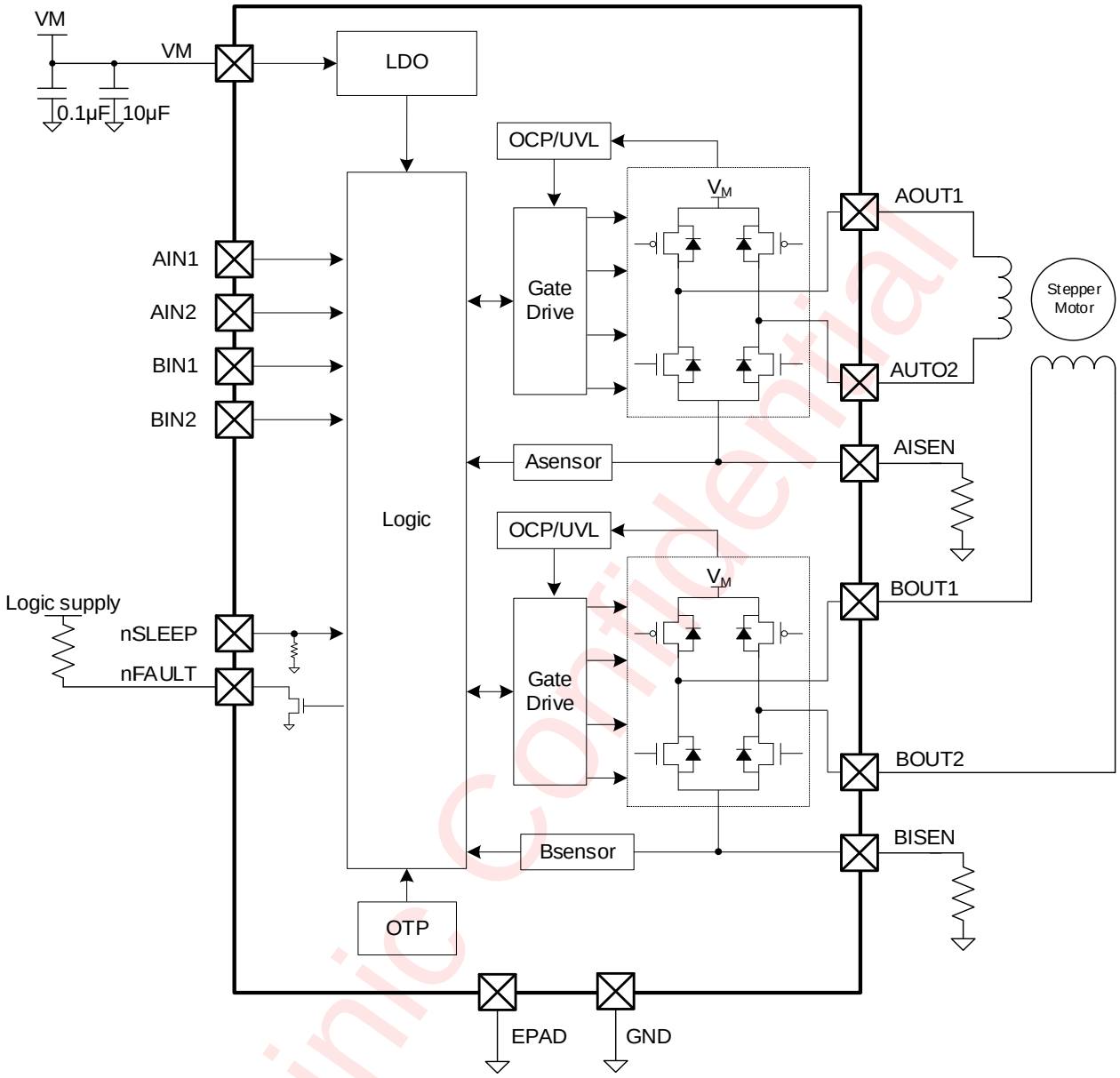
HGFN - AWD8833CTSR
XXXX - Production Tracing Code

Pin Definition

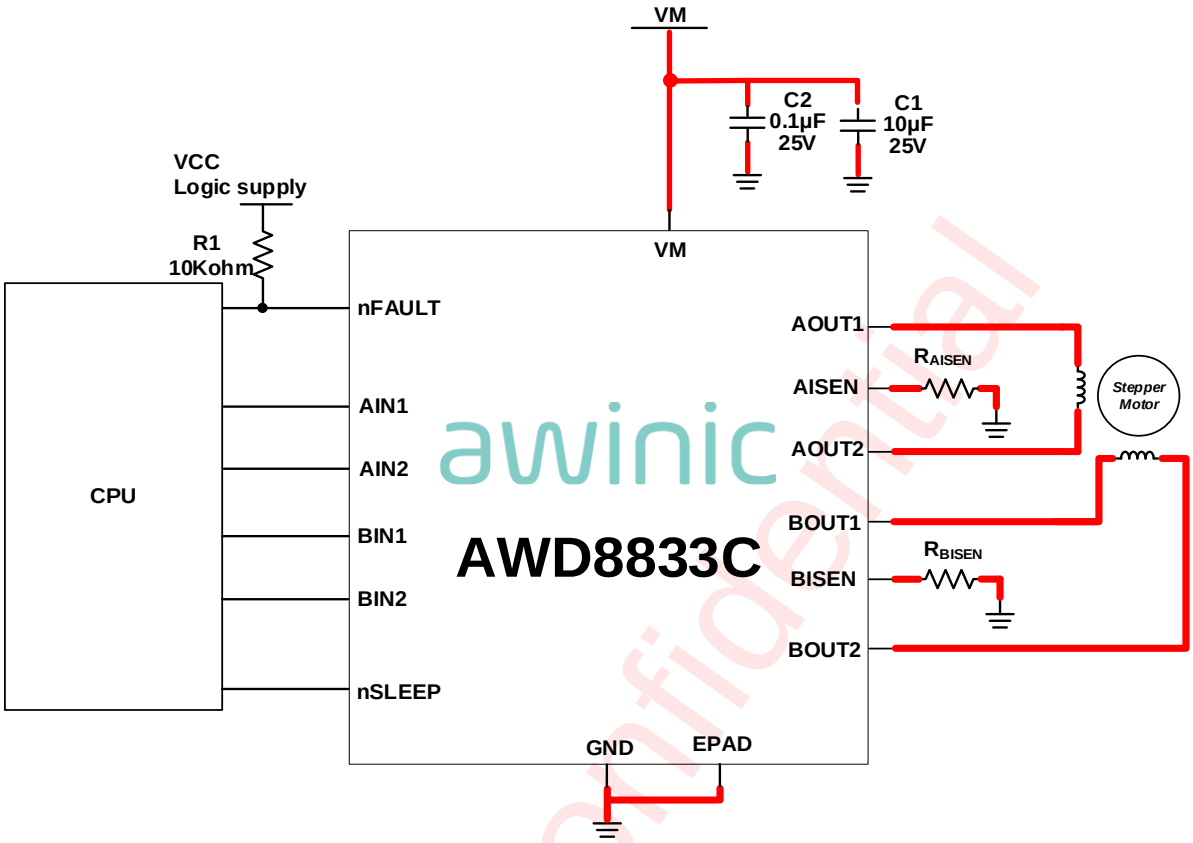
AWD8833CTSR

No.	NAME	DESCRIPTION
3	AISEN	Sense output of bridge A. If current regulation is not required it must connect to GND
2	AOUT1	H-bridge A output
4	AOUT2	
7	BOUT1	H-bridge B output
5	BOUT2	
6	BISEN	Sense output of bridge B. If current regulation is not required it must connect to GND
8	nFAULT	Fault indication pin. Pulled logic low with fault condition; open-drain output requires an external pull-up
9	BIN1	H-bridge B PWM input. Controls the state of BOUT1 and BOUT2; internal pulldown
10	BIN2	
11	NC	No Connection
12	VM	Power supply. Connect to motor supply voltage; Bypass to GND with a 10-μF(MIN) capacitor rated for V_M
13	GND	Ground
14	NC	No Connection
16	AIN1	H-bridge A PWM input. Controls the state of AOUT1 and AOUT2; internal pulldown
15	AIN2	
1	nSLEEP	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown

Functional Block Diagram



Typical Application Circuits



COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_1	VM	GND	25V, 10μF (minimum) ceramic capacitor rated for V_M
C_2	VM	GND	25V, 0.1μF ceramic capacitor rated for V_M
R1	VCC	nFAULT	10kΩ

1：Please place low-ESR ceramic bypass capacitors C1,C2 as close to the chip as possible.

2：Use current sense resistor R_{AISEN} and R_{BISEN} to control the chopping current according to Equation $I_{CHOP} = \frac{200mV}{R_{xISEN}}$,If current regulation is not required AISEN Pin and BISEN Pin must connect to GND. For details , please see ***CURRENT CONTROL*** .

3：The nFAULT pin is an open-drain output and requires a pull-up resistor R1 to be connected to the nFAULT pin. A typical resistor value is 10K, which pulls it up to the digital supply voltage.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWD8833CQNR	-40°C~85°C	WBQFN 3mm×3mm-16L	ECGB	MSL1	ROHS+HF	6000 units/ Tape and Reel
AWD8833CTSR	-40°C~85°C	WBETSSOP-16L	HGFN	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum RATINGS(NOTE1)

PARAMETERS	RANGE
Power supply voltage (VM)	-0.3V to 13.2V
Power supply voltage ramp rate (VM)	0V/μs to 2 V/μs
Control pin voltage (AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT)	-0.3V to 6V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	-0.3V to (VM+0.6)V
Continuous shunt amplifier input pin voltage (AISEN, BISEN)	-0.6V to 0.6V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)	Internally limited
Junction-to-ambient thermal resistance θ_{JA}(WBQFN 3mm×3mm-16L)	79.03°C /W
Junction-to-ambient thermal resistance θJA(WBETSSOP-16L)	45°C /W
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature TJMAX	150°C
Storage temperature TSTG	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including CDM HBM)	
HBM(Human Body Model)	±2000V
CDM(Charge Device Model)	±1000V
Latch-Up	
Test Condition: JEDEC STANDARD NO.78F.01	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		Range	Unit
VM	Power supply voltage	2.5 to 12	V
V_I	Logic input voltage (AINx, BINx)	0 to 5	V
f_{PWM}	Logic input PWM frequency (AINx, BINx)	0 to 200	kHz
I_{peak}	Peak output current	0 to 1	A
T_A	Operating ambient temperature	-40 to 85	°C

Electrical Characteristics

V_{VM} =5V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)						
V_{VM}	V_{VM} operating voltage		2.5		12	V
I_{VM}	V_{VM} operating supply current	V_{VM} = 5 V, nSLEEP = 1, xINx=0		470	1000	μA
I_{VMQ}	V_{VM} sleep mode supply current	V_{VM} = 5 V, nSLEEP = 0		0.5	1	μA
t_{SLEEP}	Sleep time	nSLEEP = 0, V_{VM} = 5 V, RL=24Ω+100μH		4		μs
t_{WAKE}	Wake-up time	nSLEEP high to output transition, V_{VM} = 5 V, RL=24Ω+100μH		58		μs
t_{ON}	Power-on time	V_{VM} > V_{UVLO} to output transition		30		μs
Control Inputs (AIN1, AIN2, BIN1, BIN2 and nSLEEP)						
V_{IL}	Input logic low voltage	xINx			0.45	V
		nSLEEP			0.45	V
V_{IH}	Input logic high voltage	xINx	1.3			V
		nSLEEP	1.3			V
V_{HYS}	Input logic hysteresis	xINx		0.16		V
		nSLEEP		0.2		V
I_{IL}	Input logic low current	V_{IN} = 0 V	-1		1	μA
I_{IH}	Input logic high current	V_{IN} = 5 V, xINx		35	50	μA
		V_{IN} = 5 V, nSLEEP		10	15	μA
R_{PD}	Pulldown resistance	xINx	90	150	180	kΩ
		nSLEEP	300	500	650	kΩ
t_{DEG}	Input deglitch time			600		ns
t_{PROP}	Propagation delay INx to OUTx	V_{VM} =5V, nSLEEP =1, RL=24Ω+100uH		1.1		μs
Control Output (nFAULT)						
V_{OL}	Output logic low voltage	I_O=5mA, nFAULT		0.3	0.5	V
I_{OH}	Output logic high leakage current	R_{pullup}=1kΩ to 5V, nFAULT	-1		1	μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Motor Driver Outputs (AOUT1, AOUT2, BOUT1 and BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 5 V, I = 0.2 A, T_A = 25°C		0.73	1	Ω
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 5 V, I = 0.2 A, T_A = 25°C		0.41	0.7	Ω
I_{OFF}	Off-state leakage current	V_{VM} =5V	-1		1	μA
t_{RISE}	Output rise time	V_{VM} =5V, R_L=16Ω, L=1mH		16		ns
t_{FALL}	Output fall time	V_{VM} =5V, R_L=16Ω, L=1mH		65		ns
t_{DEAD}	Output dead time	Internal dead time		220		ns
PWM Current Controls (AISEN and BISEN)						
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{OFF}	Current control constant off time	Internal PWM constant off time		28		μs
Protection Circuits						
V_{UVLO}	V_{VM} under voltage lockout	V_{VM} falling; UVLO Report	2.0	2.2	2.4	V
		VM rising; UVLO recovery	2.1	2.3	2.5	V
V_{UVLO_HYS}	UVLO hysteresis	Rising to falling threshold		0.1		V
I_{OCP}	Overcurrent protection trip level			1.5		A
t_{DEG}	Overcurrent deglitch Time			1.6		μs
t_{OCP}	Overcurrent protection Period			1.5		ms
T_{TSD}	Thermal shutdown temperature	Die Temperature T_J		160		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C

Typical Characteristics

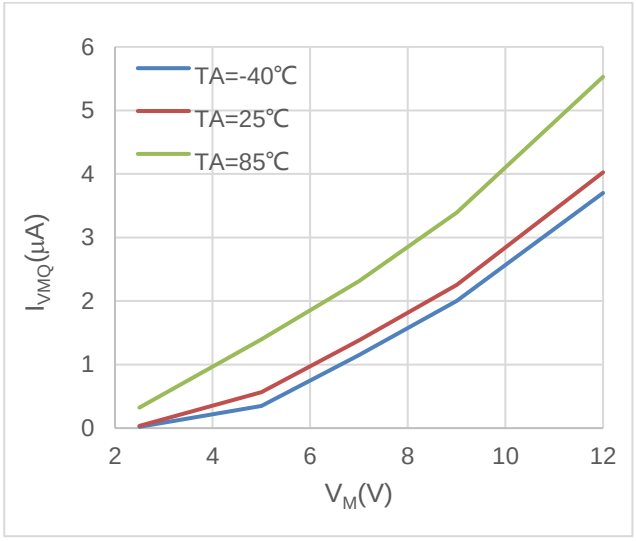


Figure 1. Sleep Current

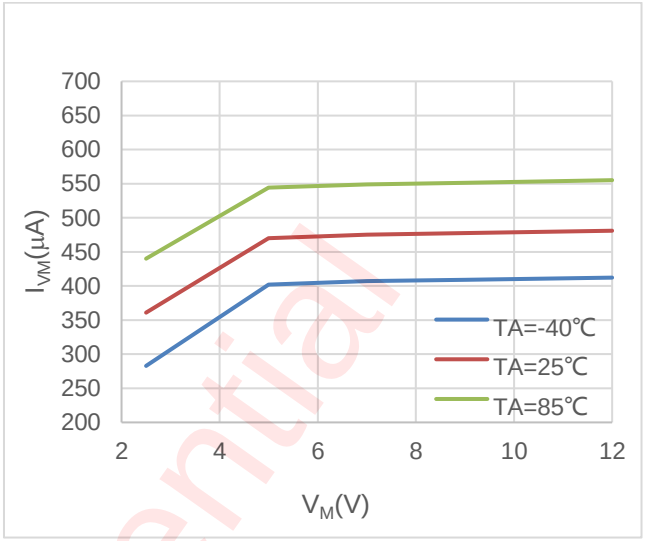


Figure 2. Supply Current

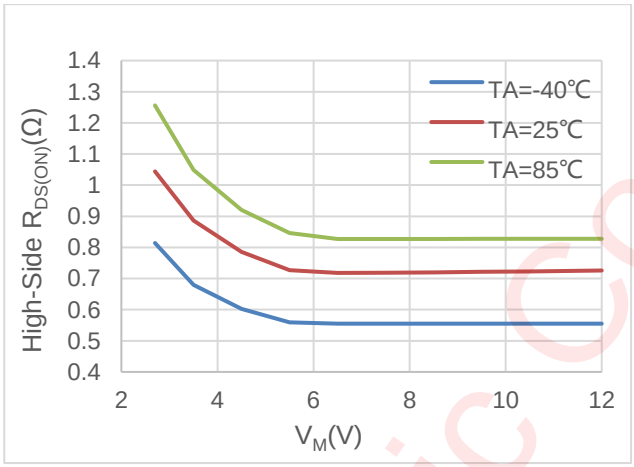


Figure 3. High-Side $R_{DS(ON)}$

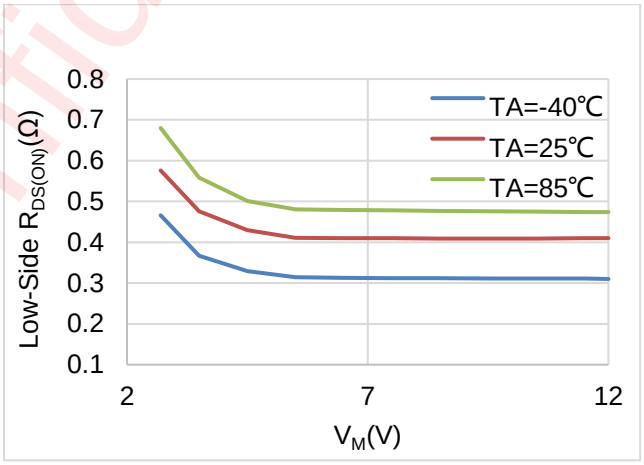


Figure 4. Low-Side $R_{DS(ON)}$

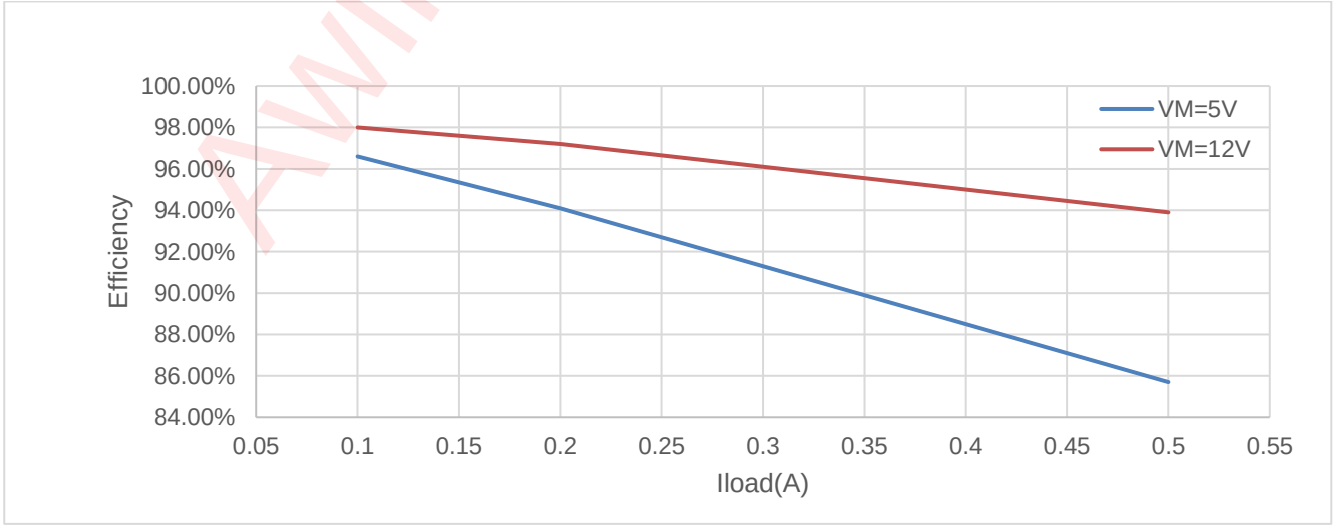


Figure 5. Output Efficiency

Detailed Functional Description

The AWD8833C device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two PMOS + NMOS H-bridges and current regulation circuitry. The AWD8833C device can be powered with a supply voltage from 2.5V to 12 V and can provide an output current up to 1A Peak.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation is a 28μs fixed off-time slow decay.

The device includes a low-power sleep mode, which lets the system save power when not driving the motor.

PWM Motor Drivers

The AWD8833C includes two full H-bridge drivers. **Figure 6** shows a block diagram of the circuit.

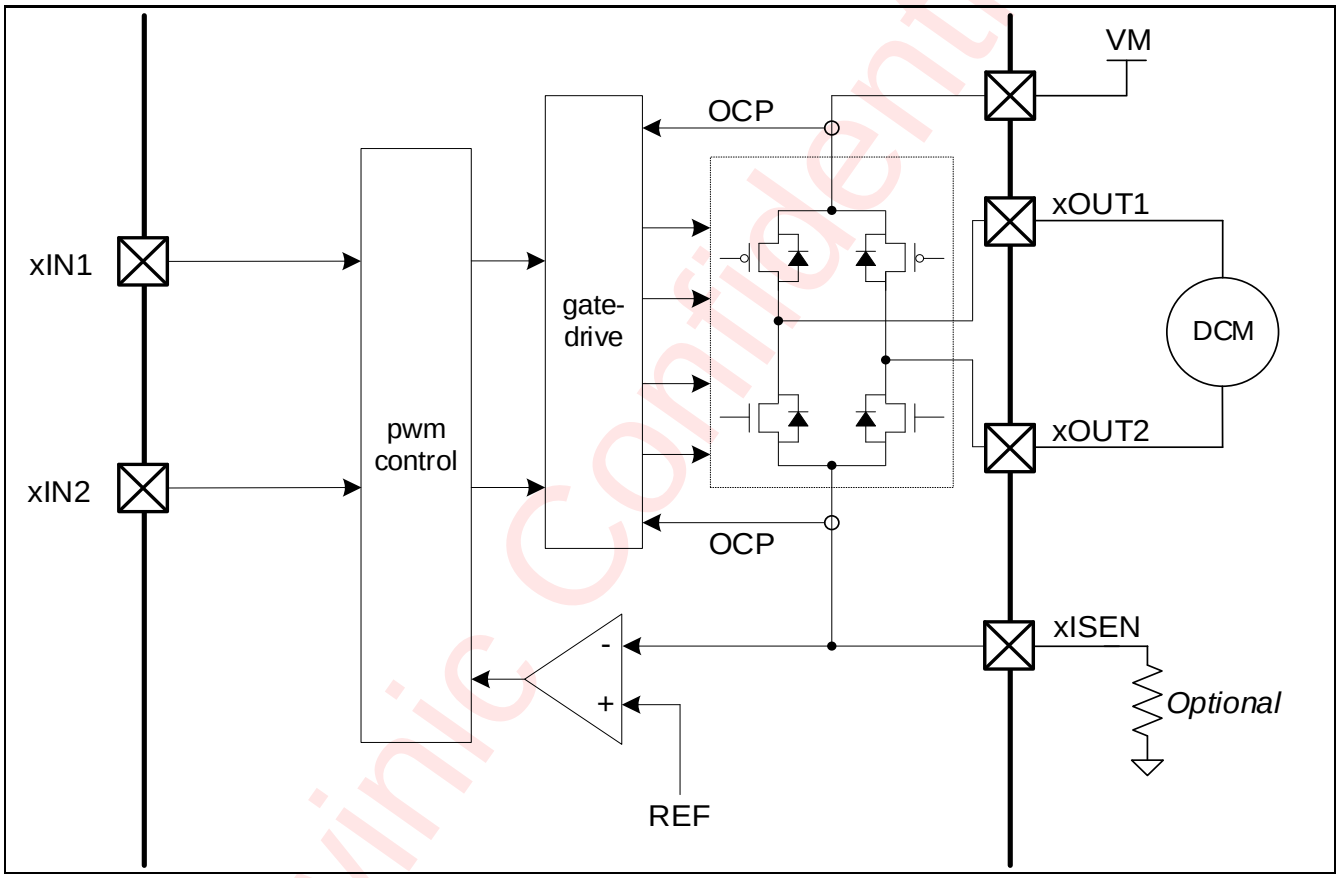


Figure 6. H-Bridge and Current Chopping block diagram

Bridge Control And Decay Modes

The AIN1 and AIN2 input pins control the state of AOUT1 and AOUT2 outputs. Similarly, the BIN1 and BIN2 Input pins control the state of BOUT1 and BOUT2 outputs. The logical states are shown in **Table 1**.

Table 1 H-Bridge Logic

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast / fast decay
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake / slow decay

Use PWM signals to control the motor speed. When the motor is suddenly turned off by a PWM signal, the H-bridge can enter two different decay modes, fast decay and slow decay. In fast decay mode, all H-bridge FETs are turned off, and the motor current discharges from VM through the body diode. In slow decay mode, the FETs at the upper end of the H-bridge are turned off, the FETs at the lower end of the H-bridge conducts, shorting the motor to ground. The logical states are shown in **Figure 7** and **Figure 8**.

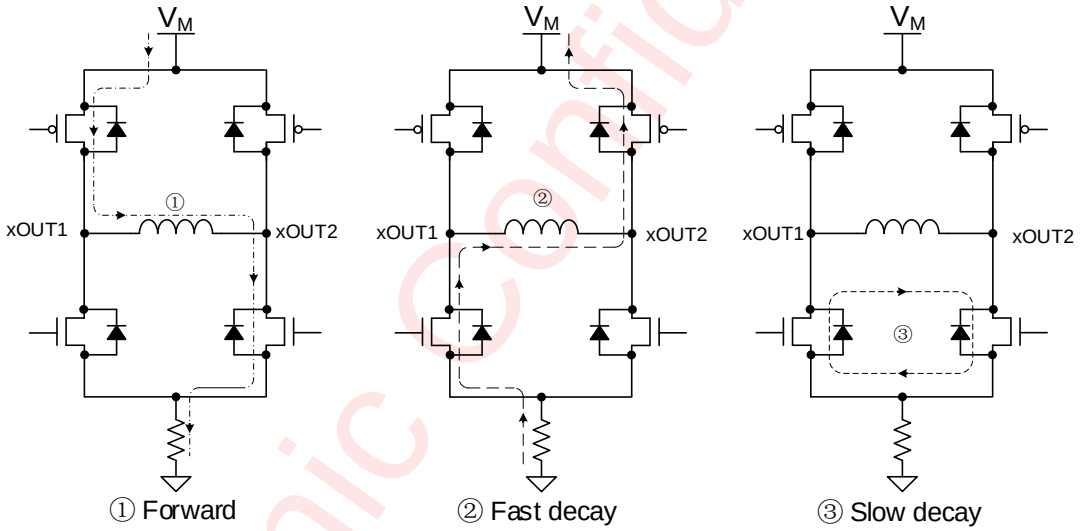


Figure 7. FORWARD Drive and Decay Modes

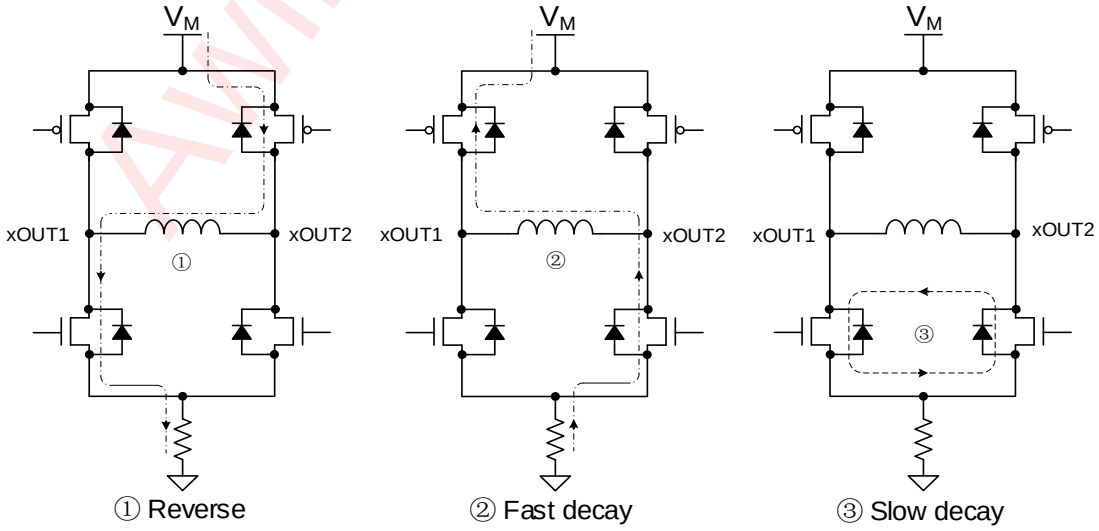


Figure 8. REVERSE Drive and Decay Modes

To enter the fast decay mode, one end of the xIN input terminal should be connected to the PWM signal, and the other end to the low level. To enter the slow decay mode, one end of the xIN input terminal should be connected to the PWM signal, and the other end to the high level, as shown in **Table 2**.

Table 2 PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

Current Control

The current through the motor windings may be limited, or controlled, by a 28μs constant off-time PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Note that immediately after the output is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 2.5μs.

The PWM chopping current is set by a comparator that compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage, $V_{TRIP,}$ is fixed at 200 mV nominally. The chopping current is calculated as in Equation 1.

$$I_{CHOP} = \frac{200mV}{R_{xISEN}} \quad (1)$$

Example: If a 0.5ohm sense resistor is used, the chopping current will be 200 mV / 0.5Ω= 400mA.

Decay Mode

When the motor current reaches I_{CHOP}, the AWD8833C device will enter slow decay mode, during which the FET at the upper end of the H-bridge turns off and the FET at the lower end of the H-bridge conducts, shorting the motor terminals. The current flowing through the motor will gradually decrease, and this short-circuit condition will last for 28μs. After 28μs, the FET at the upper end of the drive H-bridge will conduct again, and the current will gradually increase. The description and calculation of ICHOP can be found in the "**CURRENT CONTROL**" chapter.

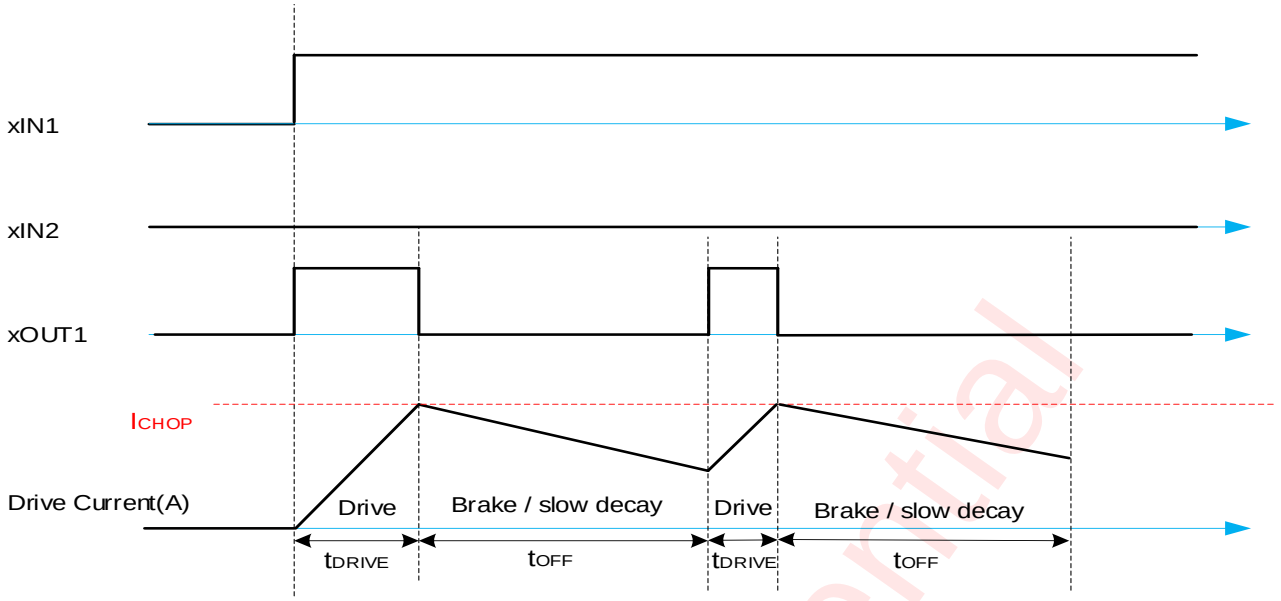


Figure 9. Current Chopping Operation

Sleep Mode

The device enters sleep mode to reduce power consumption when the nSLEEP pin is driven low. In sleep mode, all H-bridge FETs are disabled unless the nSLEEP pin is driven high again. When returning from sleep mode, some time, t_{WAKE}, needs to pass before the motor driver becomes fully.

Parallel Mode

The AWD8833C device can drive a DC motor by connecting two H-bridges in parallel, resulting in a current twice that of a single H-bridge. A sufficient dead time can ensure that the device does not have a situation where the upper and lower switches of the two H-bridges turn on simultaneously. The application is shown in **Figure 10**.

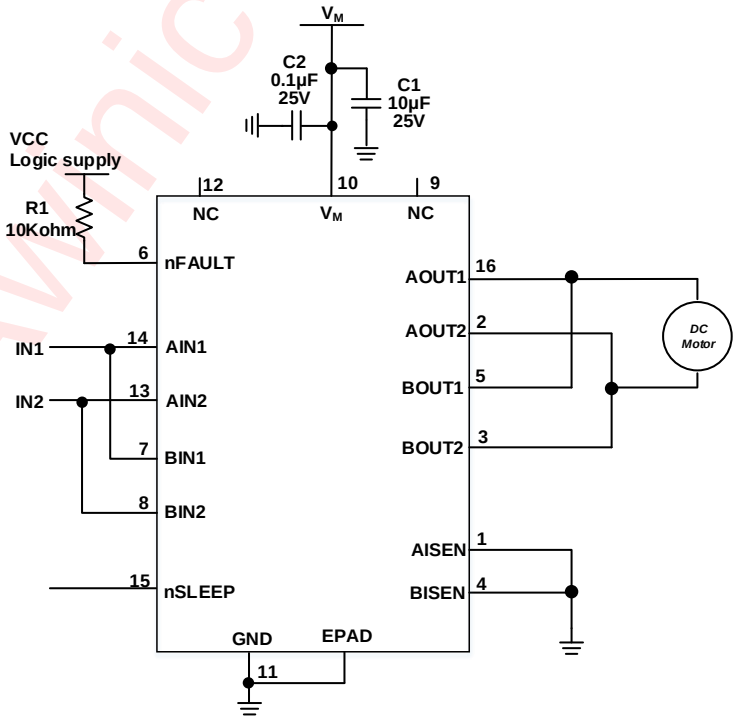


Figure 10. Parallel Mode Schematic

Stepper Motor Mode

The AWD8833C can support full- and half-stepping modes to drive a stepper motor using the PWM interface.

Full-Step Mode

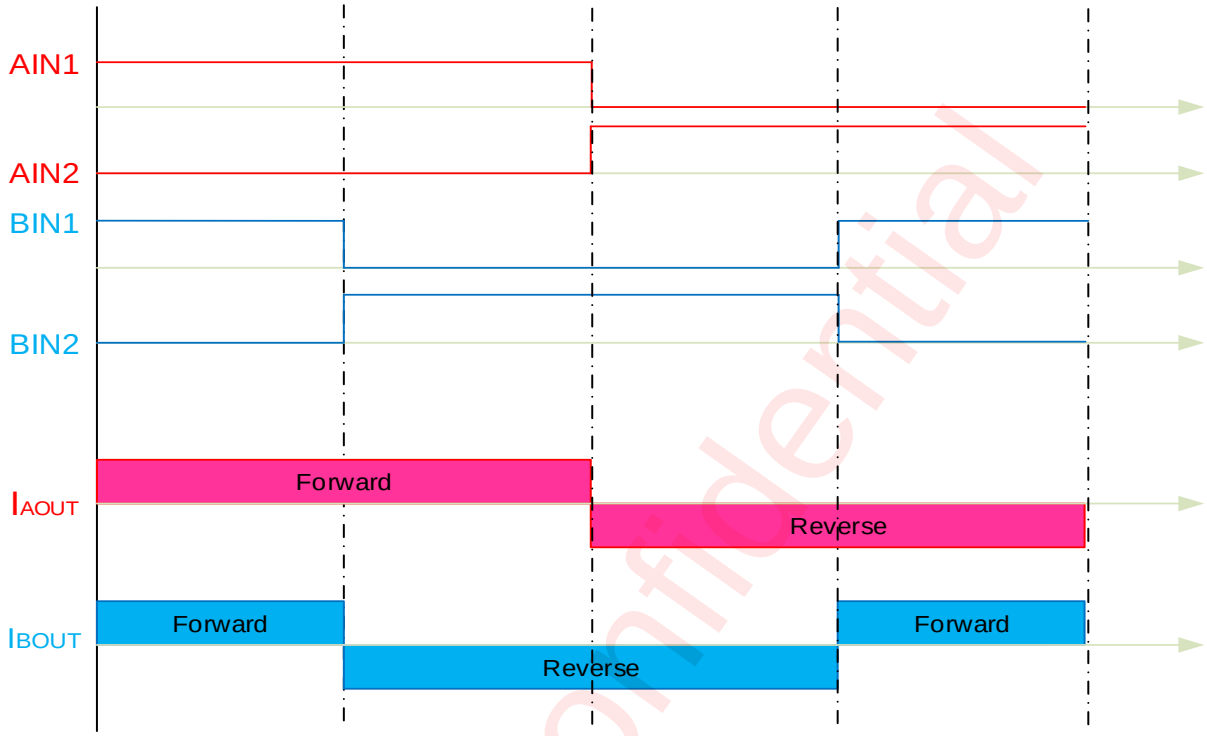


Figure 11. Full-Step Mode

Half-Step Mode

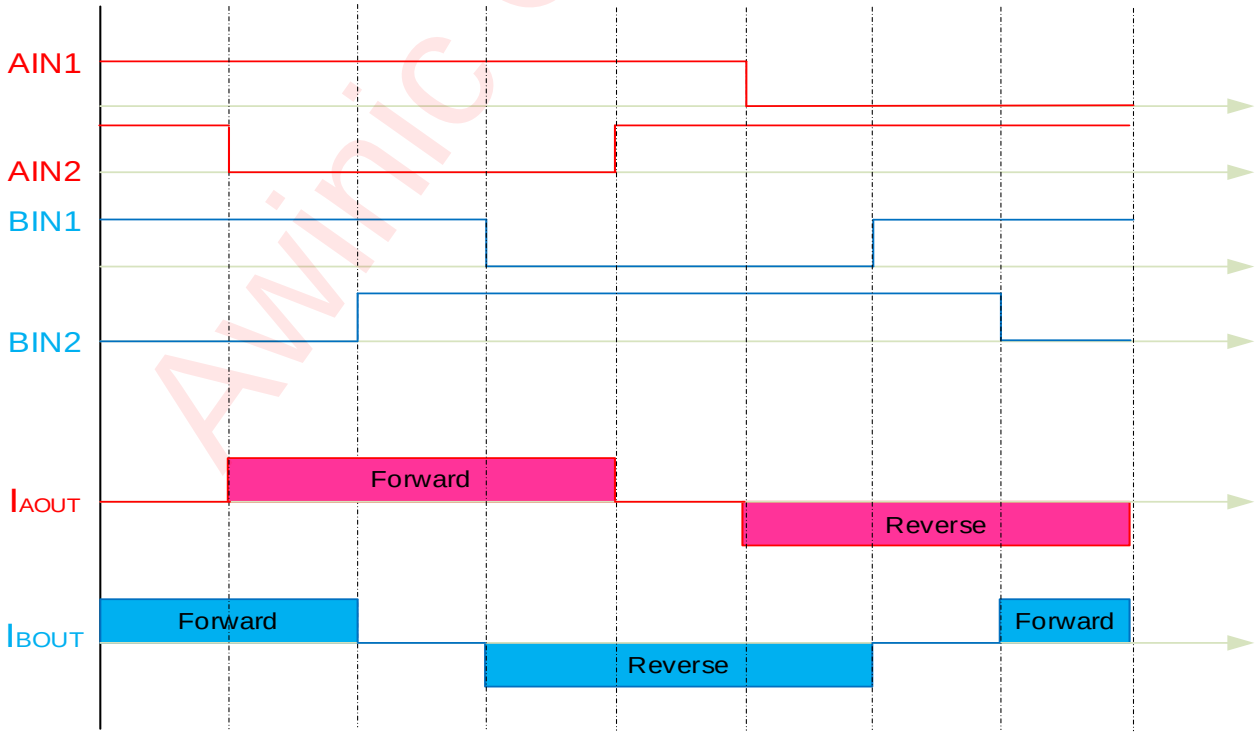


Figure 12. Half-Step Mode

Protection Circuits

The AWD8833C chip provides Overcurrent, OverTemperature, and undervoltage protections.

Table 3 Device Protection

Fault	Condition	Error Report	H-Bridge	Internal Circuits	Recovery
V_M Under-Voltage (UVLO)	V_M < 2.2V	None	Disabled	Disabled	V_M > 2.3V
Over Current (OCP)	I_{OUT} > I_{OCP}	nFAULT	Disabled	Operating	OCP
Thermal Shutdown (TSD)	T_J > T_{TSD}	nFAULT	Disabled	Operating	T_J < T_{TSD} - T_{HYS}

Over Current Protection (OCP)

Analog current limiting (IOCP) circuits on each FET limit the current through the FET by limiting the gate drive. If this analog current restriction lasts longer than the OCP deglitch time (tDEG), all MOSFET in the H-bridge disable and the nFAULT pin is driven to low level.

After the OCP retry period (tOCP) has passed, the driver will be re-enabled.The nFAULT becomes high again after the retry time. If the fault condition persists, the cycle repeats.

Current at both ends of the power supply or motor winding will cause overcurrent shutdown. Pay attention to overcurrent protection

Under Voltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the under-voltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VM pin voltage rises above the UVLO threshold. The UVLO event is not reported on the nFAULT pin.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven to low level. After the die temperature falls to a safe level, operation automatically resumes and the nFAULT pin becomes high again.

PCB layout consideration

1：Bypass the VM terminal to GND using two low-ESR ceramic bypass capacitors with the value of 100nF and 10 μF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin and EPAD pin.

2：The signal network with VM AOUT1 AOUT2 AISEN BOUT1 BOUT2 BISEN pins should be designed considering the current magnitude and if necessary, copper pours can be used in PCB layout.

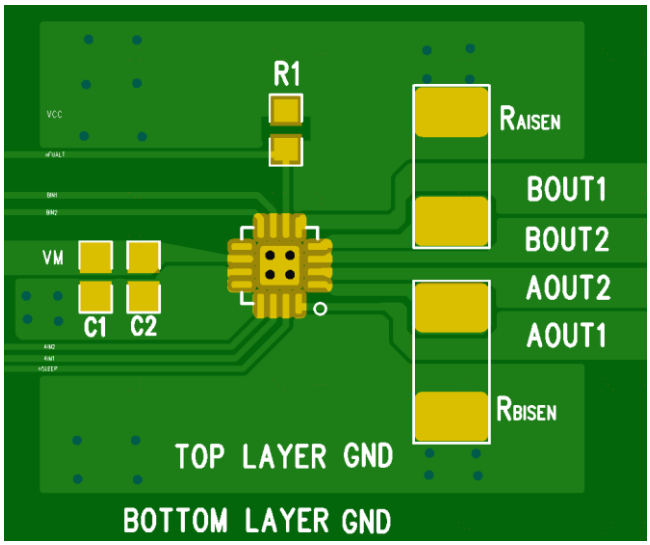


Figure 13. AWD8833CQNR LAYOUT

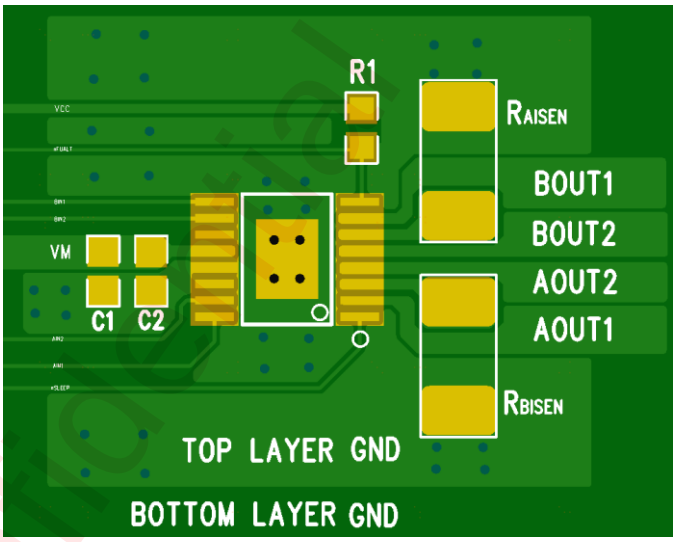


Figure 14. AWD8833CTSR LAYOUT

LAYOUT CONSIDERATIONS

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

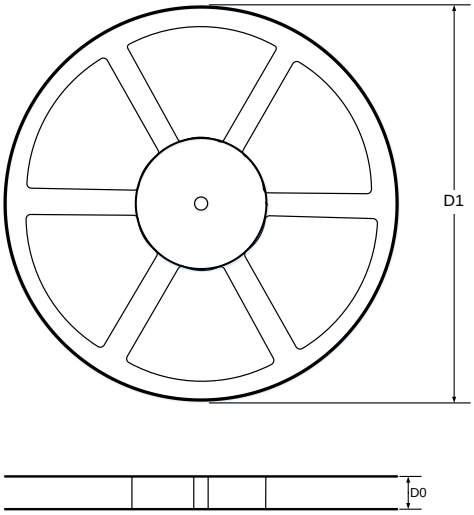
The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the I^2 x R_{DSON} heat that is generated in the device.

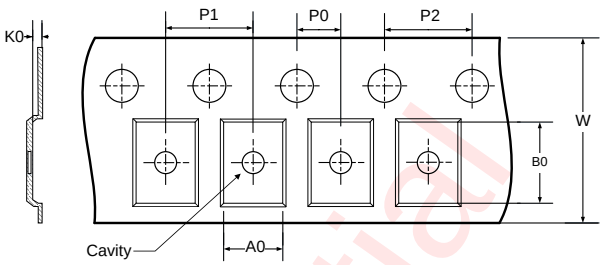
TAPE AND REEL INFORMATION

QFN3x3-16L

REEL DIMENSIONS

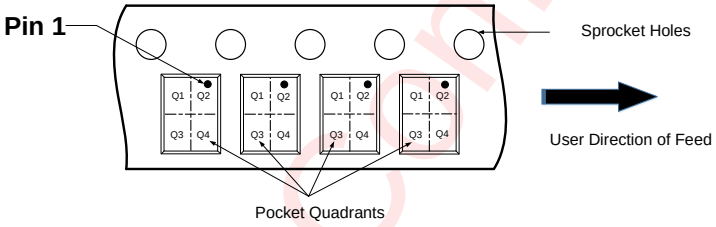


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q2

All dimensions are nominal

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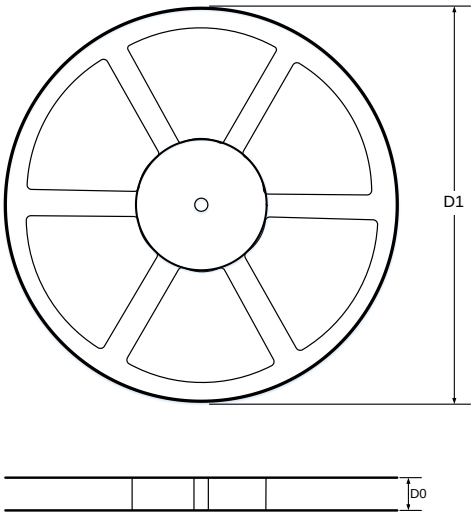
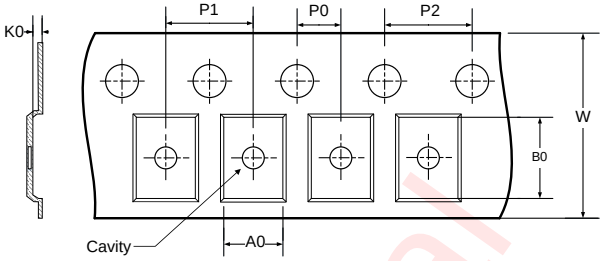
REEL DIMENSIONS

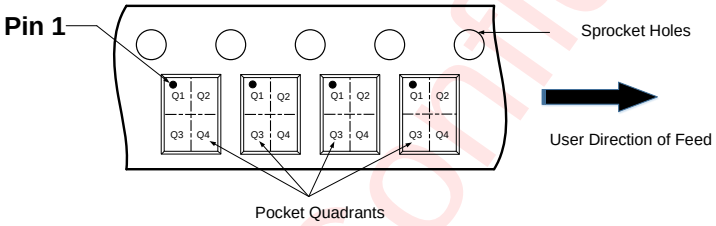


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

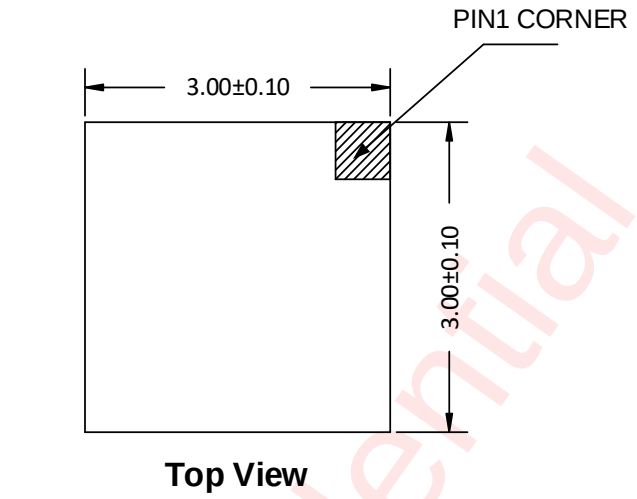
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	6.8	5.4	1.3	2	8	4	12	Q1

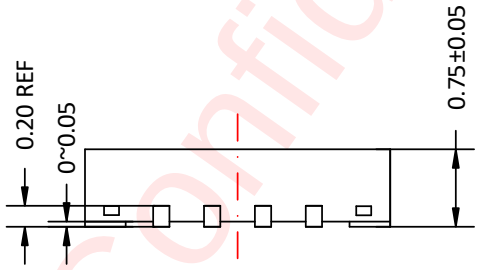
All dimensions are nominal

PACKAGE DESCRIPTION

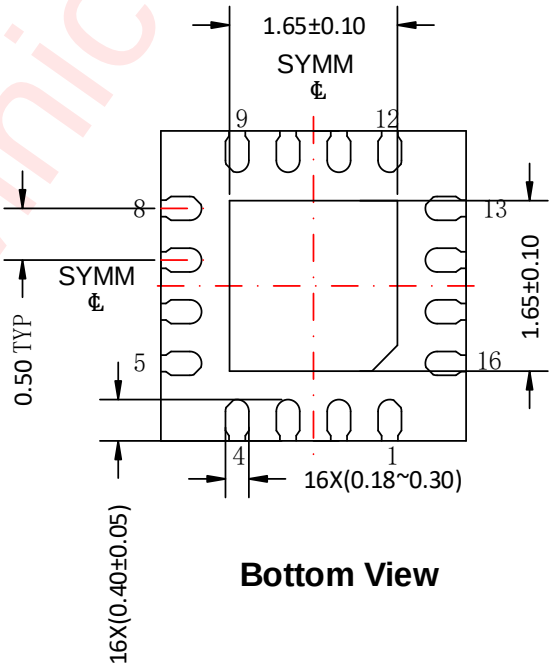
QFN3x3-16L



Top View



Side View



Bottom View

Unit: mm

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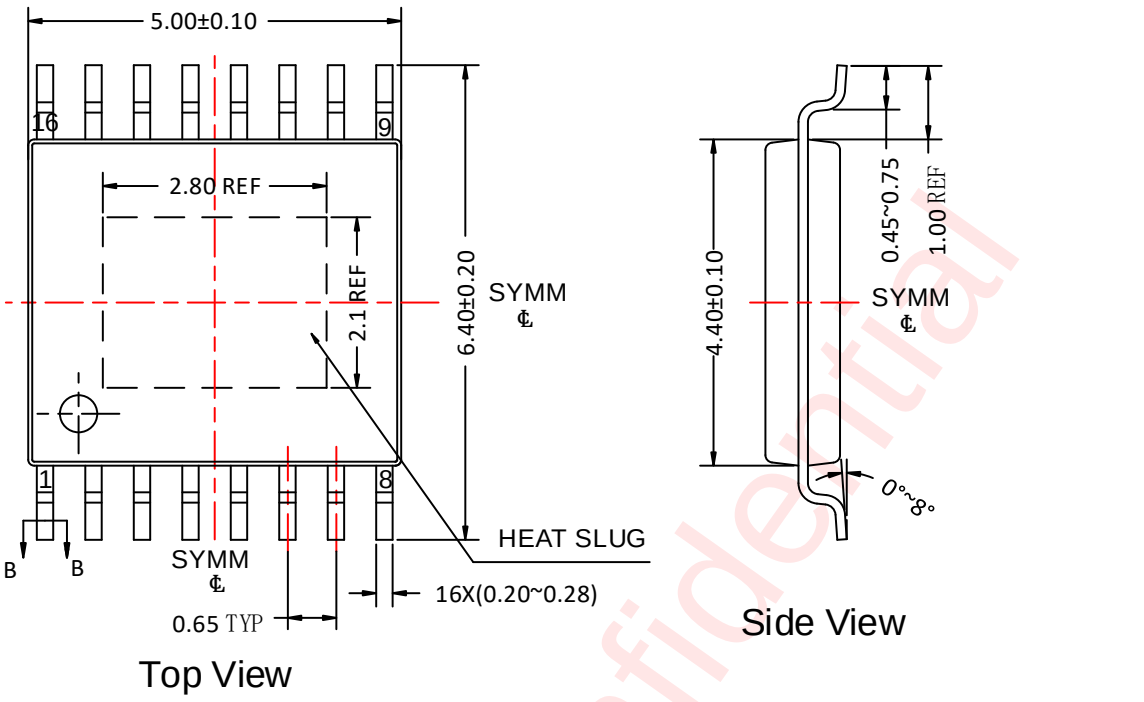
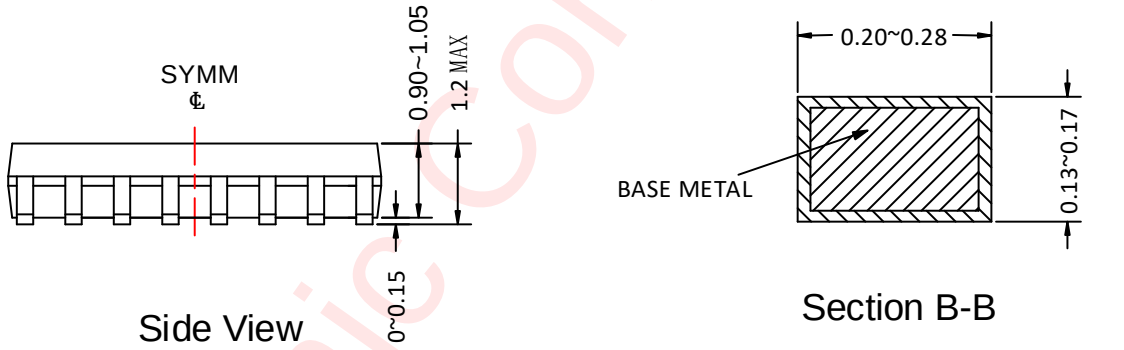
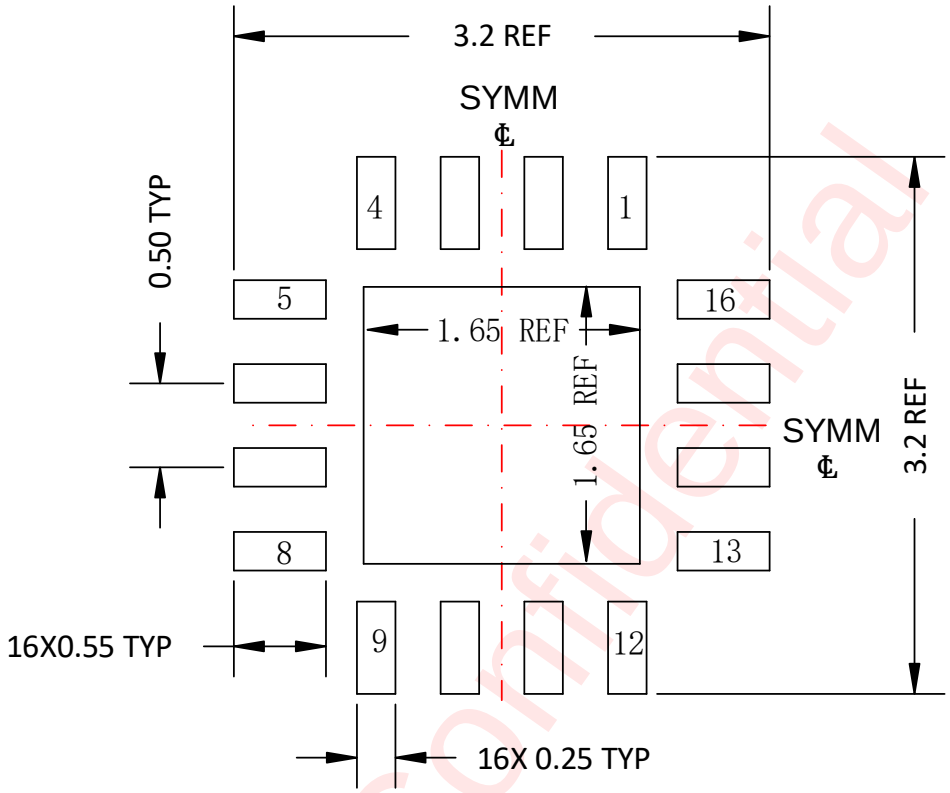


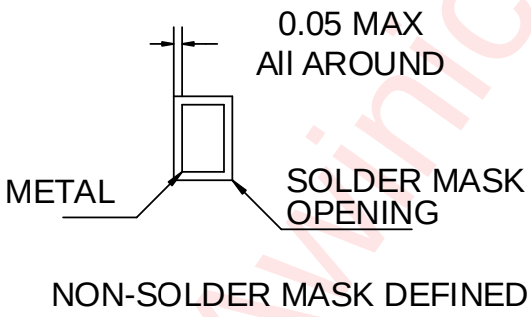


UNIT:mm

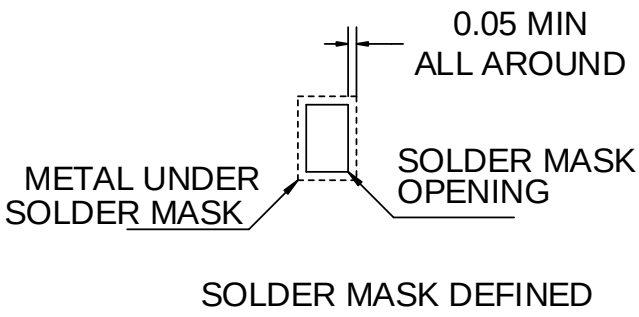
LAND PATTERN DATA

QFN3x3-16L





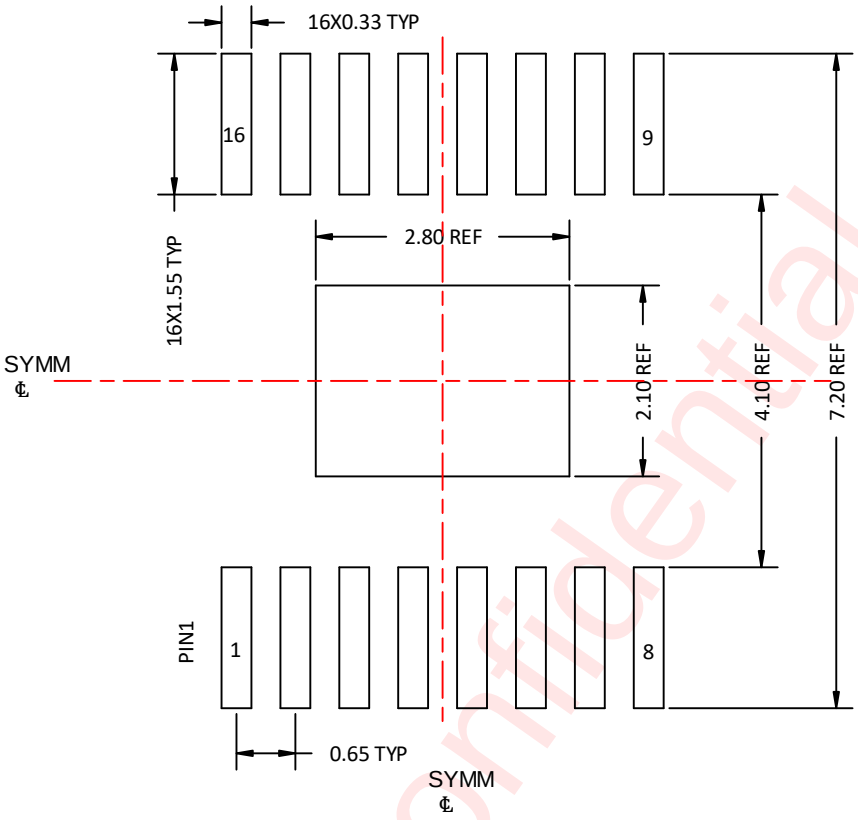
NON-SOLDER MASK DEFINED

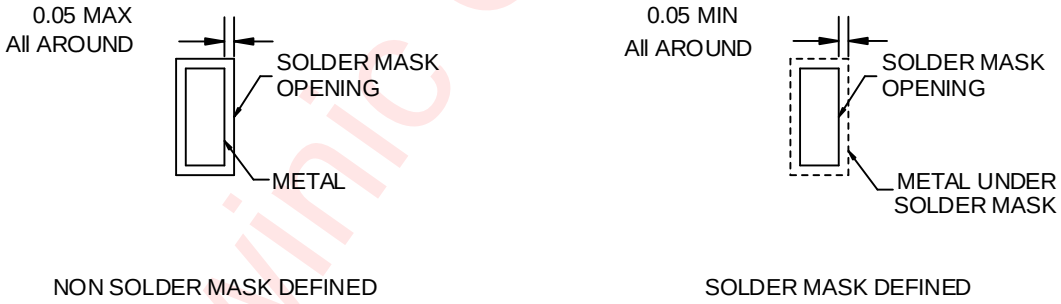


SOLDER MASK DEFINED

Unit: mm

ETSSOP-16L





Unit：mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Jul. 2023	Officially released
V1.1	Sep.2023	Added WEBSSOP-16L packaging information and description
V1.2	Oct.2023	The absolute maximum voltage for VM is modified to 13.2V
V1.3	Jun.2024	Modify the description of PWM Motor Drivers
V1.4	Jun.2025	Change the electrical characteristics of VIL and VIH
V1.5	Sep. 2025	Change the deglitch time value

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