Description

The XPL3238 is a high-current (3A), low-noise (7uVRMS), high accuracy (1% over line, load, and temperature), low-dropout linear regulator (LDO), and is capable of sourcing 3A with extremely low dropout (max. 180mV). The device supports single input supply voltage as low as 1.1V that makes it easy to use.

The low noise, high PSRR, and high output current capability make the XPL3238 ideal to power noise-sensitive devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. To reduce inrush current with very high accuracy, remote sensing, and soft-start capabilities, the XPL3238 is ideal for powering digital loads such as FPGAs, DSPs, and ASICs.

The external enable control and power good indicator function make the sequence control easier. The output noise immunity is enhanced by adding external bypass capacitor on NR/SS pin. The device is fully specified over the temperature range of TJ = −40°C to 125°C and is offered in a WQFN-12L 2.2x2.5 (FC) package.

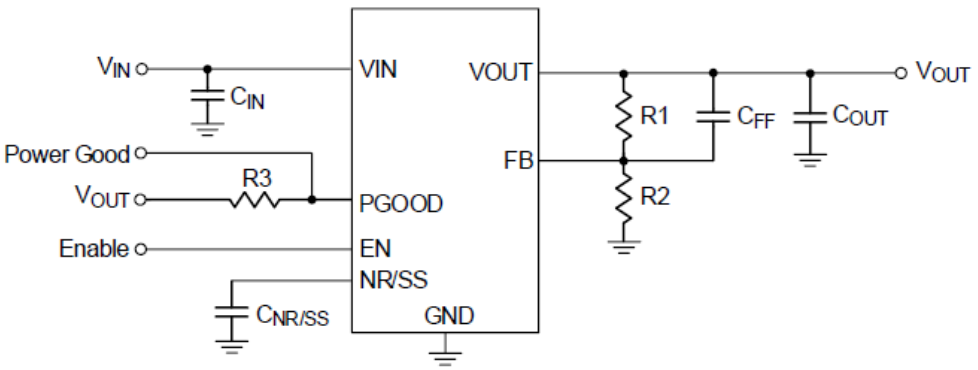
Features

- Input Voltage Range: 1.1V to 6.5V
- Output Voltage Range: 0.5V to 5.5V
- Accurate Output Voltage Accuracy (1%) over Line, Load and Temperature
- Ultra-High PSRR: 40dB at 500kHz
- Excellent Noise Immunity
  7uVRMS at 0.5V Output
  10uVRMS at 3.3V Output
- Ultra Low Dropout Voltage: 180mV at 3A
- Enable Control
- Programmable Soft-Start Output
- Stable with 10uF or higher Output Ceramic Capacitor
- Support Power-Good Indicator Function
- RoHS Compliant and Halogen Free

Applications

- Portable Electronic Devices
- Wireless Infrastructure: SerDes, FPGA, DSP
- RF, IF Components: VCO, ADC, DAC, LVDS

Figure 1. Typical Application Circuit



Revision History

Table 1. Revision History

Release	Rev	Changes	Date
Initial release	0.8	Initial release	04/10/2024

Ordering information

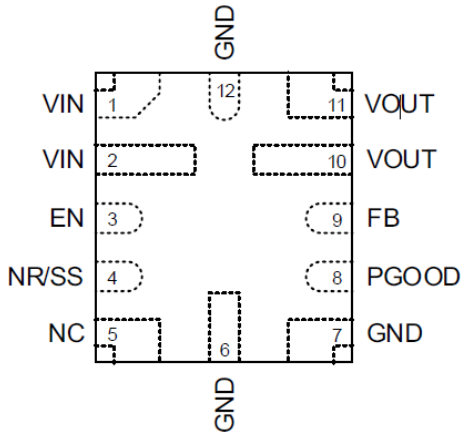
Table 2. Ordering information

Part Number	VREF (V)	Output Current (A)	Top Marking	MPQ
XPL3238AQ12R	0.5V	3	L3238A	3000
XPL3238BQ12R	0.8V	3	L3238B	3000

MPQ = Minimum Packaging Quantity.
For production orders greater than MPQ, the order must be a multiple of MPQ per package size above.

PIN Configuration and Description

(TOP VIEW)



WQFN-12L 2.2x2.5 (FC)

Figure2. Top View

Table 3. Pin Definition

Pin	Name	Description
1,2	VIN	Supply input. A minimum of 22uF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.
3	EN	Enable control input. Connecting this pin to logic high enables the regulator while driving this pin low makes the device enter shutdown mode. The device can operate with VIN and VEN sequenced in any order. Generally, enabling the device after VIN presence can achieve precise timing control.
4	NR/SS	Noise-reduction and soft-start pin. Decoupling this pin to GND with an external capacitor CNR/SS can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft-start behavior. For low noise applications, a 10nF to 1uF CNR/SS is recommended.
5	NC	No internal connection. Leaving this pin floating does not affect the chip functionality. By connecting it to GND, design engineers can extend the GND copper coverage on the PCB top layer to enhance the thermal convection.
6,7,12	GND	Ground. These pins must be soldered to a large PCB and connected to GND for maximum power dissipation.
8	PGOOD	Power good indicator output. It is an open-drain output and is active high when the output voltage reaches 95% of the target. The pin is pulled to ground when the output voltage is lower than its specified threshold, EN shutdown, OCP and OTP.
9	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.5V typically for XPL3238A and 0.8V typically for XPL3238B.

10,11	VOUT	LDO output pins. A 22uF or larger ceramic capacitor (10uF or greater of effective capacitance) is required for stability. Place the output capacitor as close to the device as possible and minimize the impedance between VOUT pins and load.

Absolute Maximum Ratings

Maximum Ratings (1)

Parameter	Min	Max	Units
VIN, PGOOD, EN	-0.3	+7.0	V
VOUT	-0.3	+7.0	V
NR/SS, FB	-0.3	+3.6	V
Storage Temperature Range	-65	+150	°C
Junction Temperature	-40	+150	°C
Electrostatic Discharge (HBM)	-2000	+2000	V
Electrostatic Discharge (CDM)	-1000	+1000	V

(1) Operation of the device outside of these parameters may cause permanent damage.

Recommended Operating Conditions

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{IN}	1.1		6.5	V
Operating Temperature, Junction	T_{OJ}	-40		+125	°C

Thermal Information

Junction to ambient thermal resistance is a function of board layout and ambient air flow condition. This data is based on four layers PCB (30mm x 30mm; 70µm Cu top signal layer) in still air box in accordance with JEDEC standard JESD51 on natural convection.

Parameter	Symbol	Typ	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	46	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	29	°C/W

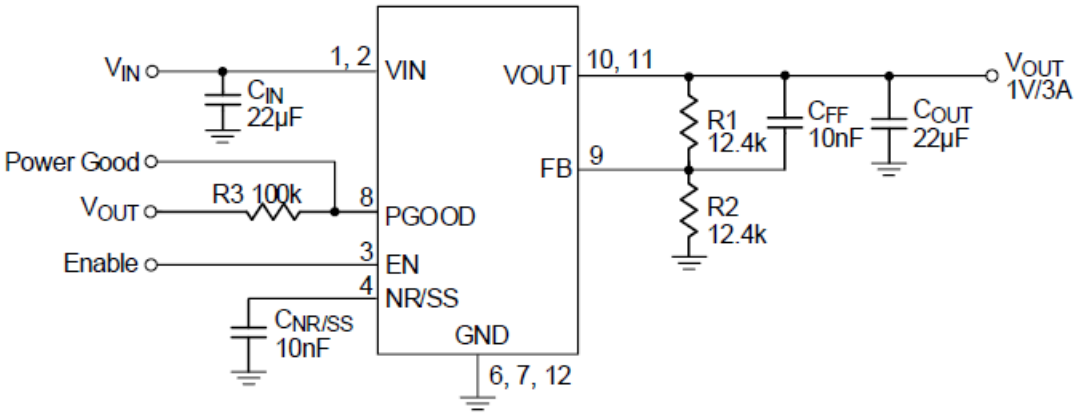
Electrical Specifications

Over operating temperature range (T_J = −40°C to 125°C), (1.1V ≤ V_{IN} < 6.5V and V_{IN} ≥ $V_{OUT(TARGET)}$ + 0.3V, $V_{OUT(TARGET)}$ = 0.5V, V_{OUT} connected to 50Ω to GND, V_{EN} = 1.1 V, C_{IN} = 10µF, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PGOOD pin pulled up to V_{IN} with 100 kΩ, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Operating Input Voltage Range	V_{IN}		1.1		6.5	V
Feedback Reference Voltage	V_{REF}			0.5		V
NR/SS Pin Voltage	V_{NRSS}			0.5		V
Under Voltage Lockout	UVH	VIN Increasing		1.04	1.085	V
	UVL	Hysteresis		100		mV
Output Voltage Range		Using external resistors	0.5		5.5	V
Output Voltage Accuracy	VOUT	VIN = VOUT + 0.3V, 0.5V <= VOUT <= 5.5V, 5mA <= IOUT <= 3A	-1		1	%
Line Regulation	ΔVOUT/ΔVIN	IOUT = 5mA, 1.4V <= VIN <= 6.5V		0.05		%
Load Regulation	ΔVOUT/ΔIOUT	5mA <= IOUT <= 3A		0.08		%
Dropout Voltage	VDROP	VIN = 1.1V to 6.5V, IOUT = 3A, VFB = 0.5 - 3%		100	180	mV
Output Current Limit	ILIM	VOUT = 90% VOUT (Target), VIN = VOUT(Target) + 0.4V.	3.7	4.3	4.7	A
Short Circuit Current Limit	ILIM_SC	VOUT = 10% VOUT (Target), VIN = VOUT(Target) + 0.4V.		1.5		A
Ground Pin Current	IGND	IOUT = 5mA, VIN = 6.5V		6	7	mA
		IOUT = 3A, VIN = 1.4V		3	4	mA
		Shutdown, PGOOD = Open, VIN = 6.5V, VEN = 0.5V.			25	uA
EN Pin Current	IEN	VIN = 6.5V, VEN = 0 and 6.5V	-0.1		0.1	uA
EN Pin High Level Input Voltage	VEN_H	Enable Device	1.1		6.5	V
EN Pin Low Level Input Voltage	VEN_L	Disable Device	0		0.5	V
PGOOD Pin Threshold	VTH_PGOOD	For rising VOUT	0.935 *Vout	0.947 *Vout	0.957 *Vout	V
		For falling VOUT	0.879 *Vout	0.89 *Vout	0.892 *Vout	
PGOOD Pin Low Level Output Voltage	VPGOOD_L	VOUT < VTH_PGOOD, IPGOOD = 1mA.			0.4	V
PGOOD Pin Leakage Current	IPGOOD_LK	VOUT> VTH_PGOOD, VPGOOD = 6.5V.			1	uA
NR/SS Pin Charging Current	INRSS	VNRSS = 0V, VIN = 6.5V.	4	6.4	9	uA
FB Pin Leakage Current	IFB	VIN = 6.5V	-100		100	nA

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Power Supply Rejection Ratio	PSRR	IOUT = 3A, CNRSS = 100nF, CFF = 10nF, COUT=47uF||10uF||10uF	f = 10kHz VIN = 1.2V, VOUT = 0.5V		42		dB
			f = 500kHz VIN = 1.2V, VOUT = 0.5V		30		
			f = 10kHz VIN = 5.5V, VOUT = 5.0V		40		
			f = 500kHz VIN = 5.5V, VOUT = 5.0V		25		
Output Noise Voltage	e_{NO}	BW = 10Hz to 100kHz, IOUT = 3A, CNRSS = 100nF, CFF = 10nF, COUT=47uF||10uF||10uF	VIN = 1.1V, VOUT = 0.5V		7		uV_{RMS}
			VOUT = 3.3V		10		
Thermal Shutdown Threshold	T_{SD}	Temperature Increasing			160		deg C
		Temperature Decreasing			140		

Typical Application Circuit

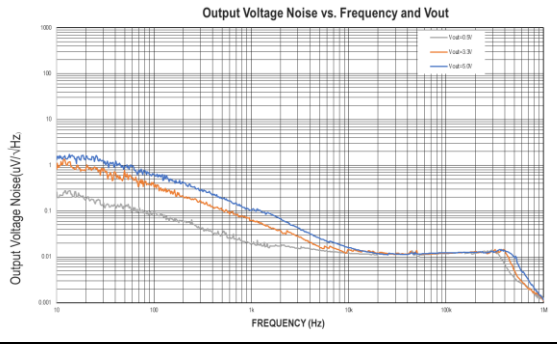


$$Vout = Vref * \left(1 + \frac{R1}{R2}\right)$$

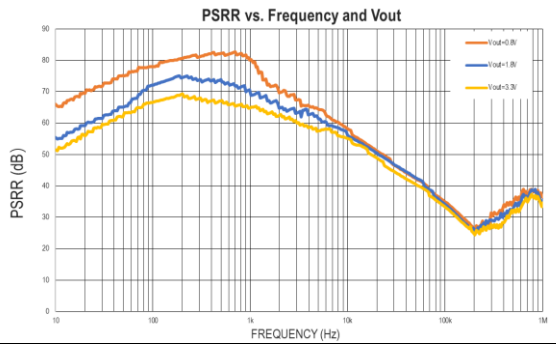
Table 4. Recommended Feedback-Resistor Values

Output Voltage (V)	External Resistor Divider Combinations	
	R1 (kohm)	R2 (kohm)
0.7	12.4	31
1	12.4	12.4
1.2	12.4	8.86
1.5	12.4	6.2
1.8	12.4	4.77
2.5	12.4	3.1
3.3	12.4	2.21
4.5	12.4	1.55
5	12.4	1.38

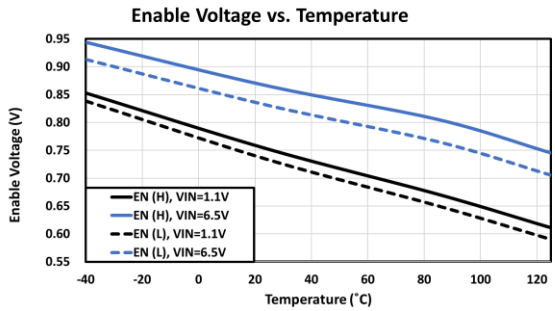
Typical Operating Characteristics



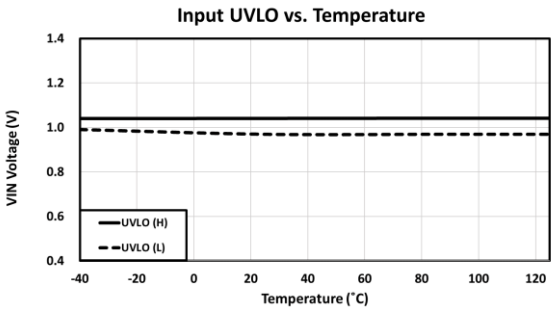
VOUT=0.5V/3.3V/5.0V
CIN=47uF, COUT=47uF//10uF//10uF
CFF=10nF, CNRSS=100nF



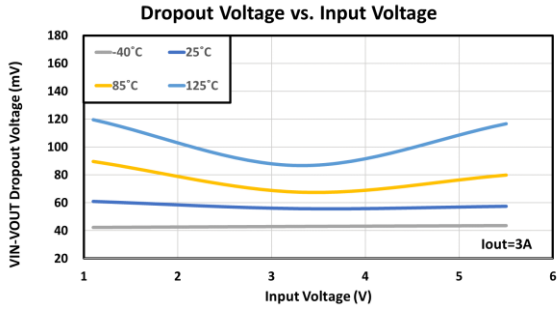
VIN=VOUT+0.4V, IOUT=3A, VOUT =0.8V/1.8V/3.3V
COUT=47uF//10uF//10uF
CFF=CNRSS=10nF



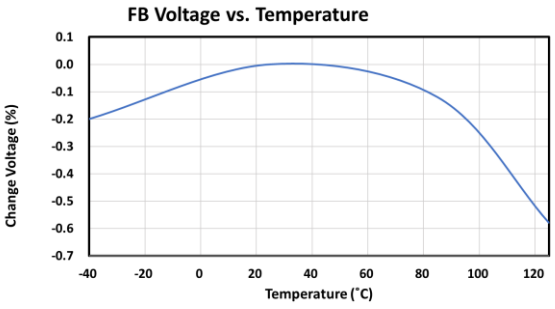
VIN=1.8V, VOUT=0.5V, IOUT=10mA



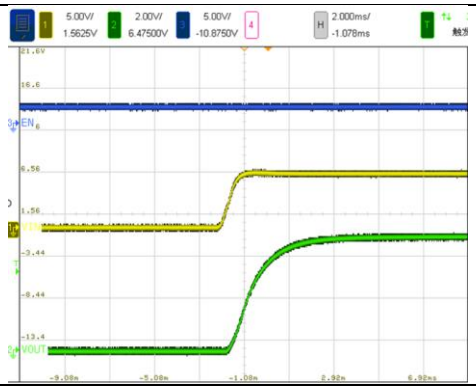
VOUT=0.5V, IOUT=10mA



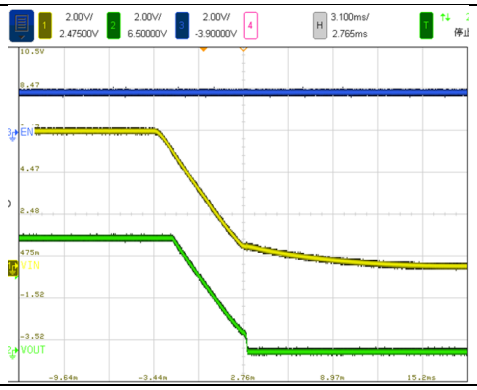
IOUT=3A



VIN=1.1V



VIN=6.5V, VOUT=5.5V, IOUT=3A
Power on



VIN=6.5V, VOUT=5.5V, IOUT=3A
Power off

Function Block Diagram

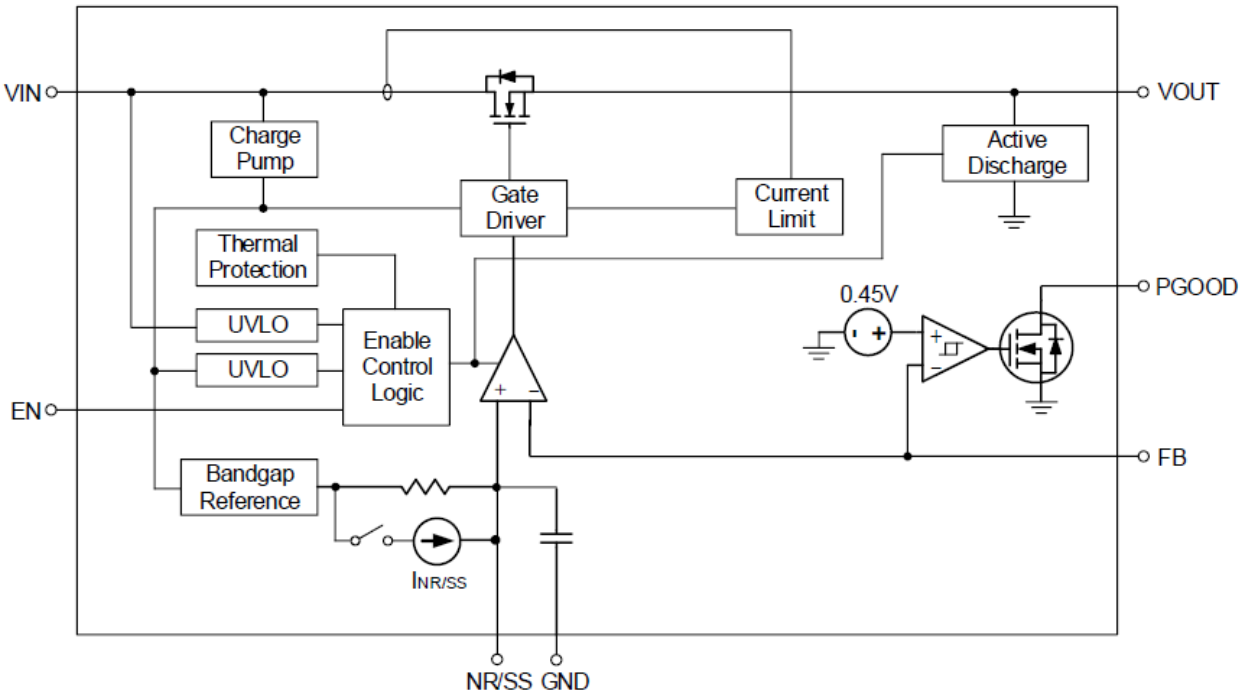


Figure 4. XPL3238A Block Diagram

Operation

The XPL3238 operates with single supply input ranging from 1.1V to 6.5V and is capable to deliver 3A current to the output. The device features high PSRR and low noise providing a clean supply to the application.

A low-noise reference and error amplifier are included to reduce device noise. The NR/SS capacitor filters the noise from the reference, and feed-forward capacitor filters the noise from the error amplifier. The high power-supply rejection ratio (PSRR) of the XPL3238 minimizes the coupling of input supply noise to the output.

Enable and Shutdown

The XPL3328 provides an EN pin, as an external chip enable control, to enable or disable the device. The regulator is turned off and enters the shutdown mode when VEN is below 0.5V. When VEN is above 1.1V, the regulator is turned on. When the regulator is shut down, the ground current is reduced to a maximum of 25uA. The enable circuitry has hysteresis (typically 20mV) for use with relatively slow ramping analog signals.

If the enable timing control is not used, connect EN to the largest capacitance on the input as close as possible to prevent voltage droops on the VIN line from triggering the enable circuit. The XPL3328 enables normal start-up even with a negative pre-bias voltage at output.

Programmable Soft Start

The noise-reduction capacitor (CNRSS) accomplishes dual purpose of noise-reduction and programming the soft-start ramp time during turn-on. When EN and UVLO exceed the respective threshold voltage, the XPL3238 activates a quick-start circuit to charge the noise reduction capacitor (CNRSS) and then the output voltage ramps up.

The soft-start ramp time can be calculated by equation as below:

$$tss = Vref * CNRSS/INRSS$$

Power Good

The power-good circuit monitors the feedback pin voltage to indicate the status of the output voltage. The open-drain PGOOD pin requires an external pull-up resistor to an external supply. Any downstream device can receive power-good as a logic signal that can be used for sequencing. The pull-up resistor from 10k Ω to 100k Ω is recommended. Make sure that the external pull-up supply voltage results in a valid logic signal for the receiving device or devices.

After start-up, the PGOOD pin becomes high impedance when the feedback voltage exceeds VTH_PGOOD (Typically 95% of 0.5V reference voltage level). The PGOOD is pulled to GND when the feedback pin voltage falls below the VTH_PGOOD, EN low, the current limit or OTP levels are reached.

Undervoltage Lockout

The UVLO circuit monitors the input voltage to prevent the device from turning on before VIN rises above the UVH threshold. The UVLO circuit also disables the output of the device when VIN falls below the lockout voltage (UVH − UVL). The UVLO circuit is activated to disable the output of the device if VIN collapses.

Internal Current Limit

The XPL3238 continuously monitors the output current to protect the pass transistor against abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to limit the output within the predefined range.
Thermal shutdown can be activated during a current limit event because of the high-power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances of the input and load. Continuous operation in current limit is not recommended.
With the build-in body diode, the pass transistor conducts current when the output voltage exceeds input voltage. Since the current is not limited, external current protection should be added if the device works at reverse voltage state.

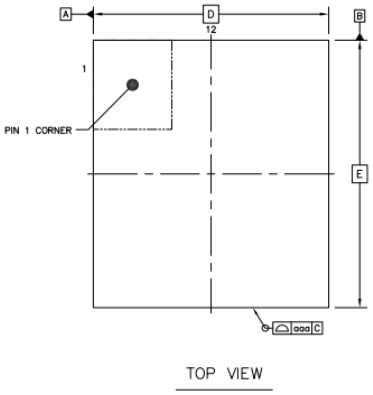
Over Temperature Protection

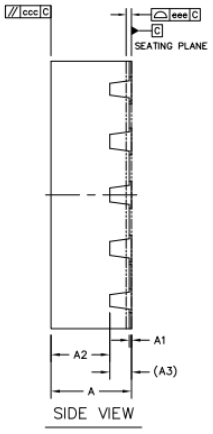
The XPL3238 implements thermal shutdown protection. The device is disabled when the junction temperature (TJ) exceeds 160˚C (typical). The LDO automatically turns on again when the temperature falls below 140˚C (typical).
For reliable operation, limit the junction temperature to a maximum of 125˚C. Continuously running the XPL3238 into thermal shutdown or above junction temperature of 125˚C reduces long-term reliability.

Output Active Discharge

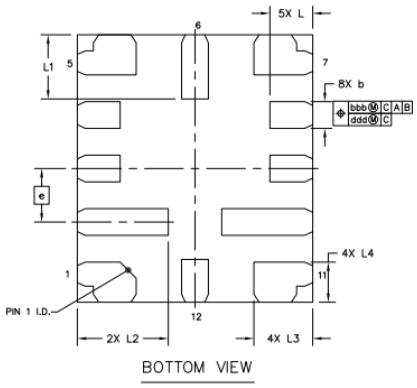
When the device is disabled, the XPL3238 discharges the LDO output (via VOUT pins) to ground through an internal impedance of several hundred ohms. Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. External current protection should be added if the device works at reverse voltage state.

Physical Dimensions





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		2.2 BSC	
	Y	E		2.5 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.55	0.6	0.65
		L2	0.8	0.85	0.9
		L3	0.5	0.55	0.6
		L4	0.325	0.375	0.425
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	



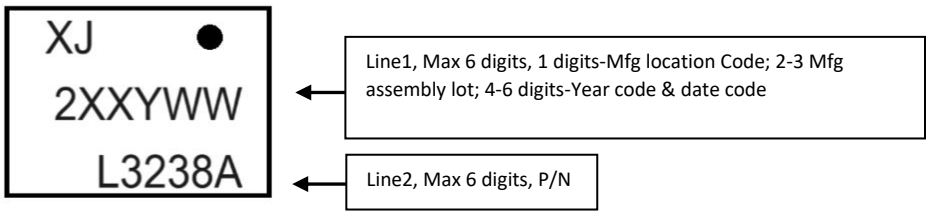
NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP · Sn8~20u

Marking And Reel Information

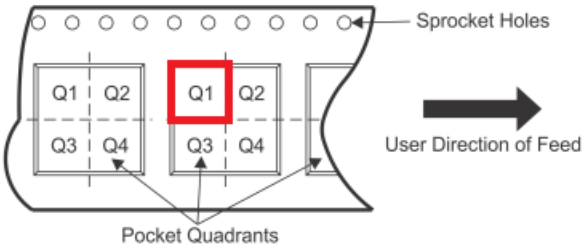
Package Marking & PQ information

XPL3238AQ12R Marking

Format:



Pin 1 located in Q1 direction in T&R (follow EIA-418)



Remark:

Font: Arial

Letter height of 0.5mm

Side pitch of 0.4mm

Line space of 0.25mm

Logo of XINJI should be required and placed on assigned Logo position as upside illustration.

Trace-ability Code:

1. Manufacturing Location Code + Assembly lot#+Year Code+WK code Line 1

a) 1st digit: Assembly location code: JCET: 2

b) 2nd & 3rd digit: Assembly lot number

XX means serial number for traceability, either of the 2 characters can be replaced by "0-9, A-Z, a-z"

c) 4th digit: Year code.

Year Code 2020-2051

Year	Code
2020	0
2021	1
2022	2
2023	3
2024	4
2025	5
2026	7
2027	C

Year	Code
2028	D
2029	E
2030	F
2031	H
2032	I
2033	J
2034	K
2035	L

Year	Code
2036	N
2037	P
2038	R
2039	S
2040	T
2041	U
2042	V
2043	X

Year	Code
2044	Y
2045	Z
2046	b
2047	c
2048	d
2049	h
2050	i
2051	j

d)5th & 6th digit: Week code, 01 means the 1st Work Week based on XinJi's calendar.

WK01 means the 1st Work Week based on XinJi's calendar.

2. Product Number Code: Line 2

Product Name	P/N Code	Remark
XPL3238AQ12R	L3238A	

3. Packing: 3k/Reel