

I²S/TDM Input, 10.25V BOOST Digital Smart K Audio Amplifier with Speaker Voltage and Current Sense

FEATURES

- **Smart BOOST with total efficiency up to 83%**
- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 11 μ V**
- **THD+N: 0.02%**
- **Speaker Voltage and Current monitor and feedback with I²S/TDM interface**
- Supports 6 Ω Speaker
- Extensive Pop-Click Suppression
- Volume control (from -96dB to 0dB)
- I²S/TDM interface:
 - I²S, Left-Justified and Right-Justified
 - Supports 1/2/4/6/8 slots TDM
 - Input Sample Rates from 8kHz to 96kHz
 - Data Width: 16, 20, 24, 32 Bits
- Ultrasonic support with sample frequency of 96kHz
- I²C-bus control interface(400kHz)
- Power Supplies:
 - VBAT: 3.0V-5.5V
 - DVDD: 1.65V~1.95V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- FCQFN 2.5mm X 2.5mm-25L package

APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

DESCRIPTION

The AW88265 is an I²S/TDM input, high efficiency digital Smart K audio amplifier with an integrated 10.25V smart boost converter. Due to its 11 μ V noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 5.2W output power into an 8 Ω speaker at 1% THD+N.

The AW88265 integrates a high-efficiency smart boost converter as the Class-D amplifier supply rail. The output voltage of boost converter can be adjusted smartly according to the input amplitude, which extremely improves the efficiency without clipping distortion.

The AW88265 features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I²C-bus interface, and the device address is configurable.

The AW88265 offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

AW88265 is available in a FCQFN 2.5mm X 2.5mm-25L package.

PIN CONFIGURATION AND TOP MARK

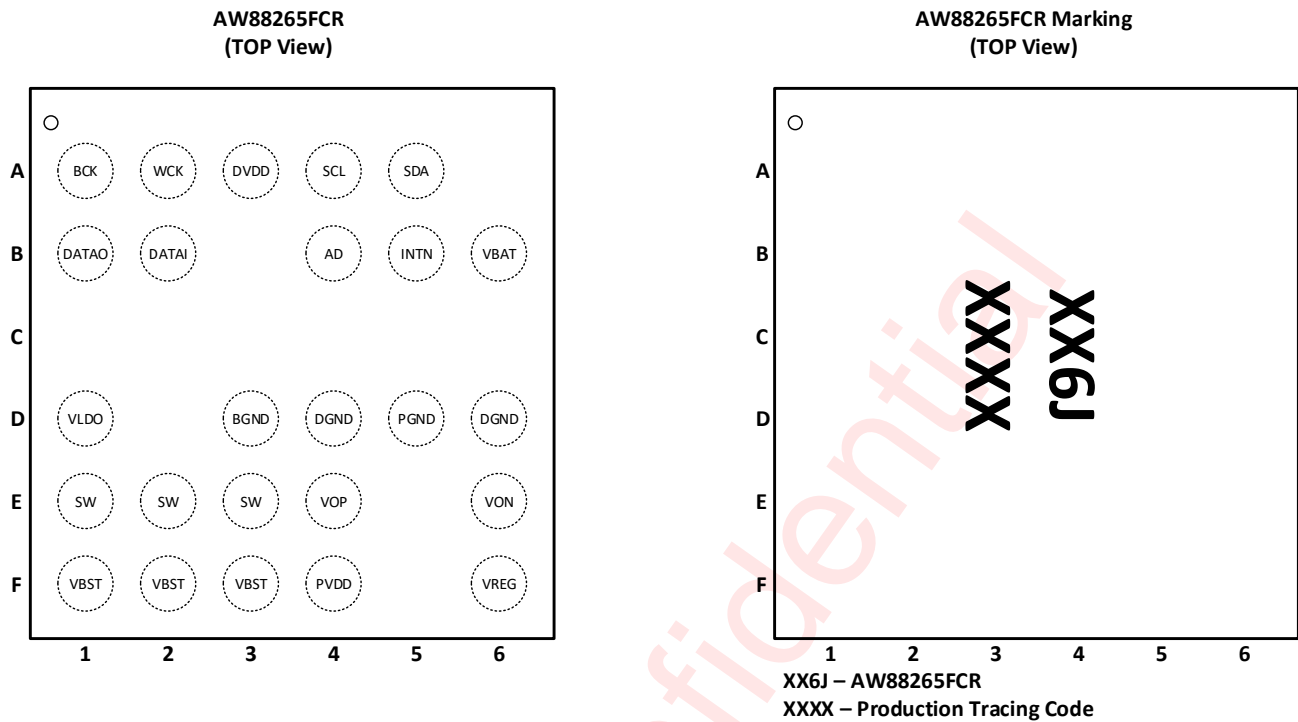


Figure 1 AW88265FCR pin diagram top view and device marking

PIN DESCRIPTION

Pin No	Pin Name	Description
A1	BCK	I ² S/TDM bit clock input
A2	WCK	I ² S word select input / TDM frame sync signal
A3	DVDD	Digital power supply
A4	SCL	I ² C clock input
A5	SDA	I ² C data IO
B1	DATAO	I ² S/TDM data out
B2	DATAI	I ² S/TDM data input
B4	AD	I ² C address select input
B5	INTN	Interrupt output
B6	VBAT	Battery power supply
D1	VLDO	Digital core voltage regulator output
D3	BGND	Boost GND
D4,D6	DGND	Digital GND
D5	PGND	Power GND

Pin No	Pin Name	Description
E1,E2,E3	SW	Boost switch pin
E4	VOP	Non-inverting Class-D output
E6	VON	Inverting Class-D output
F1,F2,F3	VBST	Boost output
F4	PVDD	Power supply voltage
F6	VREG	Voltage output of regulator

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FUNCTIONAL BLOCK DIAGRAM

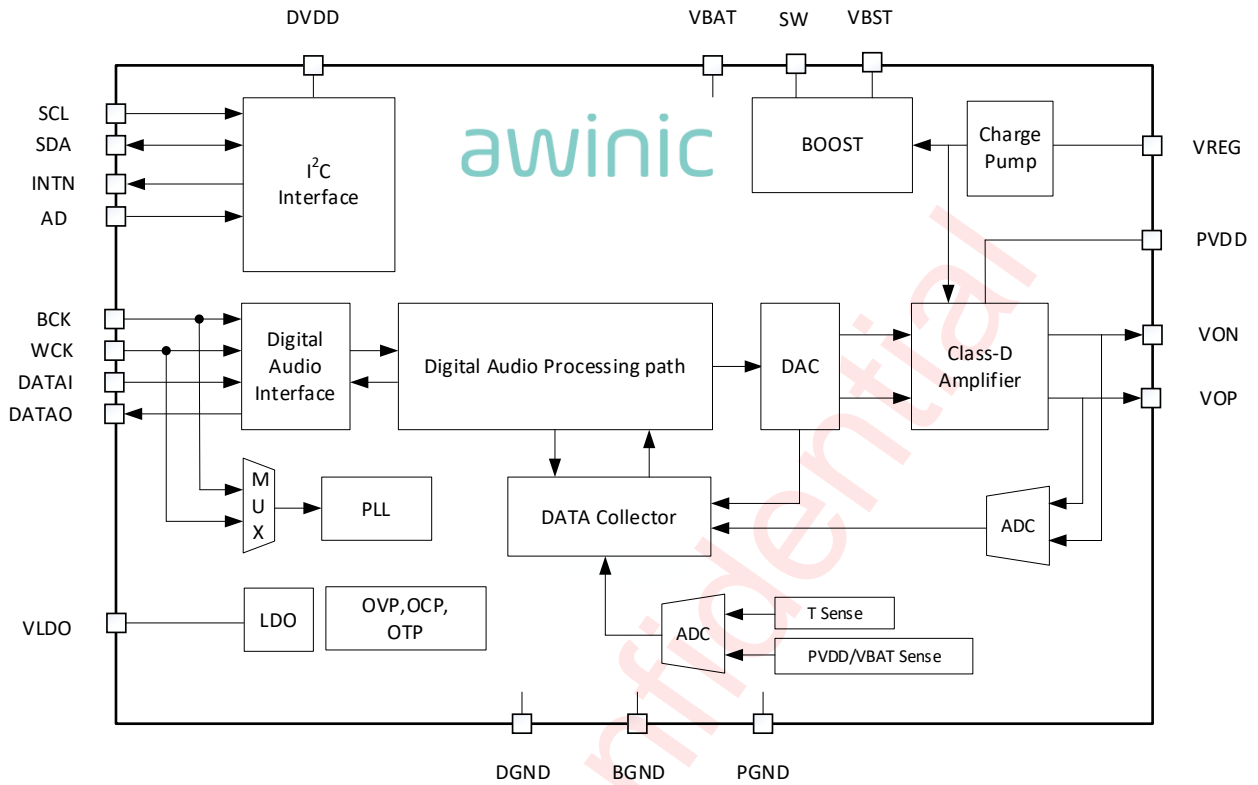


Figure 2 FUNCTIONAL BLOCK DIAGRAM

APPLICATION DIAGRAM

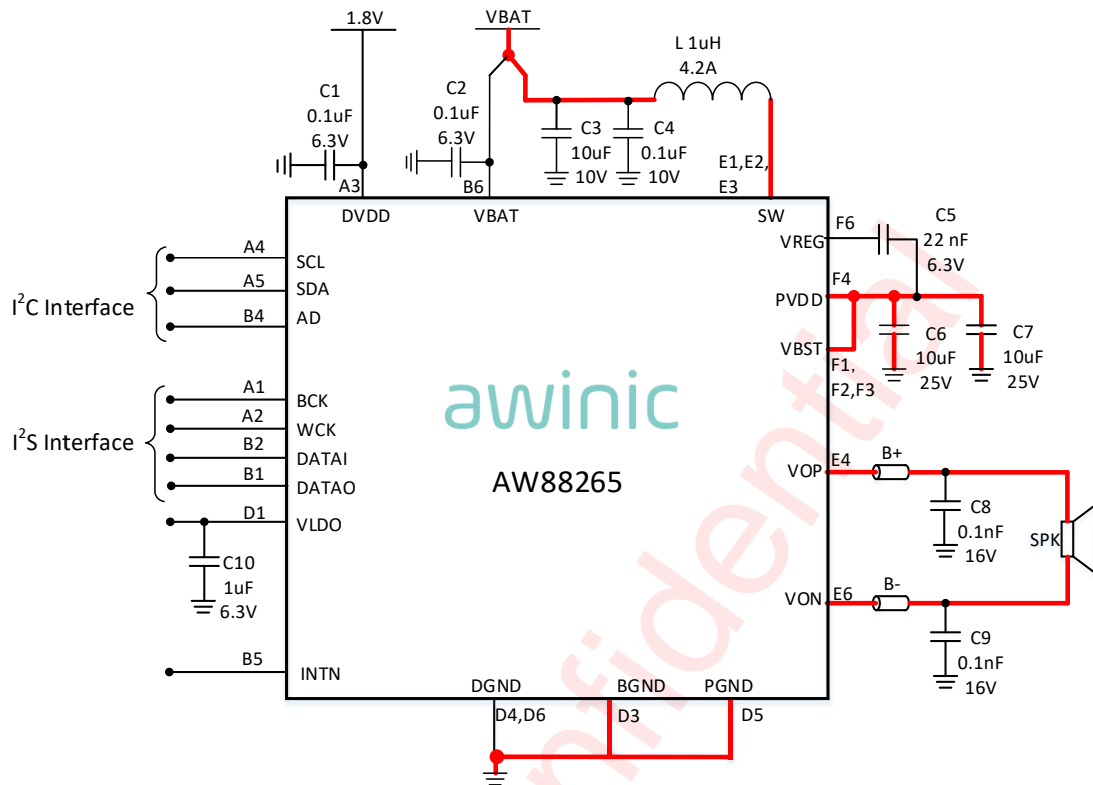


Figure 3 AW88265 Application Circuit

Note: Traces carry high current are marked in red in the above figure

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ORDERING INFORMATION

Product Type	Temperature	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW88265FCR	-40°C ~ 85°C	FCQFN 2.5X2.5-25L	XX6J	MSL1	RoHS+HF	4500 units/ Tape and Reel

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ABSOLUTE MAXIMUM RATING(NOTE1)

Parameter	Range
Battery Supply Voltage V_{VBAT}	-0.3V to 6V
Digital Supply Voltage V_{DVDD}	-0.3V to 2V
Boost output voltage V_{PVDD}	-0.3 to 13V
Boost SW pin voltage	-0.3 to V_{PVDD} (Note 2)
VOP/VON pin voltage	-0.3 to V_{PVDD} (Note 2)
Minimum load resistance R_L	5 Ω
Package Thermal Resistance θ_{JA}	60°C/W
Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature Range T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating (Note 3,4)	
HBM (Human Body Model)	±2000V
CDM (Charge Device Model)	±1000V
Latch-up	
Test Condition: JEDEC STANDARD NO.78E SEPTEMBER 2016	+IT: 450mA -IT: -450mA

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: SW/VOP/VON pin can handle 16V transients for less than 5ns

Note 3: The human body model is a 100pF capacitor discharged through a 1.5k Ω resistor into each pin. Test method: MIL-STD-883J Method 3015.9

Note 4: Test method: JEDEC EIA/JESD22-C101F

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS

Test condition: $T_A=25^{\circ}\text{C}$, $V_{BAT}=3.6\text{V}$, $DVDD=1.8\text{V}$, $PVDD=10.25\text{V}$, $R_L=8\Omega+33\mu\text{H}$, $f=1\text{kHz}$ (unless otherwise noted)

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
V_{VBAT}	Battery supply voltage	On pin VBAT	3.0		5.5	V
V_{DVDD}	Digital supply voltage	On pin DVDD	1.65	1.8	1.95	V
I_{VBAT}	Battery supply current	Operating mode		7.5		mA
		Standby mode		5		μA
		Power down mode, $DVDD=0\text{V}$		0.6	2	μA
I_{DVDD}	Digital supply current	Operating mode		3.5		mA
		Power down mode		4		μA
Boost						
V_{PVDD}	Boost output voltage			10.25 ^(Note1)		V
V_{OVP}	Over-voltage threshold			$V_{PVDD}+0.5$		V
	OVP hysteresis voltage			500		mV
I_{L_PEAK}	Inductor peak current limit			4 ^(Note1)		A
F_{BST}	Operating Frequency	$f_s = 48\text{KHz}$		2		MHz
D_{MAX}	The maximum duty cycle			90		%
η_{BST}	Boost converter efficiency	$V_{BAT}=4.2\text{V}$, $PVDD = 10.25\text{V}$, $I_{load} = 0.5\text{A}$, SmartBoost		88		%
Class-D						
R_{dson}	Drain-Source on-state resistance	High side MOS + Low side MOS		300		$\text{m}\Omega$
P_o	Speaker Output Power	THD+N=1%, $R_L=8\Omega+33\mu\text{H}$, $V_{BAT}=4.2\text{V}$, $PVDD=10.25\text{V}$		5.2		W
		THD+N=10%, $R_L=8\Omega+33\mu\text{H}$, $V_{BAT}=4.2\text{V}$, $PVDD=10.25\text{V}$		6.5		W
		THD+N=1%, $R_L=6\Omega+33\mu\text{H}$, $V_{BAT}=4.2\text{V}$, $PVDD=10.25\text{V}$		5.4		W
		THD+N=10%, $R_L=6\Omega+33\mu\text{H}$, $V_{BAT}=4.2\text{V}$, $PVDD=10.25\text{V}$		6.7		W
V_{OS}	Output offset voltage	I ² S signal input 0	-10	0	10	mV
F_{PWM}	PWM Switching frequency	Typical Sample Rate: 48kHz		384		kHz
η	Total efficiency (Class-D)	$V_{BAT}=4.2\text{V}$, $P_o=0.48\text{W}$, $R_L=8\Omega+33\mu\text{H}$		87		%

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
	Total efficiency (SmartBoost+Class-D)	VBAT=4.2V, Po=1W, RL=8Ω+33μH		83		%
THD+N	Total harmonic distortion plus noise	VBAT=4.2V, Po=1W, RL=8Ω+33μH, f=1kHz, PVDD=10.25V		0.02		%
EN	Speaker Mode Output noise	A-weighting		16		μV
	Receiver Mode Output noise	A-weighting		11		μV
FR _{amp}	Frequency response flatness (Note2)	SPK(20Hz-20kHz), Po=1W		0.3		dB
		SPK(20Hz-40kHz), Po=1W		1.0		dB
		RCV(20Hz-20kHz), Po=0.5W		0.15		dB
		RCV(20Hz-40kHz), Po=0.5W		0.4		dB
SNR	Signal-to-noise ratio	VBAT=4.2V, PVDD=10.25V, Po=5.2W, RL=8Ω+33μH, A-weighting		112		dB
PSRR	Power supply rejection ratio	Receiver Mode, VBAT=4.2V, V _{p-p,sin} =200mV	217Hz	85		dB
			1kHz	80		dB
Current Sense						
ISNS_FS	Current sense full scale			3.3		A
SNR	Signal-to-noise ratio	I _{peak} =1A, RL=8Ω+33μH, A-weighting		65		dB
THD+N	Total harmonic distortion plus noise	Po=1W, RL=8Ω+33μH		0.4		%
ΔISNS	Current sense accuracy	Po=1W, RL=8Ω+33μH		2		%
Digital Logical Interface						
V _{IL}	Logic input low level	BCK, WCK, DATAI Pin			0.3 x V _{DVDD}	V
V _{IH}	Logic input high level		0.7 x V _{DVDD}		V _{DVDD}	V
V _{IL}	Logic input low level	SCL, SDA, AD Pin			0.3 x V _{DVDD}	V
V _{IH}	Logic input high level		0.7 x V _{DVDD}		3.6	V
V _{OL}	Logic output low level	I _{OUT} =4mA			0.45	V
V _{OH}	Logic output high level	I _{OUT} =-4mA	V _{DVDD} - 0.45		V _{DVDD}	V
Protection						

Symbol	Description	Test Conditions	Min	Typ.	Max	Units
T _{SD}	Over temperature protection threshold			150		°C
T _{SDR}	Over temperature protection recovery threshold			130		°C
UVP	Under-voltage protection voltage			2.4		V
	Under-voltage protection hysteresis voltage			200		mV

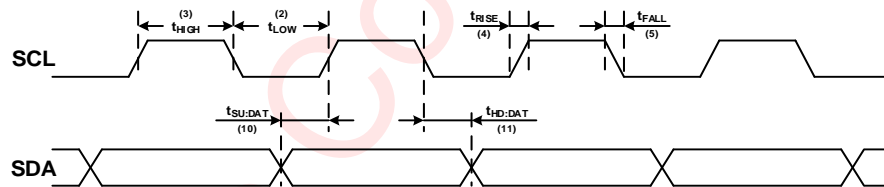
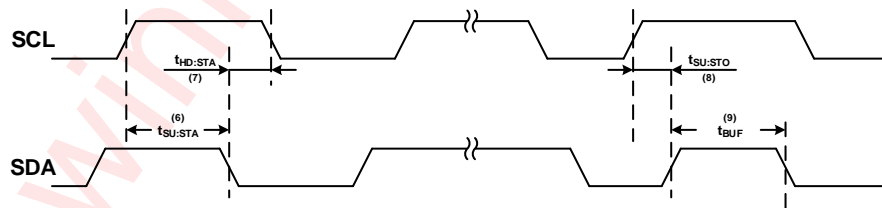
Note 1: Registers are adjustable; Refer to the list of registers.

Note 2: FS=96KHz when the amplitude response variation is 20Hz-40kHz.

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I²C INTERFACE TIMING

Parameter			MIN	TYP	MAX	UNIT
No.	Sym	Name				
1	f _{SCL}	SCL Clock frequency			400	kHz
2	t _{LOW}	SCL Low level Duration	1.3			μs
3	t _{HIGH}	SCL High level Duration	0.6			μs
4	t _{RISE}	SCL, SDA rise time			0.3	μs
5	t _{FALL}	SCL, SDA fall time			0.3	μs
6	t _{SU:STA}	Setup time SCL to START state	0.6			μs
7	t _{HD:STA}	(Repeat-start) Start condition hold time	0.6			μs
8	t _{SU:STO}	Stop condition setup time	0.6			μs
9	t _{BUF}	the Bus idle time START state to STOP state	1.3			μs
10	t _{SU:DAT}	SDA setup time	0.1			μs
11	t _{HD:DAT}	SDA hold time	10			ns

**Figure 4 SCL and SDA timing relationships in the data transmission process****Figure 5 The timing relationship between START and STOP state**

DIGITAL AUDIO INTERFACE TIMING

Parameter Name		Min	Typ.	Max	Units
f_s	sampling frequency, on pin WCK	8		96	kHz
f_{bck}	Bit clock frequency, on pin BCK	$32 \cdot f_s$		$128 \cdot f_s$	Hz
t_{su}	WCK, DATAI Setup time to BCK	10			ns
t_h	WCK, DATAI hold time to BCK	10			ns
t_d	DATAO output delay time to BCK			50	ns

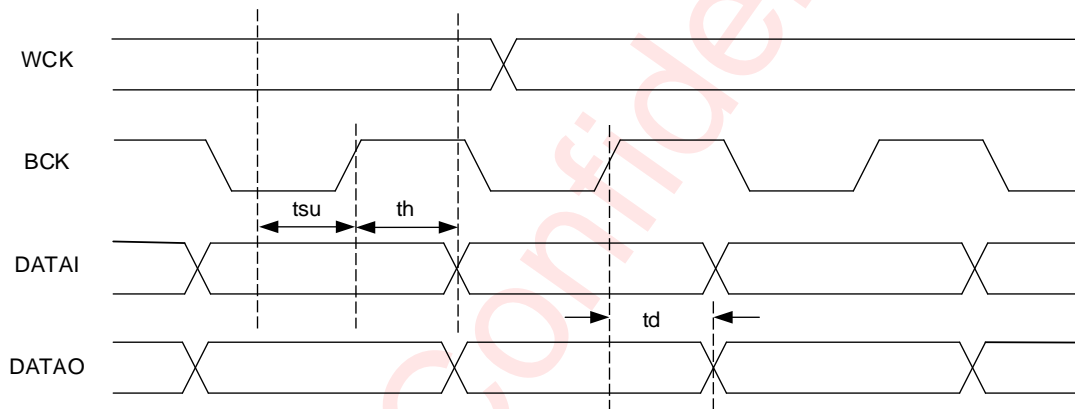
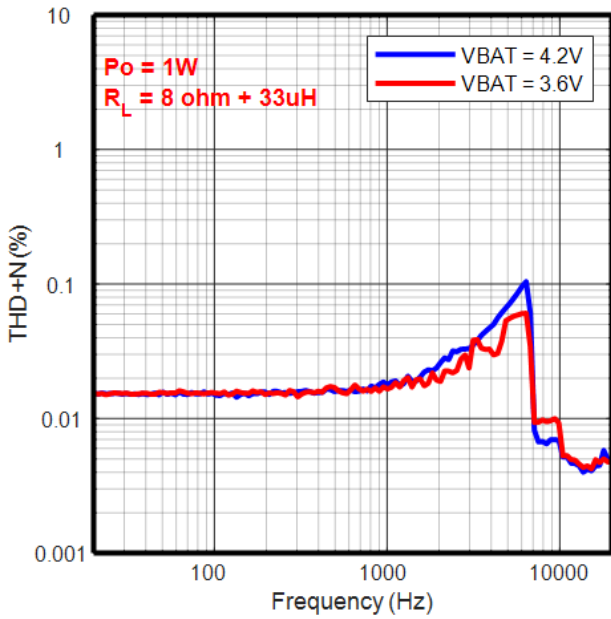


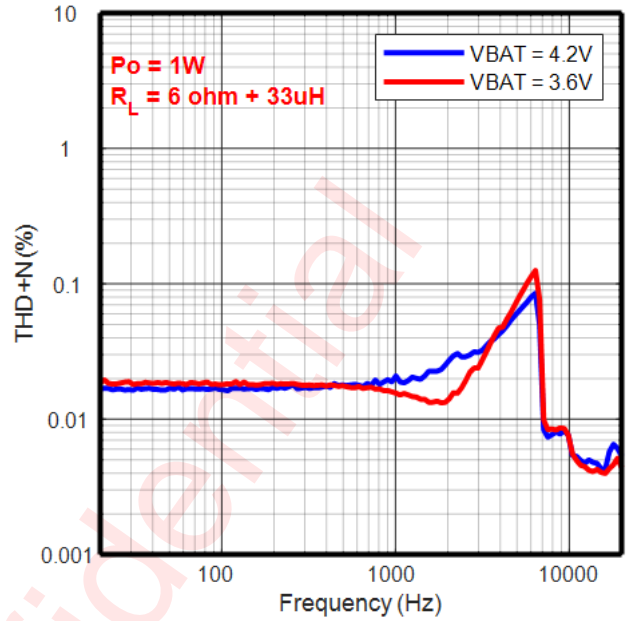
Figure 6 Digital Audio Interface Timing

TYPICAL CHARACTERISTIC CURVES

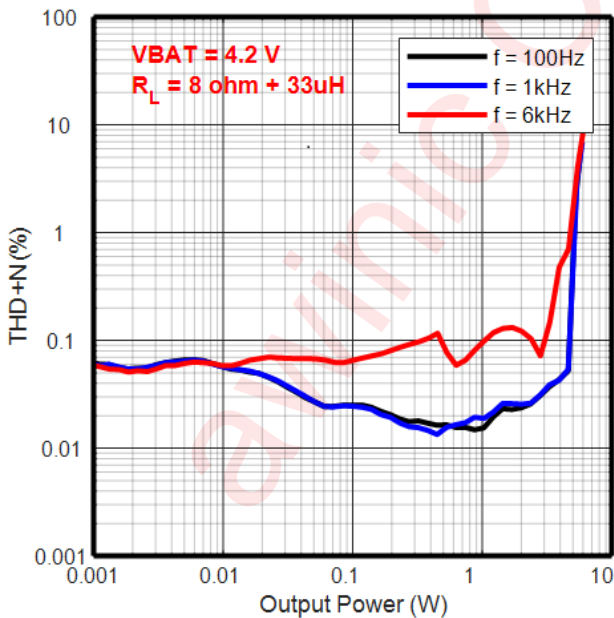
THD+N VS. FREQUENCY



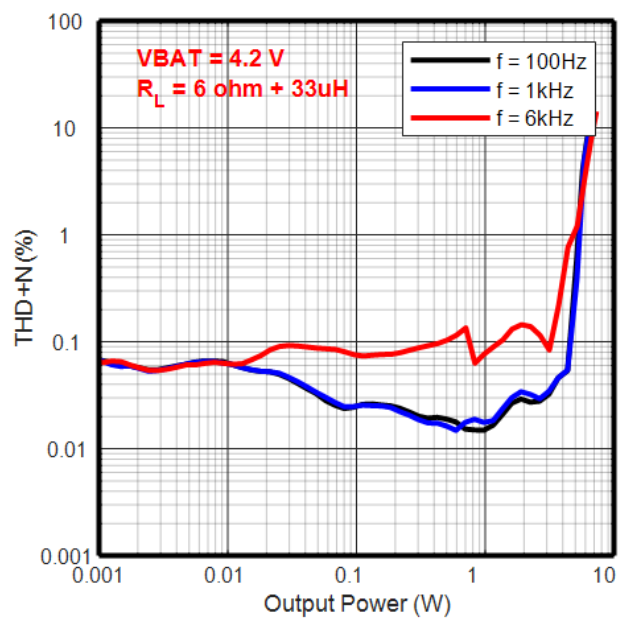
THD+N VS. FREQUENCY



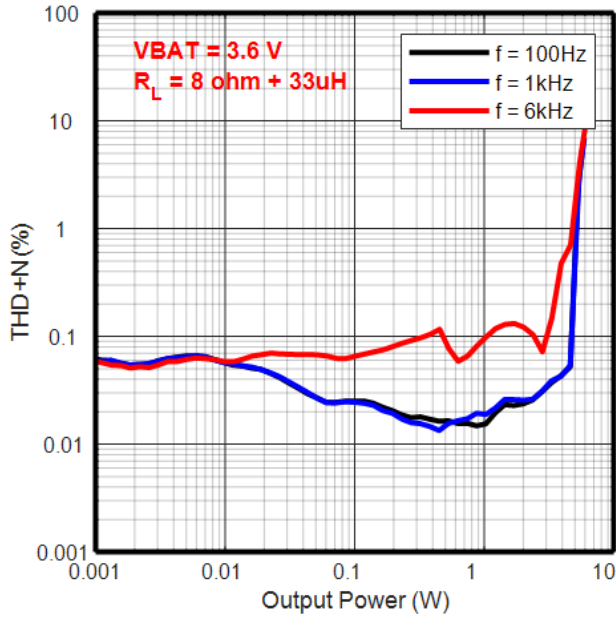
THD+N VS. OUTPUT POWER



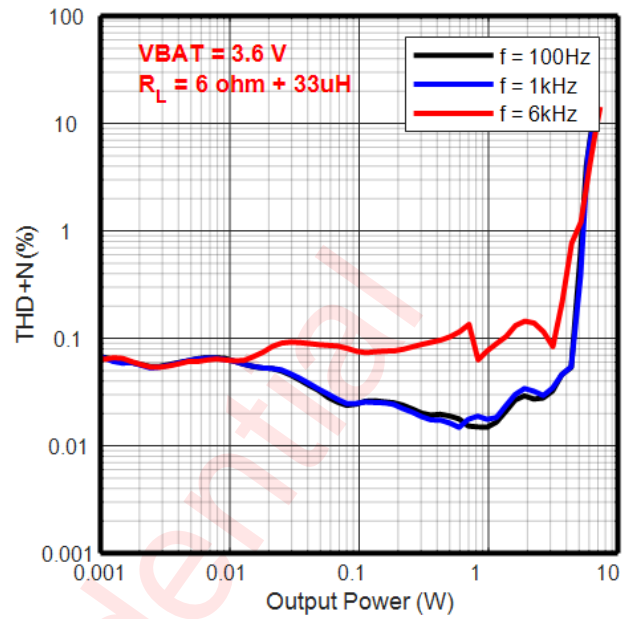
THD+N VS. OUTPUT POWER



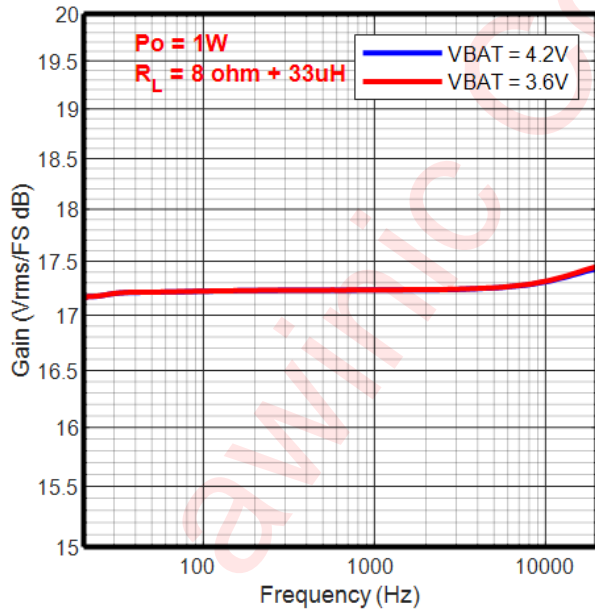
THD+N VS. OUTPUT POWER



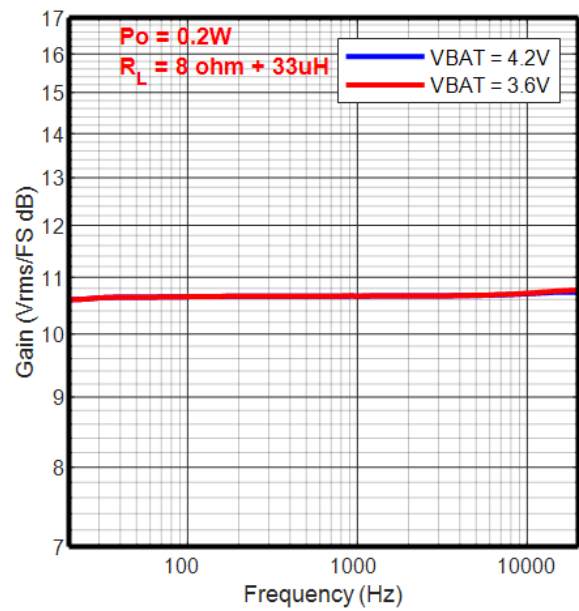
THD+N VS. OUTPUT POWER



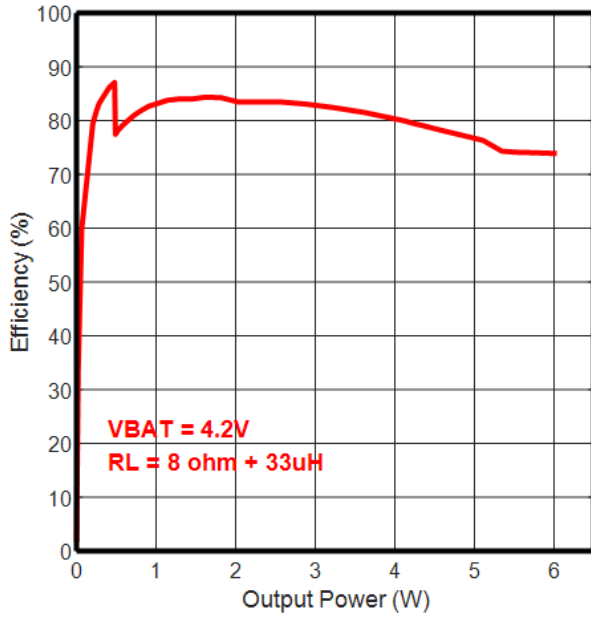
SPEAKER GAIN VS. FREQUENCY



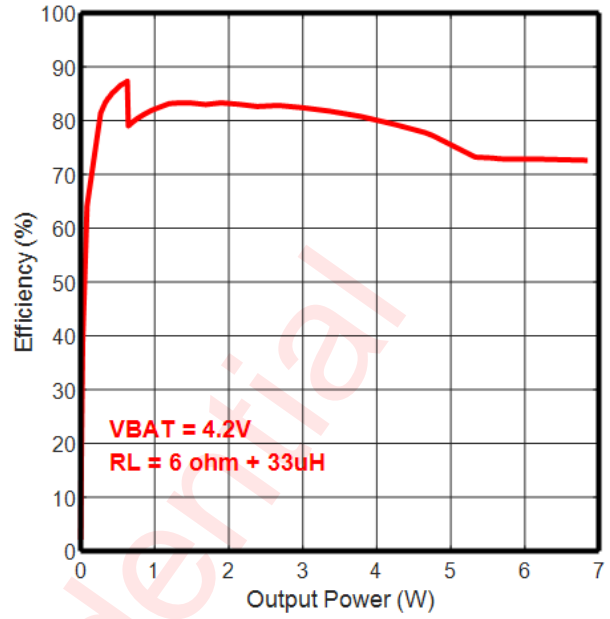
RECEIVER GAIN VS. FREQUENCY



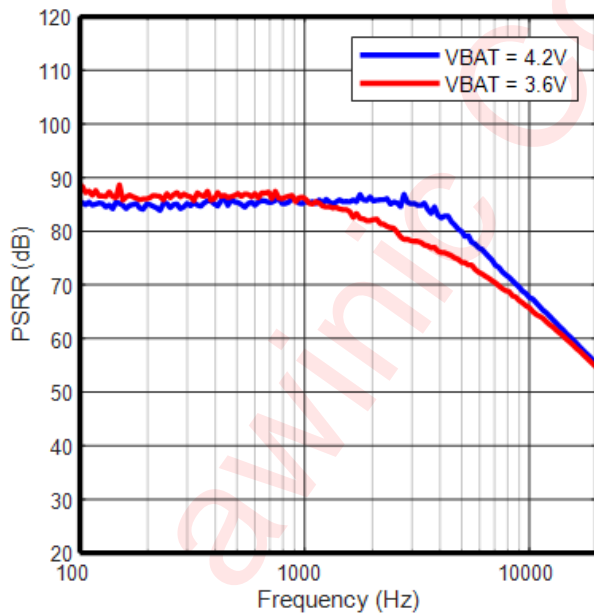
EFFICIENCY VS. OUTPUT POWER



EFFICIENCY VS. OUTPUT POWER



RECEIVER PSRR VS. FREQUENCY



DETAIL FUNCTIONAL DESCRIPTION

POWER ON RESET

The device provides a power-on reset feature that is controlled by VBAT and DVDD supply voltage. When the VBAT supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The internal reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

OPERATION MODE

The device supports 4 operation modes.

Table 1 Operating Mode

Mode	Condition	Description
Power-Down	$V_{VBAT} < 2.1V$ $V_{DVDD} < 1.1V$	Power supply is not ready, chipset is power down.
Stand-By	$V_{VBAT} > 3V$ $V_{DVDD} > 1.65V$	Power supply is ready, most parts of the device are power down for low power consumption except I ² C interface
Configuring	PWDN = 0	Device is biased while boost and Class-D output is floating. System configuration carried out in this mode
Operating	AMPDP = 0	Amplifier is fully operating

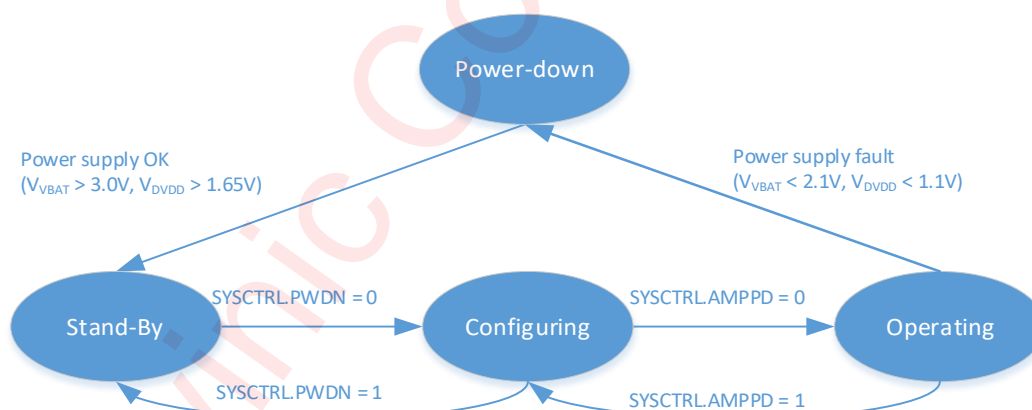


Figure 7 Device operating modes transition

POWER-DOWN MODE

The device switches to power-down mode when any of the following events occurred:

- $V_{DVDD} < 1.1V$
- $V_{VBAT} < 2.1V$

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

$V_{DVDD} > 1.65\text{ V}$ and $V_{VBAT} > 3\text{ V}$

STAND-BY MODE

The device switches stand-by mode when the power supply voltages are OK. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

CONFIG MODE

The device switches to OFF mode when:

- SYSCTRL.PWDN = 0;
- SYSCTRL.AMPPD = 1;

In this mode the internal bias, OSC, PLL will start to work

OPERATING MODE

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.

This device power up sequence is illustrated in the following figure:

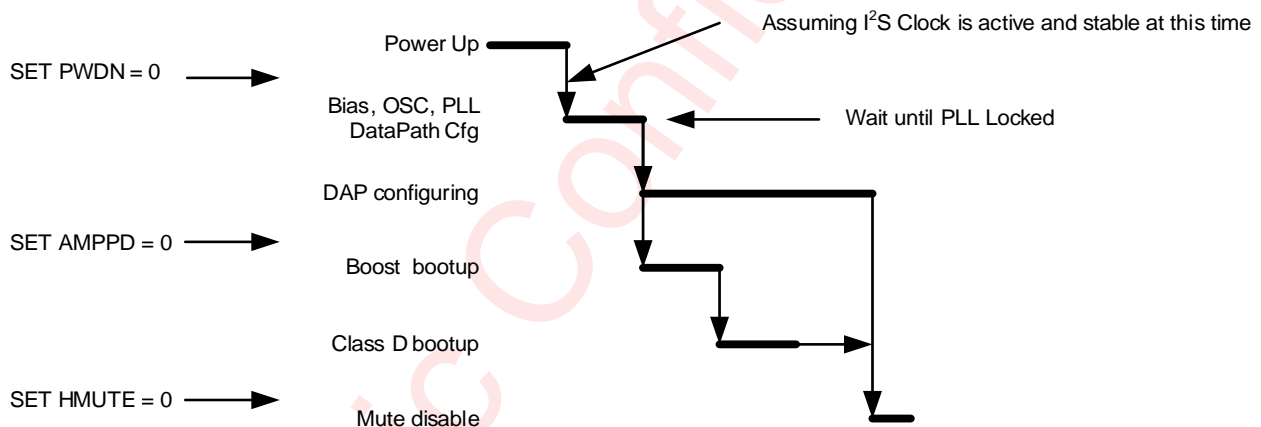


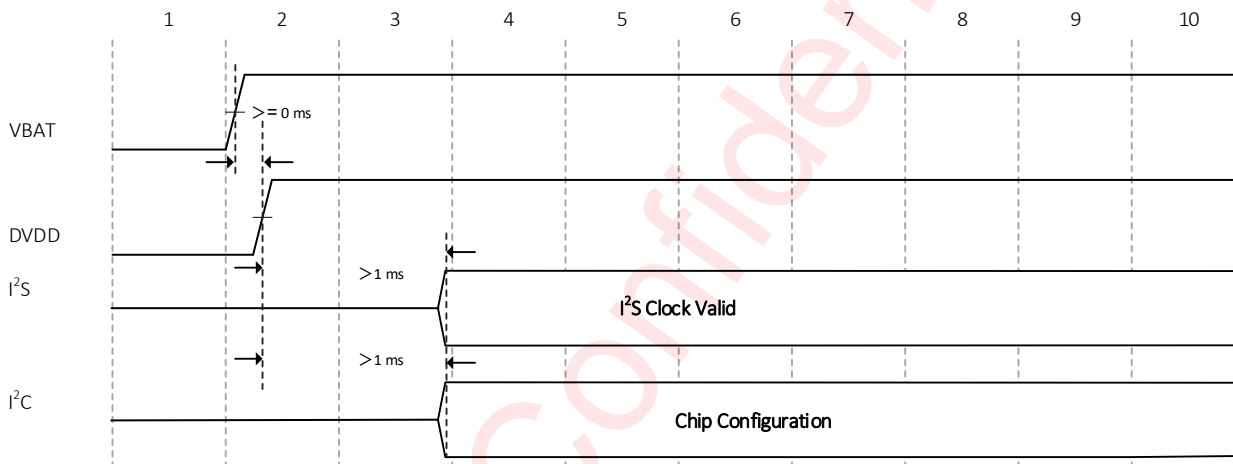
Figure 8 Power up sequence

Detail description for each step is listed in the following table.

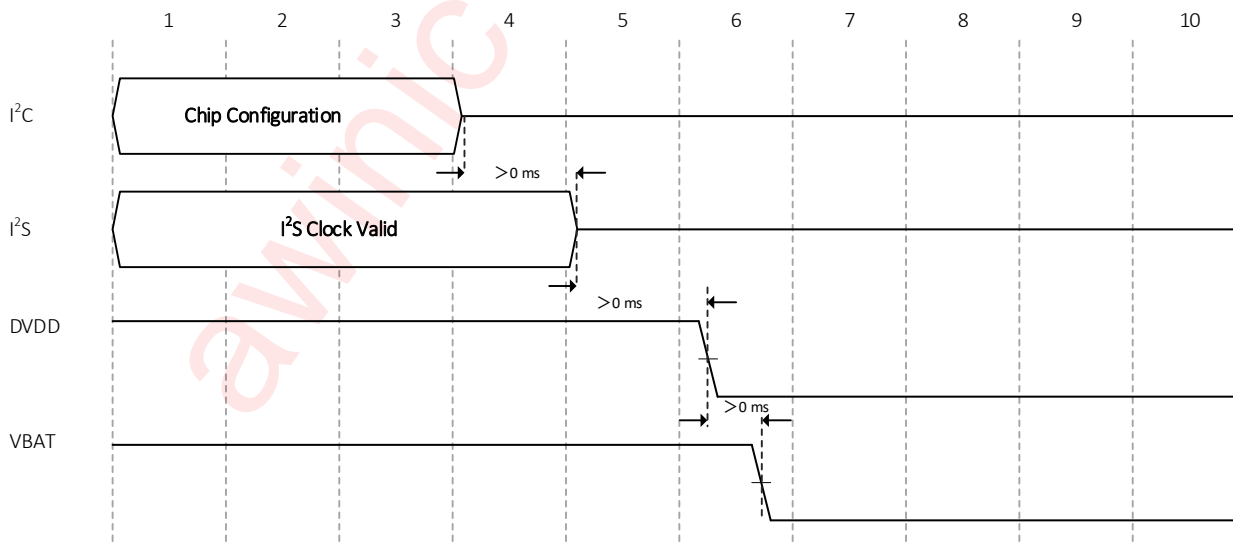
Table 2 Detail Description of Power up sequence

Index	description	Mode
1	Wait for VBAT、DVDD supply power up	Power-Down
2	I ² S + Data Path Configuration	Stand-By
3.1	Enable system (SYSCTRL.PWDN = 0)	Configuring
3.2	Active Bias, OSC and PLL	
3.3	Wait for PLL to be locked	
4.1	Enable Boost and amplifier (SYSCTRL.AMPPD = 0) Boost and Amplifier boot up	Operating
4.2	Wait for SYSST.SWS = 1	
5	Release Hard-Mute Data Path active	

Power up sequence considering I²S, I²C timing shows as below:



Power down sequence considering I²S, I²C timing shows as below:



SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I²C interface will reset the device internal circuits and all configuration registers.

DIGITAL AUDIO INTERFACE

The state of each digital input and output are shown in below table. After power on, the input signal pin BCK, WCK, DATAI are set to high impedance by default. If I2STXEN bit is enabled, DATAO is actively driven when outputting data otherwise it is high impedance by default.

Digital I/O	Type	Description (Default State)
SCL	Input	Hi-Z
SDA	Input	Hi-Z
INTN	Output	Hi-Z
AD	Input	Weak pull down
BCK	Input	Hi-Z
WCK	Input	Hi-Z
DATAI	Input	Hi-Z
DATAO	Output	Hi-Z

DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATAI
- DATAO

Two-slot I²S and 1/2/4/6/8-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I²S are supported, including standard I²S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL1.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL1.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz. It is selected via configurable register I2SCTRL1.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL1.I2SBCK. The frequency of BCK can be calculated according to the following equation:

$$BCK \text{ frequency} = \text{SampleRate} * \text{SlotLength} * \text{SlotNumber}$$

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I²S mode, 4-slot supported in TDM mode.

The word select and bit clock signals of the I²S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL1.CHSEL.

Table 3 Supported I²S interface parameters

Interface format(MSB first)	Data width	BCK frequency
Standard I ² S	16b/20b/24b/32b	32fs/48fs /64fs
left-justified	16b/20b/24b/32b	32fs/48fs /64fs
right-justified	16b/20b/24b/32b	32fs /48fs /64fs

The output port DATA0, can be enabled or disabled via bit I2SCTRL3.I2STXEN. The unused slots can be set to Hi-z or zero, which is controlled by I2SCTRL3.DOZH.

STANDARD I²S MODE

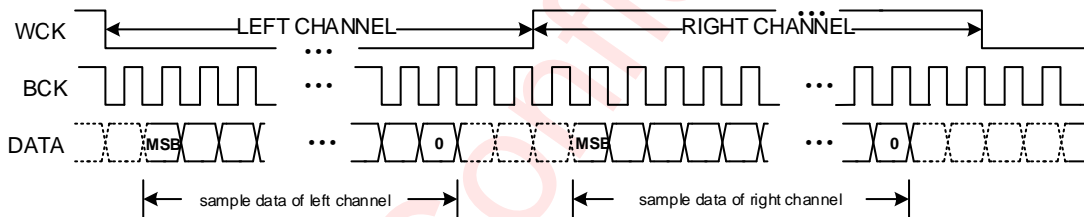


Figure 9 I²S Timing for Standard I²S Mode

- When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.
- The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

LEFT-JUSTIFIED MODE

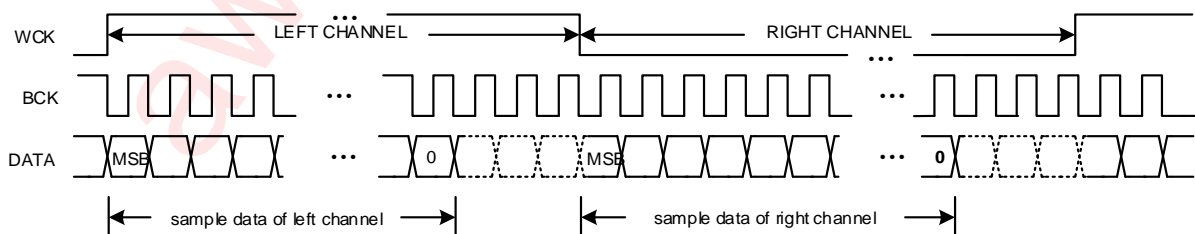


Figure 10 I²S Timing for Left-Justified Mode

- When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.

- The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

RIGHT-JUSTIFIED MODE

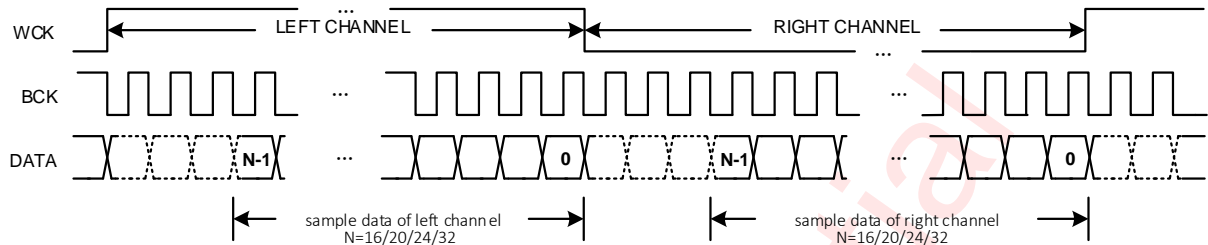


Figure 11 I²S Timing for Right-Justified Mode

- When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data.
- The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

TDM MODE

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 4-slot is supported in TDM mode, while 2-slot is supported in I²S mode

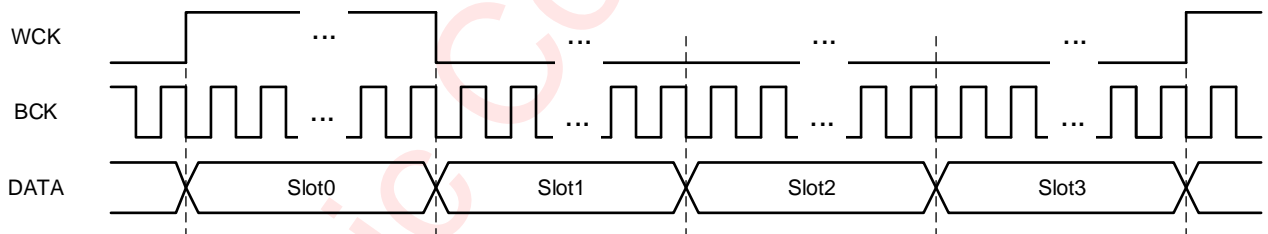


Figure 12 TDM Timing

Note: The high level pulse width of WCK signal can be one slot time or one period of BCK.

DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- HDCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the DAP (Digital Audio Processor) is illustrated in the following figure.

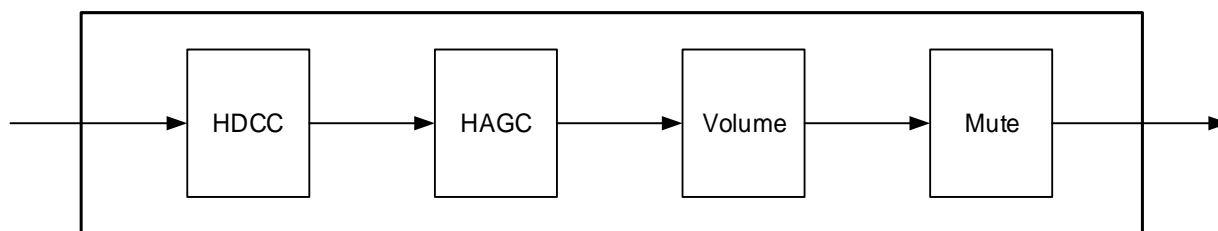


Figure 13 Block Diagram of DAP

HDCC

This module performs hardware DC canceling for the input audio stream. It blocks DC components into analog class D loop.

HAGC

System output power tends to be more than rated power of speaker, such as in the 10.25V power supply, as for 8Ω speaker, the maximum undistorted power is about 5.2W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with hardware AGC can protect the speaker effectively, When the output power is not exceeding the setting threshold, the hardware AGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the hardware AGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

VOLUME CONTROL

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -95.875db with 0.125db/step

MUTE

This module performs mute control for the audio stream

DC-DC CONVERTER

This device using smart boost converter generates the amplifier supply rail, working in 1.6MHz. The DC-DC converter can work in different mode via BSTCTRL1.BST_MODE:

- **Pass-through mode:** the voltage of VBAT is transparently passed to output of converter PVDD
- **Force boost mode:** the output voltage is boosted to the programmed output voltage
- **Smart boost 1 mode:** the output voltage can be switch between VBAT and programmed output voltage according to the input audio level.
- **Smart boost 2 mode:** the output voltage can be dynamically adjusted according to the amplifier output's signal swing requirements in order to maximize efficiency.

Pass-through mode

The internal boost circuit is not working; the voltage of VBAT is passed to PVDD directly.

Force boost mode

The boost circuit is always working and converts the voltage of VBAT to the programmed output voltage. The output voltage is configured via BSTCTRL2.VOUT_VREFSET

Smart boost 1 mode

Smart boost 1 mode can dynamically turn on or off the boost according to the amplifier output's signal swing requirements in order to maximize efficiency.

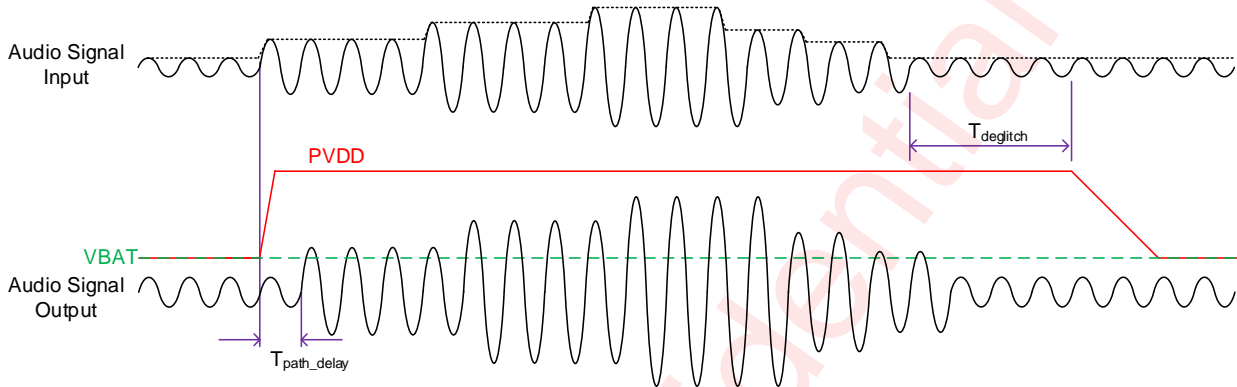


Figure 14 Boost Circuit Behavior in Smart Boost 1 Mode

Smart boost 2 mode

The boost circuit works dynamically according to the output audio level. When the level of output audio signal is below the setting threshold, the boost circuit will not be activated. Till the level of output audio signal is above the threshold, the boost circuit starts to work before the audio stream arriving at amplifier power stage. The output voltage PVDD is dynamically adjusted to meet the requirement of output audio signal.

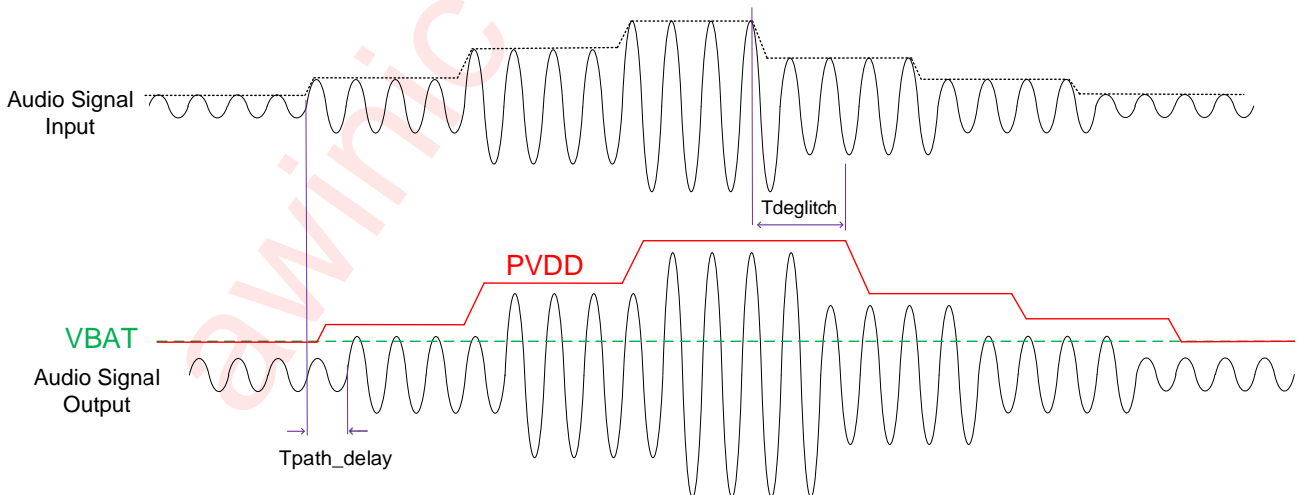


Figure 15 Boost Circuit Behavior in Smart Boost 2 Mode

PROTECTION MECHANISMS

Over Voltage Protection (OVP)

The boost circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the boost circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 150°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to PVDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when under voltage occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected under-voltage event has taken place.

BATTERY VOLTAGE MONITORING

The device monitors the voltage on the VBAT pin, which is most commonly the battery for the system. The battery voltage level is available via bits VBAT_DET in the Battery Supply Voltage register VBAT. Status bits VBAT_DET can be used to calculate the battery voltage. The battery voltage level V_{VBAT} is:

$$V_{VBAT} = \frac{VBAT_DET}{2^{10} - 1} \times 6.025V$$

For example, if VBAT_DET = 1001100011, the battery voltage level V_{VBAT} is equal to 3.6V.

PVDD VOLTAGE MONITORING

The device monitors the voltage on the PVDD pin, which is most commonly the PVDD voltage level for the system. The PVDD pin voltage level is available via bits PVDD_DET in the Power Supply Voltage monitor register PVDD. Status bits PVDD_DET can be used to calculate the PVDD voltage. The PVDD voltage level V_{PVDD} is:

$$V_{PVDD} = \frac{PVDD_DET}{2^{10} - 1} \times 12.05V$$

For example, if PVDD_DET = 1001100011, the PVDD voltage level V_{PVDD} is equal to 7.2V.

DIE TEMPERATURE MONITORING

The device monitors the die temperature and the result is available via bits TEMP_DET in the Temperature register TEMP. The TEMP_DET is a two's complement value. For example, if TEMP_DET = 00011001, the die temperature is 25°C.

CURRENT SENSING

The device provides speaker current sense for real time monitoring of loudspeaker behavior. The current sensing transfer function I_{SNS} is:

$$I_{SNS} = \frac{D_{OUT}}{2^{15} - 1} \times 3.3A$$

D_{OUT} : the current sense I²S output stream

AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP_NORM_V \times D_{in}$$

D_{in} : the level of input signal with a range from -1 to +1

AMP_NORM_V : the equivalent amplifier output voltage when D_{in} is 1. In receiver mode the AMP_NORM_V is 4.5V, in speaker mode it's 12V.

RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. If the receiver magnification is one times, the noise floor will be 11 μ V. Speaker and Receiver combo applications can be realized without changing any hardware.

When the device is set to receiver mode, the power supply of Class D driver stage is from VBAT directly without boost.

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

DEVICE ADDRESS

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

Table 4 Address Selection

AD	Address(7-bit)
Connect to GND	0x34
Connect to DVDD	0x35
Connect to SCL	0x36
Connect to SDA	0x37

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

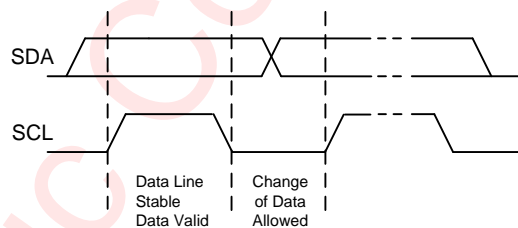
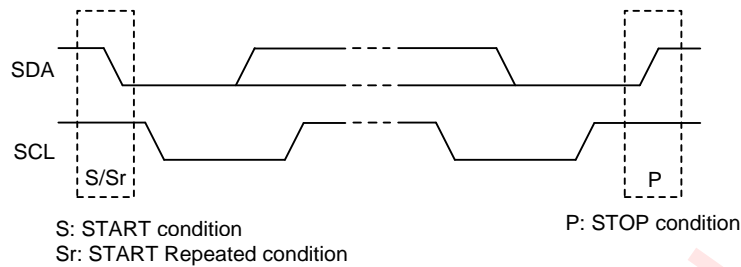


Figure 16 Data Validation Diagram

I²C START/STOP

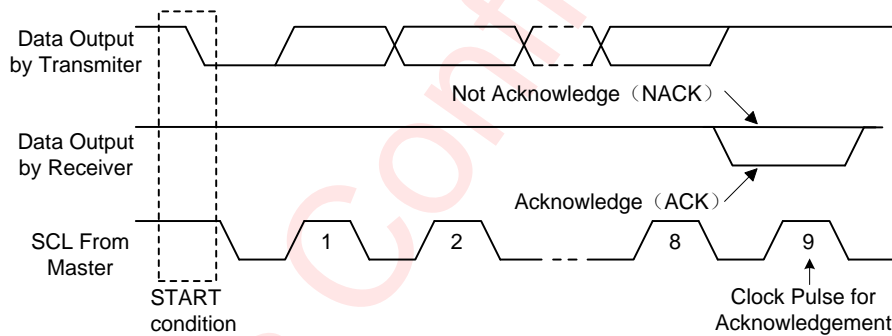
I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

Figure 17 I²C Start/Stop Condition Timing**ACK (ACKNOWLEDGEMENT)**

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

Figure 18 I²C ACK Timing**WRITE CYCLE**

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit)
- e) Slave sends acknowledge signal
- f) Master sends high data byte of 16-bit data to be written to the addressed register
- g) Slave sends acknowledge signal
- h) Master sends low data byte of 16-bit data to be written to the addressed register
- i) Slave sends acknowledge signal
- j) If master will send further 16-bit data bytes, the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)
- k) Master generates STOP condition to indicate write cycle end

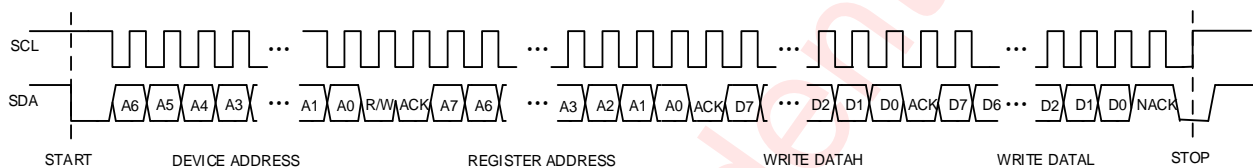


Figure 19 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

- a) Master device generates START condition
- b) Master device sends slave address (7-bit) and the data direction bit ($r/w = 0$).
- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit)
- e) Slave sends acknowledge signal
- f) Master generates STOP condition followed with START condition or REPEAT START condition
- g) Master device sends slave address (7-bit) and the data direction bit ($r/w = 1$).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends read high data byte of 16-bit data from addressed register.
- j) Master sends acknowledge signal.
- k) Slave sends read low data byte of 16-bit data from addressed register.
- l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.
- m) If the master device generates STOP condition, the read cycle is ended.

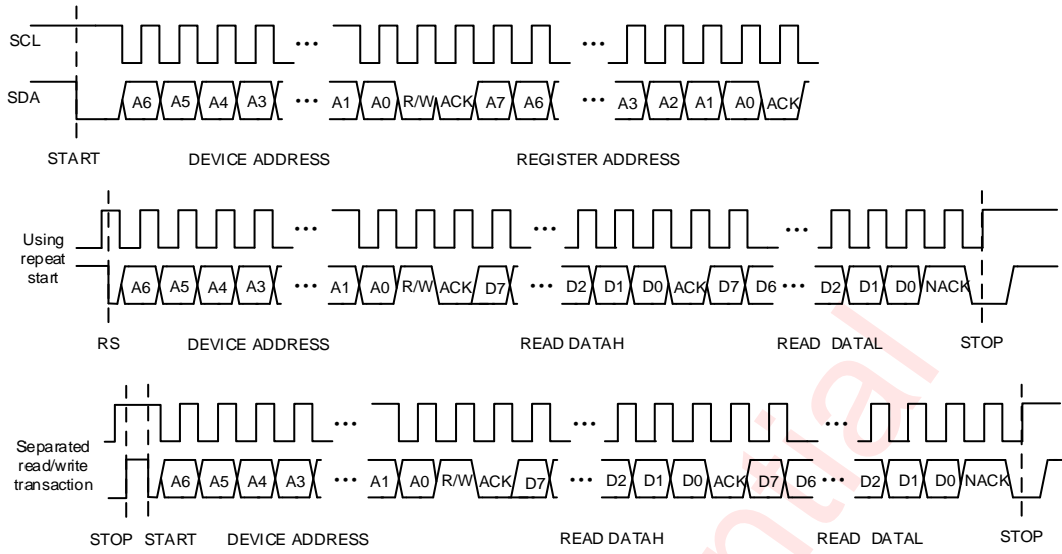


Figure 20 I²C Read Byte Cycle

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REGISTER MAP

REGISTER DESCRIPTION

REGISTER LIST

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
0x00	ID	RO	IDCODE																	
0x01	SYSST	RO	OVP2S	UVLS	ADPS		BSTOCS	OVPS	BSTS	SWS	CLIPS		NOCLKS	CLKS	OCDS	BOPS	OTHS	PLLS		
0x02	SYSINT	RC	OVP2I	UVLI	ADPI		BSTOCI	OVPI	BSTI	SWI	CLIP1		NOCLKI	CLKI	OCDI	BOPI	OTHI	PLLI		
0x03	SYSINTM	RW	OVP2M	UVLM	ADPM		BSTOCM	OVPM	BSTM	SWM	CLIPM		NOCLKM	CLKM	OCDM	BOPM	OTHM	PLLM		
0x04	SYSCTRL	RW		ULS_HMUTE			RMSE	HAGCE	HDCCE	HMUTE	EN_TRAN	I2SEN	WSINV	BCKINV	IPLL		AMPDP	PWDN		
0x05	SYSCTRL2	RW				ULS_MODE	INTMODE	INTN	VOL											
0x06	I2SCTRL1	RW		CFSEL			CHSEL		I2SMD		I2SFS		I2SBCK		I2SSR					
0x07	I2SCTRL2	RW		SLOT_NUM			I2S_TX_SLOTVLD			I2S_RXR_SLOTVLD			I2S_RXL_SLOTVLD							
0x08	I2SCTRL3	RW									FSYNC_TYPE	I2STXEN	DRVSTREN	I2SRXEN	IV2CH	I2SDOSEL	DOHZ	I2SCHS		
0x09	DACCFG1	RW	RVTH							AVTH										
0x0a	DACCFG2	RW	ATTH																	
0x0b	DACCFG3	RW	RTTH																	
0x0c	DACCFG4	RW	HOLDTH																	
0x20	DACST	RO	BSTVOUT_ST																	
0x21	VBAT	RO	VBAT_DET																	

ADDR	NAME	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	TEMP	RO									TEMP_DET							
0x23	PVDD	RO									PVDD_DET							
0x60	BSTCTRL1	RW			BST_RTH						BST_MODE		BST_ATH					
0x61	BSTCTRL2	RW	BST_IPEAK										VOUT_VREFSET					

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DETAILED REGISTER DESCRIPTION

ID: (Address 00h)				
Bit	Symbol	R/W	Description	Default
15:0	IDCODE	RO	Chip ID will be returned after read. All configuration registers will be reset to default Value after 0x55aa is written	0x2113

SYSST: (Address 01h)				
Bit	Symbol	R/W	Description	Default
15	OVP2S	RO	Boost OVP2 status indicator 0: Normal 1: OVP	0
14	UVLS	RO	VBAT under UVLO threshold Voltage indicator 0: Normal 1: UVLO	0
13	ADPS	RO	Boost Adaptive status. 0: Transparent 1: Boost	0
12	Reserved	-	Reserved	0
11	BSTOCS	RO	Boost over current indicator 0: Normal 1: Over Current	0
10	OVPS	RO	Boost OVP status indicator 0: Normal 1: OVP	0
9	BSTS	RO	Boost start up finished. 0: Not finished 1: Finished	0
8	SWS	RO	Amplifier switching status. 0: Not switching 1: Switching	0
7	CLIPS	RO	Amplifier clipping status. 0: Not clipping 1: Clipping	0
6	Reserved	-	Reserved	0
5	NOCLKS	RO	The reference clock of PLL is not available 0: Clock Ok 1: No Clock	0
4	CLKS	RO	Internal clocks status flag, status 0 means At least one clock are not stable 0: Not stable 1: Stable	0
3	OCDS	RO	Over current status in amplifier 0: Normal 1: OC	0

2	BOPS	RO	whether bop status is triggered or not 0: not triggered 1: triggered	0
1	OTHS	RO	Die Temperature is higher than 150°Cs 0: Normal 1: OT	0
0	PLLS	RO	PLL locked status. 0: Unlocked 1: Locked	0

SYSINT: (Address 02h)				
Bit	Symbol	R/W	Description	Default
15	OVP2I	RC	Interrupt indicator for OVP2S.	0
14	UVLI	RC	Interrupt indicator for Power On and UVLS	0
13	ADPI	RC	Interrupt indicator for ADPS	0
12	Reserved	-	Reserved	0
11	BSTOCI	RC	Interrupt indicator for BSTOCS.	0
10	OVPI	RC	Interrupt indicator for OVPS.	0
9	BSTI	RC	Interrupt indicator for BSTS.	0
8	SWI	RC	Interrupt indicator for SWS.	0
7	CLIP I	RC	Interrupt indicator for CLIPS.	0
6	Reserved	-	Reserved	0
5	NOCLKI	RC	Interrupt indicator for NOCLKS.	0
4	CLKI	RC	Interrupt indicator for CLKS.	0
3	OCDI	RC	Interrupt indicator for OCDS	0
2	BOPI	RC	Interrupt indicator for BOPS	0
1	OTHI	RC	Interrupt indicator for OTHS.	0
0	PLLI	RC	Interrupt indicator for PLLS.	0

SYSINTM: (Address 03h)				
Bit	Symbol	R/W	Description	Default
15	OVP2M	RW	Interrupt mask for OVP2I	1
14	UVLM	RW	Interrupt mask for UVLI.	1
13	ADPM	RW	Interrupt mask for ADPI	1
12	Reserved	RW	Reserved	1
11	BSTOCM	RW	Interrupt mask for BSTOCI.	1
10	OVPM	RW	Interrupt mask for OVPI	1
9	BSTM	RW	Interrupt mask for BSTI.	1
8	SWM	RW	Interrupt indicator for SWI.	1
7	CLIPM	RW	Interrupt indicator for CLIP I.	1
6	Reserved	RW	Reserved	1
5	NOCLKM	RW	Interrupt mask for NOCLKI.	1
4	CLKM	RW	Interrupt mask for CLKI.	1
3	OCDM	RW	Interrupt mask for OCDI.	1
2	BOPM	RW	Interrupt mask for BOPS.	1
1	OTHM	RW	Interrupt mask for OTHI.	1
0	PLLM	RW	Interrupt mask for PLLI.	1

SYSCTRL: (Address 04h)				
Bit	Symbol	R/W	Description	Default

15	Reserved	RW	Not used	0
14	ULS_HMUTE	RW	Only when HMUTE&ULS_HMUTE=1, ultrasound can be muted 0:disable 1:enable	0
13:12	Reserved	RW	Not used	3
11	RMSE	RW	Hardware HAGC mode selection 0: Peak AGC 1: RMS AGC	0
10	HAGCE	RW	Disable/Enable Hardware AGC 0: disable 1: enable	0
9	HDCCE	RW	Disable/Enable Hardware DC Canceling module 0: disable 1: enable	1
8	HMUTE	RW	Disable/Enable Hardware mute module 0: disable 1: enable	1
7	EN_TRAN	RW	Transparent mode for ClassD, OC threshold will decrease when it is active at Receiver mode 0: SPK 1: RCV	0
6	I2SEN	RW	Disable/Enable whole I ² S interface module 0: disable 1: enable	1
5	WSINV	RW	I ² S Left/Right channel switch control 0: Not switch 1: Switch	0
4	BCKINV	RW	I ² S bit clock invert control 0: Not invert 1: Inverted	0
3	IPLL	RW	PLL reference clock selection 0: BCK 1: WCK	0
2	Reserved	RW	Not used	0
1	AMPPD	RW	Amplifier power down control bit, Power Down until system configuration finished 0: Working 1: Power Down	1
0	PWDN	RW	System power down control bit 0: Working 1: Power Down	1

SYSCTRL2: (Address 05h)				
Bit	Symbol	R/W	Description	Default
15:13	Reserved	RW	Not used	0
12	ULS_MODE	RW	Ultrasonic mode control 0: Legacy 1: TDM	0
11	INTMODE	RW	Interrupt pad INTN output mode selection 0: Open-drain 1: Push Pull	0

10	INTN	RW	Interrupt pad INTN pin-source selection 0: SYSINT 1: SYSST	0
9:0	VOL	RW	Volume control, from 0 to -95.875dB [5:0] : in unit of -0.125dB [9:6] : in unit of -6dB	0

I2SCTRL1: (Address 06h)				
Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0
14:12	CFSEL	RW	I ² S legacy path output data selection 000: HAGC 001: Reserved 010: IVBT 011: IV Sense Others: Reserved	0
11:10	CHSEL	RW	Left/right channel selection for I ² S input 00: Reserved 01: Left 10: Right 11: Mono	1
9:8	I2SMD	RW	I ² S interface mode selection 00: Philip Standard 01: MSB justified 10: LSB justified 11: Reserved	0
7:6	I2SFS	RW	I ² S data resolution selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits	3
5:4	I2SBCK	RW	I ² S BCK mode 00: 32*fs 01: 48*fs 10: 64*fs 11: Reserved	2
3:0	I2SSR	RW	I ² S interface sample rate configuration 0000: 8 KHz 0001: 11 KHz 0010: 12 KHz 0011: 16 KHz 0100: 22 KHz 0101: 24 KHz 0110: 32 KHz 0111: 44 KHz 1000: 48 KHz 1001: 96 KHz Others: Reserved	8

I2SCTRL2: (Address 07h)				
Bit	Symbol	R/W	Description	Default
15	Reserved	RW	Not used	0

14:12	SLOT_NUM	RW	I ² S TDM mode control (support max to 8 slots). 000: I ² S mode 001: TDM1s 010: TDM2s 011: TDM4s 100: TDM6s 101: TDM8s 110: Reserved	0
11:8	I2S_TX_SLOTVLD	RW	TX slot selection, data will be sent to one of the flowing slots. 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 0111: Slot 7 Others: Reserved	0
7:4	I2S_RXR_SLOTVLD	RW	RX right channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 0111: Slot 7 Others: Reserved	1
3:0	I2S_RXL_SLOTVLD	RW	RX left channel slot selection 0000: Slot 0 0001: Slot 1 0010: Slot 2 0011: Slot 3 0100: Slot 4 0101: Slot 5 0110: Slot 6 0111: Slot 7 Others: Reserved	0

I2SCTRL3: (Address 08h)				
Bit	Symbol	R/W	Description	Default
15:8	Reserved	RW	Not used	0
7	FSYNC_TYPE	RW	Audio Frame synchronization signal (WCK) pulse width configuration 0: One-slot 1: One-bck	0
6	I2STXEN	RW	Disable/Enable I ² S transmitter module 0: disable 1: enable	1
5	DRVSTREN	RW	I2S_DATAO PAD driving strength setting 0: 4mA 1: 12mA	1

4	I2SRXEN	RW	Disable/Enable I ² S receiver module 0: disable 1: enable	1
3	IV2CH	RW	I ² S TX channel data packing mode control. When I2SBCK is set to 32*fs mode, Current & Voltage data could be transmitted to I ² S Left & Right channels by using Special Mode. 0: Legacy 1: Special	0
2	I2SDOSEL	RW	I ² S unused channels output data selection 0: Zeros 1: TX Data	1
1	DOHZ	RW	Unused channel Data control, When it is set to 0, all Channels are available with same data. Otherwise Unused channel is set to be Hi-Z. 0: All 1: Hi-Z	1
0	I2SCHS	RW	I ² S TX Channel selection 0: Left 1: Right	0

DACCFG1: (Address 09h)				
Bit	Symbol	R/W	Description	Default
15:8	RVTH	RW	Release Amplitude threshold, in percent of signal full scale	0x39
7:0	AVTH	RW	Attack Amplitude threshold, in percent of signal full scale RMSE = 0 (Peak AGC) : $P0 = ((i/256 * Gain)^2) / R_{Load} / 2$ RMSE = 1 (RMS AGC) : $P0 = (i/256) * (Gain^2) / R_{Load}$ i is the register Value, default 0x40 Gain is the Amplifier Gain configured by SYSCTRL.SPK_GAIN, default 12 R_{Load} is 8Ω/6Ω for different application, default 8 Ω	0x40

DACCFG2: (Address 0ah)				
Bit	Symbol	R/W	Description	Default
15:0	ATTH	RW	Attack time threshold in unit of 20.8μs 0: Reserved n: n*20.8us	0x0030

DACCFG3: (Address 0bh)				
Bit	Symbol	R/W	Description	Default
15:0	RTTH	RW	Release time threshold in unit of 20.8μs 0: Reserved n: n*20.8μs	0x01E0

DACCFG4: (Address 0ch)				
Bit	Symbol	R/W	Description	Default
15:8	Reserved	RW	Not used	0
7:0	HOLDTH	RW	Hold time before release control, in unit of about 1.33ms 0: Reserved n: n*1.33ms	0x64

DACST: (Address 20h)				
Bit	Symbol	R/W	Description	Default
15:7	Reserved	RO	Not used	0
6:0	BSTVOUT_ST	RO	BOOST max output Voltage control bits (62.5mV/Step) 0000000~00101111: reserved 0011000: 5V 1101100: 10.25V others: reserved	0

VBAT: (Address 21h)				
Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	VBAT_DET	RO	Detected Voltage of battery, and the full range is 6.025V $V_BATS=(VBAT)/1023 \times 6.025$	0x263

TEMP: (Address 22h)				
Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	TEMP_DET	RO	Detected Die Temperature (Two's Complement), typical Values are as follows. 0x3D8 : -40 °C 0x00 : 0 °C 0x01 : 1 °C 0x19 : 25 °C 0x37 : 55 °C Please convert it to decimal number.	0x019

PVDD: (Address 23h)				
Bit	Symbol	R/W	Description	Default
15:10	Reserved	RO	Not used	0
9:0	PVDD_DET	RO	Detected Voltage of PVDD, and the full range is 12.05V $PVDD=(PVDD_DET)/1023 \times 12.05$	0x263

BSTCTRL1: (Address 60h)				
Bit	Symbol	R/W	Description	Default
15:14	Reserved	RW	Not used	0
13:8	BST_RTH	RW	Smart boost release threshold setting, When signal is below the threshold, the Voltage of VBST will not be raised up higher than VBAT in smart boost mode Release threshold = BST_RTH * 1/64 Full-scale	4
7:6	BST_MODE	RW	BOOST mode selection, Initialize to 6 . 000: Transparent 001: Force Boost 010: Smart Boost1 011: Smart Boost2 Others: Reserved	0x3

5:0	BST_ATH	RW	Smart boost attack threshold setting. When signal is above over the threshold, the Voltage of VBST will be raised up higher than VBAT in smart boost mode Attack threshold = BST_ATH * 1/64 Full-scale	2
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BSTCTRL2: (Address 61h)				
Bit	Symbol	R/W	Description	Default
15:12	BST_IPEAK	RW	Boost peak current limiter threshold 0000:1.75A 0001:2.0A 0010:2.25A 0011:2.5A 0100:2.75A 0101:3.0A 0110:3.25A 0111:3.5A 1000:3.75A 1001:4A 1010:4.25A Others: Reserved	9
11:8	BST_TDEG	RW	Smart Boost small signal level detection deglitch time 0000: 0.50 ms 0001: 1.00 ms 0010: 2.00 ms 0011: 4.00 ms 0100: 8.00 ms 0101: 10.7 ms 0110: 13.3 ms 0111: 16.0 ms 1000: 18.6 ms 1001: 21.3 ms 1010: 24.0 ms 1011: 32.0 ms 1100: 64.0 ms 1101: 128 ms 1110: 256 ms 1111: 1024ms	11
7	Reserved	RW	Not used	0
6:0	VOUT_VREFSET	RW	BOOST max output Voltage control bits (62.5mV/Step) 0000000~0010111: reserved 0011000: 5V 1101100: 10.25V others: reserved	0x58

APPLICATION INFORMATION

EXTERNAL COMPONENTS

BOOST INDUCTOR SELECTION

Inductance value is limited by the boost converter's internal loop compensation, a large L_{SW} will reduce the phase margin of the DC-to-DC converter. Also, the inductor should have low core loss at 1MHz (Min.) and low DCR for better efficiency under all operating conditions, the recommended value of inductor is 1 μ H.

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, inductance value will decline since the magnetic core begins to saturate; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. The inductor saturation current rating could to be considered with the following equation:

$$I_{L_PEAK} = \frac{2 * P_{OUT}}{\eta * V_{BAT}} + \frac{V_{BAT} * (PVDD - V_{BAT})}{2 * L_{SW} * F_{BST} * PVDD}$$

Following is the inductor selection reference for typical speaker impedances.

V_{VBAT} (V)	PVDD (V)	R_L (Ω)	Efficiency (%)	P_{OUT} (W)	I_{L_PEAK} (A)	I_{SAT_min} (A)
4.2	10.25	8	75	5.2	4.08	4.2
4.2	10.25	6	73	5.4	4.23	4.5

BOOST CAPACITOR SELECTION

Boost output capacitor is usually within the range 0.1 μ F~47 μ F. The ceramic capacitors with low ESR are recommended for low ripple voltage which is determined as following equation:

$$\Delta PVDD = \frac{(PVDD - V_{BAT}) * I_{OUT}}{\eta * PVDD * F_{BST} * C_{OUT}} + \left(\frac{I_{OUT} * PVDD}{V_{BAT}} + \frac{V_{BAT} * (PVDD - V_{BAT})}{2 * L_{SW} * F_{BST} * PVDD} \right) * R_{C_ESR}$$

Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the material, size, capacitor voltage, and capacitance values. It is suggested to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically BaTiO₃), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance.

Please notice the DC bias characteristics when selecting capacitors. For typical applications, it is necessary to ensure that the residual capacitance is higher than **3.3 μ F**. Take the following capacitances as the output capacitor of boost for example:

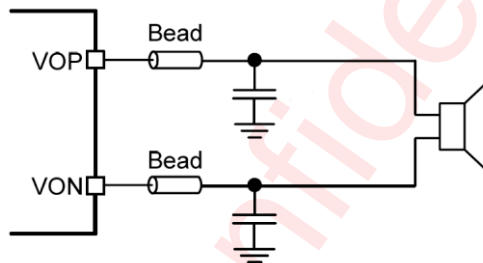
Value	Material	Size (mm ³)	Rated Voltage	Quantity	Value@10.25V
10 μ F	X5R	1.00x0.50x0.50 (0603)	25V	2	3.6 μ F
22 μ F	X5R	2.00x0.80x0.85 (0805)	25V	1	3.7 μ F

SUPPLY DECOUPLING CAPACITOR

The device is a high-performance audio amplifier that requires adequate power supply decoupling. A $1\mu\text{F}$ low equivalent-series-resistance (ESR) ceramic capacitor is recommended. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the device is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the $1\mu\text{F}$ ceramic capacitor, place a $10\mu\text{F}$ capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

FILTER FREE OPERATION AND FERRITE BEAD FILTERS

If the PA is close to the EMI sensitive circuits and/or there are long leads from amplifier to speaker, a ferrite bead filter could be used, and placed as close as possible to the output pins of the PA. When choosing a ferrite bead, select a ferrite bead with adequate current rating to prevent distortion of the output signal. In addition, a 0.1nF ceramic capacitor is typically recommended, and its rated voltage should be above 25V .



LAYOUT CONSIDERATION

In order to obtain excellent performance of the PA, the below PCB layout guidelines should be followed:

All the filter capacitors should be placed close to the corresponding pins of the PA, including VBST, VBAT, DVDD.

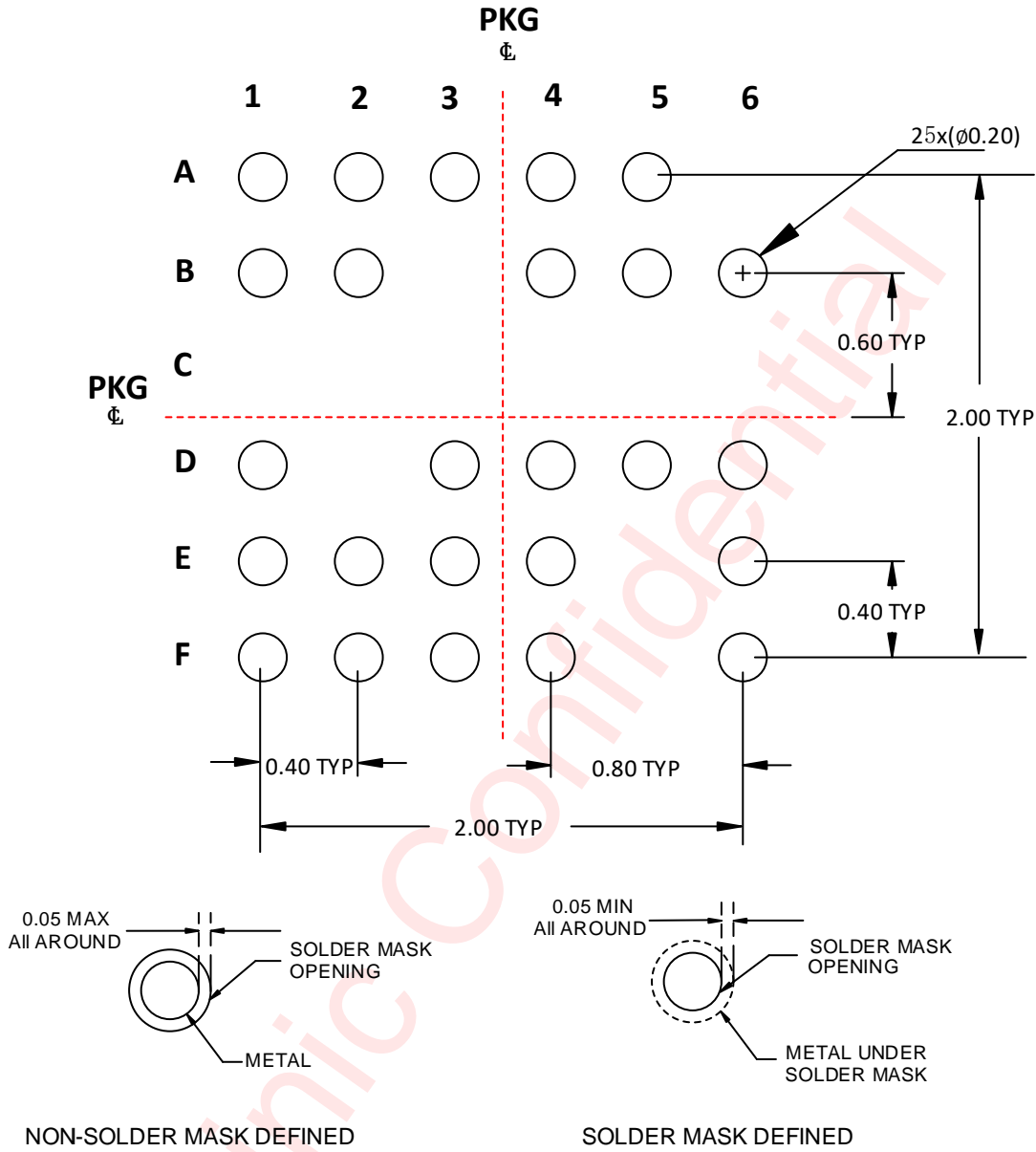
The traces of SW pin should support currents up to the device over-current limit (peak current 4A), and the input line from the battery to the SW pin should be traced above 4A current drive.

For the case of speaker impedance equal to 8Ω , try to provide a separate, short and thick power line to the PA, the copper width is recommended to be larger than 4mm .

The beads and capacitor should be placed close to the VON and VOP pin. The output line from PA to speaker should be as short and thick as possible. The width is recommended to be larger than 1.2mm .

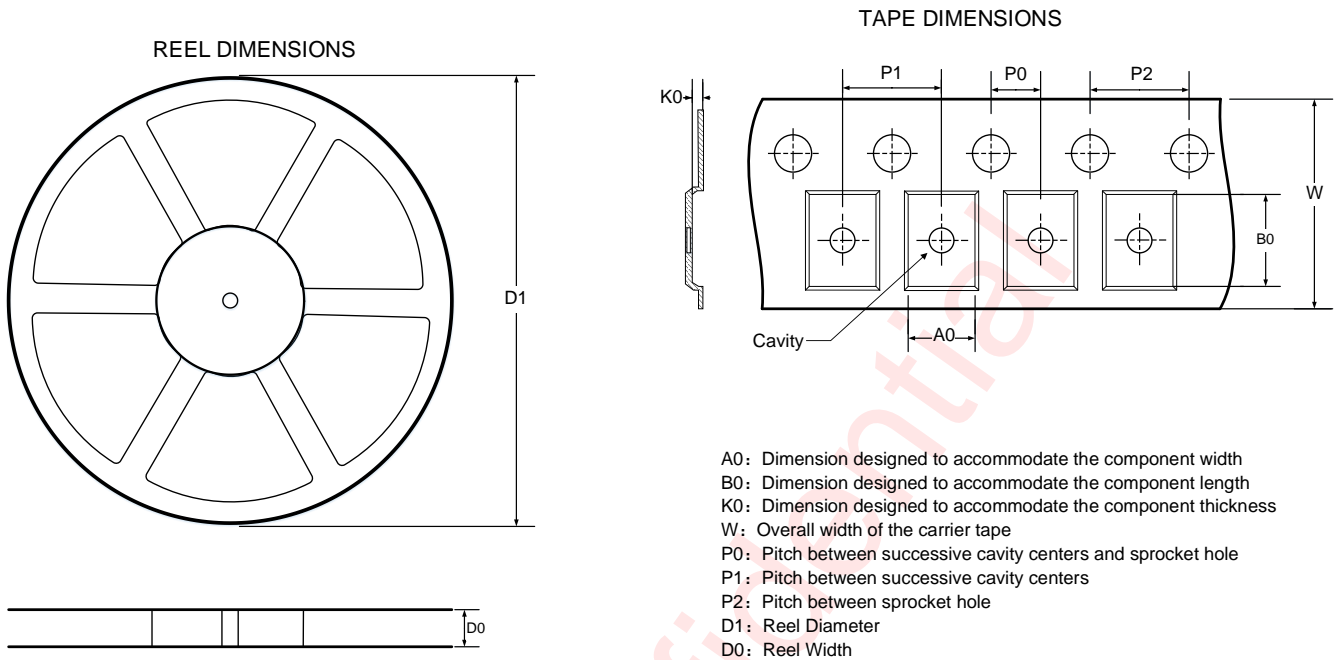
The via numbers determine the current capability. Typically, the boost converter trace need four via to handle the current requirement around 4A .

LAND PATTERN DATA

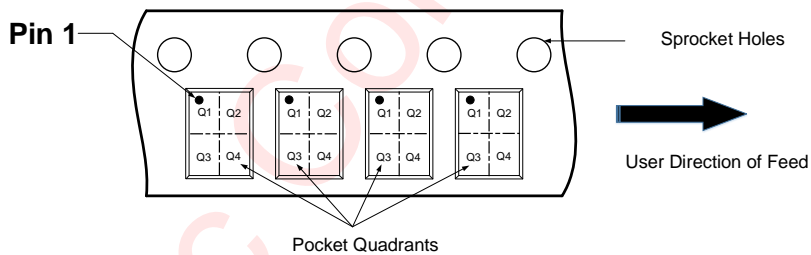


Unit: mm

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.00	8.40	2.70	2.70	0.75	2	4	4	8	Q1

All dimensions are nominal

REVISION HISTORY

Version	Date	Change Record
V1.0	Sept. 2021	Officially Released
V1.1	Feb. 2022	Update Figure 6 & update register reserved default
V1.2	Oct. 2022	Smart BOOST with total efficiency up to 83% VOLUME CONTROL : The volume control function attenuates the audio signal at the end of digital audio processing . The range of volume setting is from 0db to -95.875db with 0.125db/step

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