钍地半导体
Tudi Semiconductor

Product Specification

TUDI-SN6BC174A/SN75LBC174A

Quad RS-485 differential line driver

网址 www.sztdbdt.com

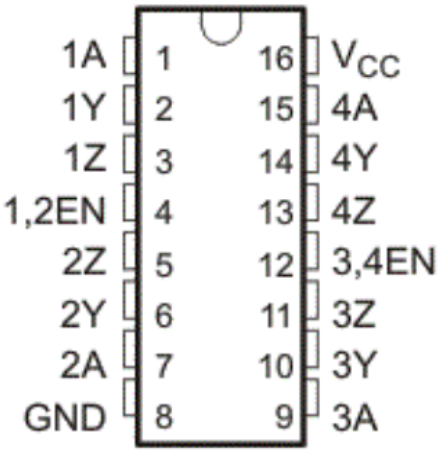
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Designed specifically for TIA/EIA-485, TIA/EIA-422, and ISO 8482 applications
- Signal transmission rate 1 up to 30Mbps
- Propagation delay time < 11ns
- Low standby power consumption - max 1.5mA
- Output ESD protection: 12kV
- Driver positive/negative current limiting
- Glitch-free power-up and power-down operation, suitable for line insertion applications
- Thermal shutdown protection
- Industry-standard pinout, compatible with SN75174, MC3487, DS96174, LTC487, and MAX3042



(TOP VIEW)

Applications

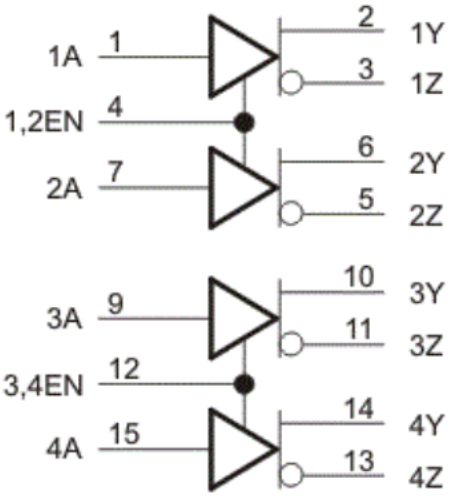
- Motor drives
- Factory automation and control

Description

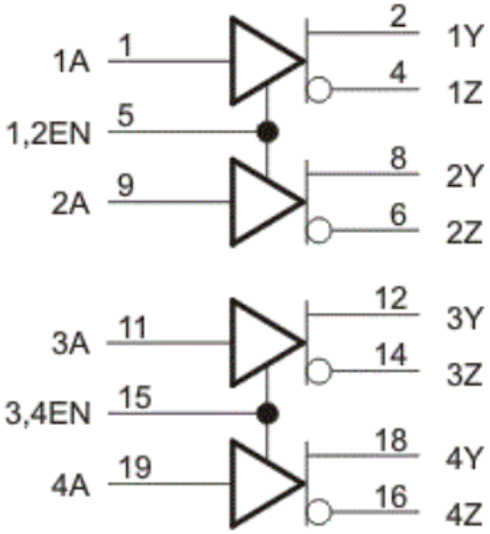
SN65LBC174A and SN75LBC174A are four-channel differential line drivers with three-state outputs, specifically designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

These devices are optimized to achieve balanced multi-point bus transmission at signal transmission rates up to 30 Mbit/s. The transmission medium can be printed circuit board traces, backplanes, or cables. The final data transmission rate and distance depend on the attenuation characteristics of the medium and environmental noise coupling.

Each driver features current limiting and thermal shutdown circuitry, making it suitable for high-speed multi-point data transmission applications in noisy environments. These devices are using LinBiCMOS®, which helps achieve low power consumption and robustness.
The two enable (EN) inputs provide two enable terminals for the drivers, or can be externally integrated to control for all four drivers with a single signal. When disabled or powered down, the driver outputs provide a high impedance to the bus, thereby reducing the system load.
The SN75BC174A operates in a temperature range of 0°C to 70°C. The SN65LBC174A operates in a temperature range of40°C to 85°C.



逻辑图（正逻辑）



逻辑图（正逻辑）

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE / UNIT
Supply voltage range, V_{CC} (2)			- 0.3 V to 6 V
Voltage range at any bus (DC)			- 10 V to 15 V
Voltage range at any bus (transient pulse through 100 Ω, see 图 6-8)			- 30 V to 30 V
Input voltage range at any A or EN terminal, V_I			- 0.5 V to V_{CC} + 0.5 V
Electrostatic discharge	Human body model (3)	Y, Z, and GND	±12 kV
		All pins	±5 kV
	Charged-device model (4)	All pins	±1 kV
Storage temperature range, T_{stg}			- 65°C to 150°C
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Tested in accordance with JEDEC standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC standard 22, Test Method C101.

5.2 Dissipation Rating Table

表 5-1. Dissipation Rating Table

PACKAGE(1)	JEDEC BOARD MODEL	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR (2) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
16 DW	LOW K	1200 mW	9.6 mW/°C	769 mW	625 mW
	HIGH K	2240 mW	17.9 mW/°C	1434 mW	1165 mW
20 DW	LOW K	1483 mW	11.86 mW/°C	949 mW	771 mW
	HIGH K	2753 mW	22 mW/°C	1762 mW	1432 mW
16 N	LOW K	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	Y, Z	- 7		12	V
High-level input voltage, V_{IH}	A, EN	2		V_{CC}	V
Low-level input voltage, V_{IL}	A, EN	0		0.8	V
Output current		- 60		60	mA
Operating free-air temperature, T_A	SN75LBC174A	0		70	°C
	SN65LBC174A	- 40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75ALS174A			UNIT
		N (PDIP)	DW (SOIC)	DW	
		16 PINS	16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	71.1	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	37.4	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	36.8	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	13.3	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	36.4	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7 Device Functional Modes

表 7-1. Function table (each driver)

INPUT(1)	ENABLE	OUTPUT	OUTPUT
A	EN	Y	Z
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

5.5 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA		- 1.5	- 0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude(2)	No load (open circuit)		3		V_{CC}	V
		R_L = 54Ω, See 图 6-1		1	1.6	2.5	
		With common-mode loading, See 图 6-2		1	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See 图 6-1		- 0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 6-3		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See 图 6-3		- 0.02		0.02	V
I_I	Input current	A, EN		- 50		50	μA
I_{OS}	Short-circuit output current	V_{TEST} = -7V to 12V, See 图 6-7	V_I = 0V	- 200		200	mA
			V_I = V_{CC}				
I_{OZ}	High-impedance-state output current		EN at 0V	- 50		50	μA
$I_{O(OFF)}$	Output current with power off		V_{CC} = 0V	- 10		10	
I_{CC}	Supply current	V_I = 0V or V_{CC}, No load	All drivers enabled			23	mA
			All drivers disabled			1.5	
C_{IN}	Input Capacitance	A inputs			13		pF
		EN inputs			21		pF

(1) All typical values are at V_{CC} = 5V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

5.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 54Ω, C_L = 50pF, See 图 6-4	5.5	8	11	ns
t_{PHL}	Propagation delay time, high-to-low level output		5.5	8	11	ns
t_r	Differential output voltage rise time		2	7.5	11	ns
t_f	Differential output voltage fall time		2	7.5	11	ns
$t_{sk(p)}$	Pulse skew $\|t_{PLH} - t_{PHL}\|$			0.6	2	ns
				0.6	2	
$t_{sk(o)}$	Output skew(1)				2	ns
$t_{sk(pp)}$	Part-to-part skew(2)				3	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See 图 6-5			25	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance				25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See 图 6-6			30	ns
t_{PLZ}	Propagation delay time, low-level-output-to-high impedance				20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

6 Parameter Measure Information

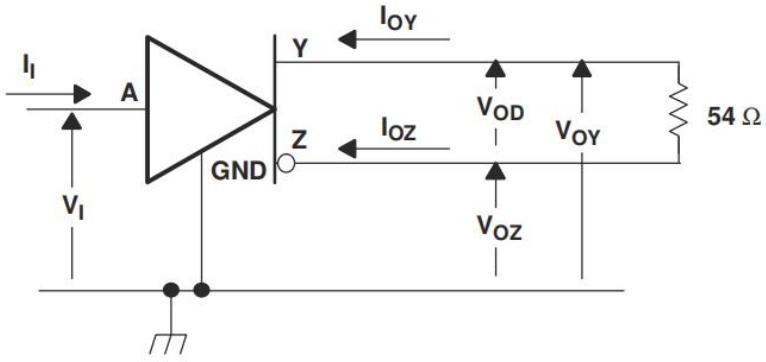


图 6-1. Test Circuit, V_{OD} Without Common-Mode Loading

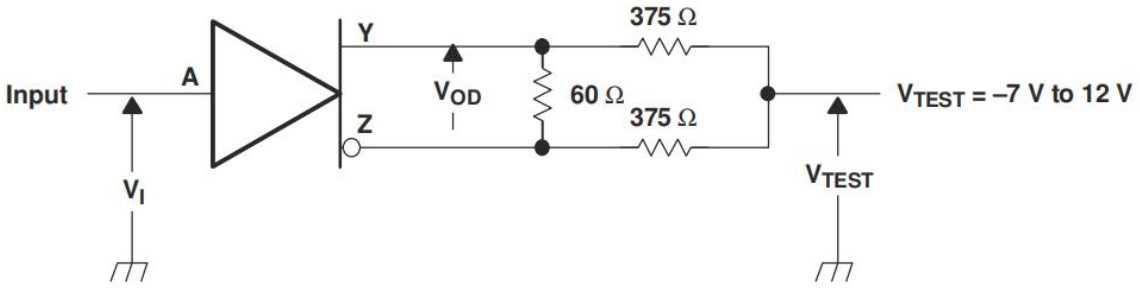
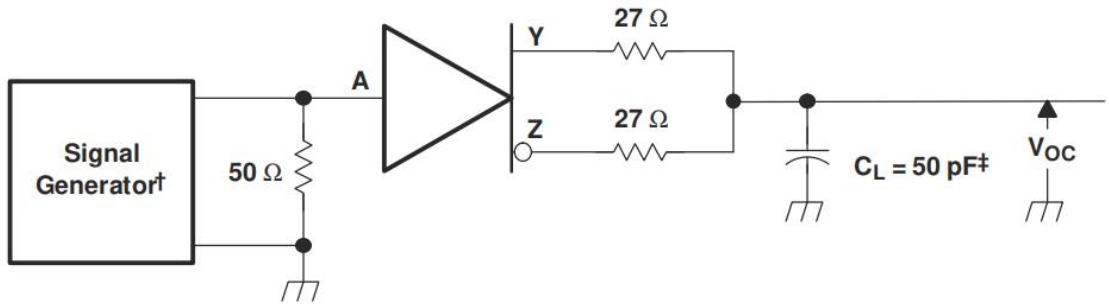
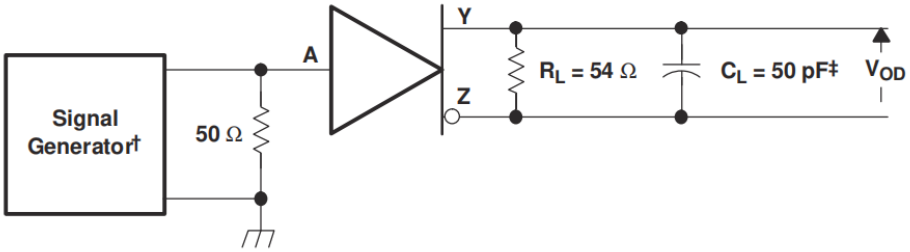


图 6-2. Test Circuit, V_{OD} With Common-Mode Loading



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

图 6-3. V_{OC} Test Circuit



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

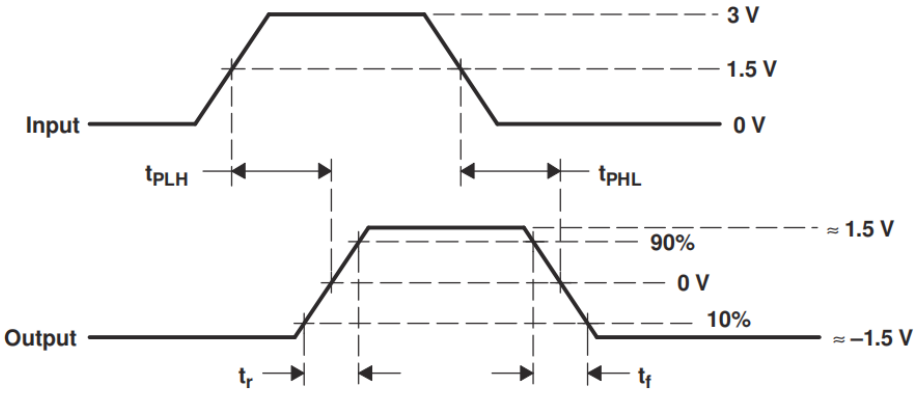
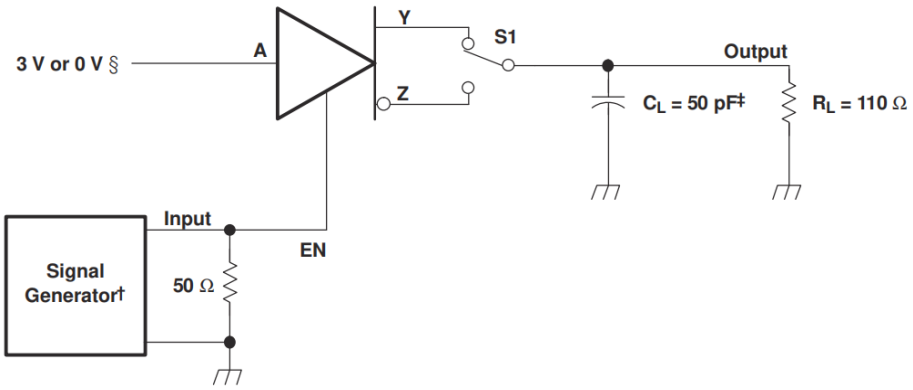


图 6-4. Output Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3 V if testing Y output, 0 V if testing Z output

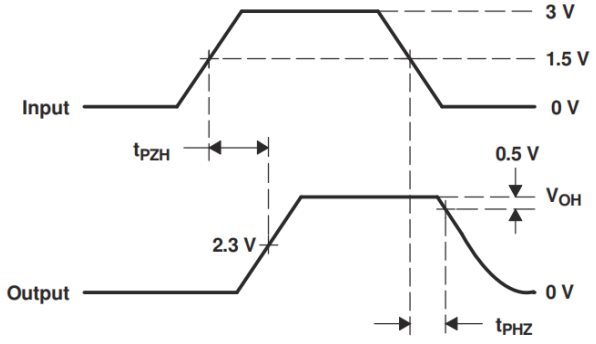
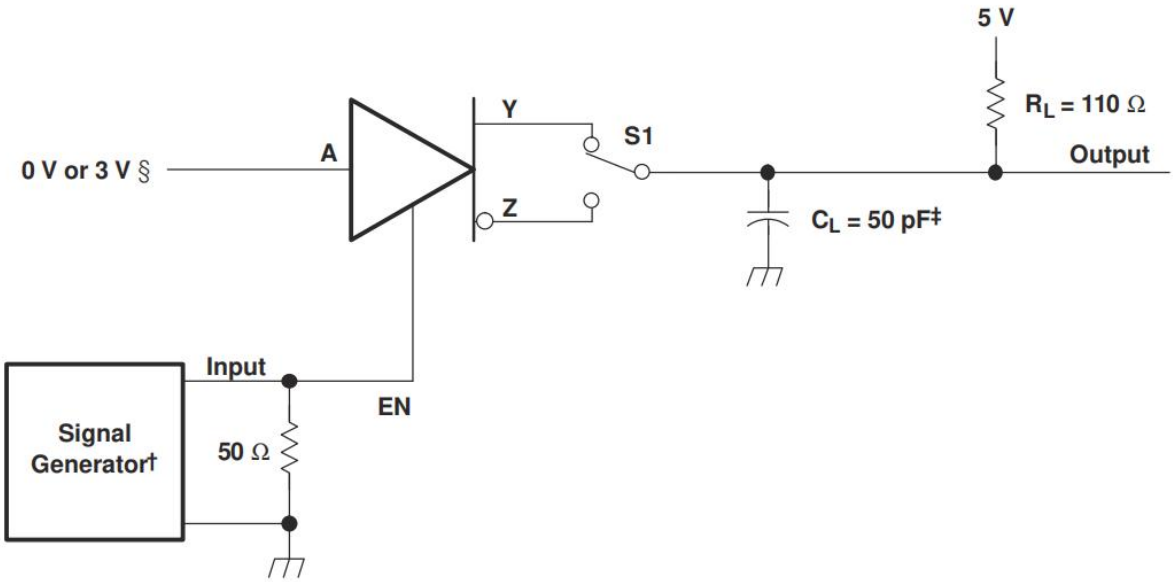


图 6-5. Enable Timing Test Circuit and Waveforms, t_{PZH} and t_{PHZ}



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3 V if testing Y output, 0 V if testing Z output

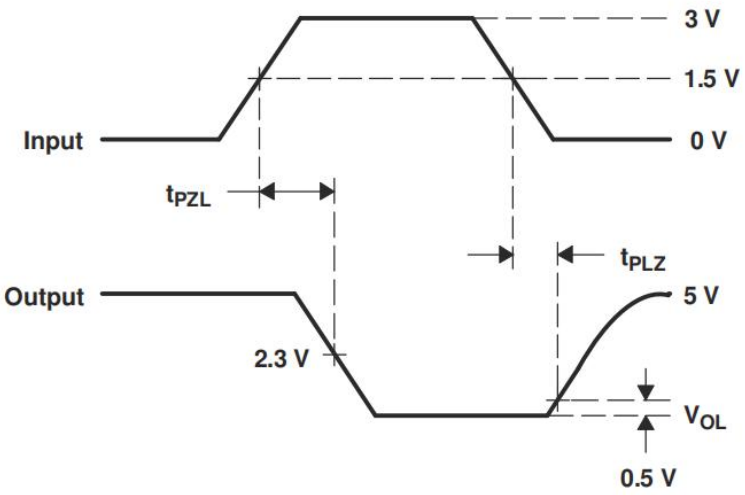


图 6-6. Enable Timing Test Circuit and Waveforms, t_{PZL} and t_{PLZ}

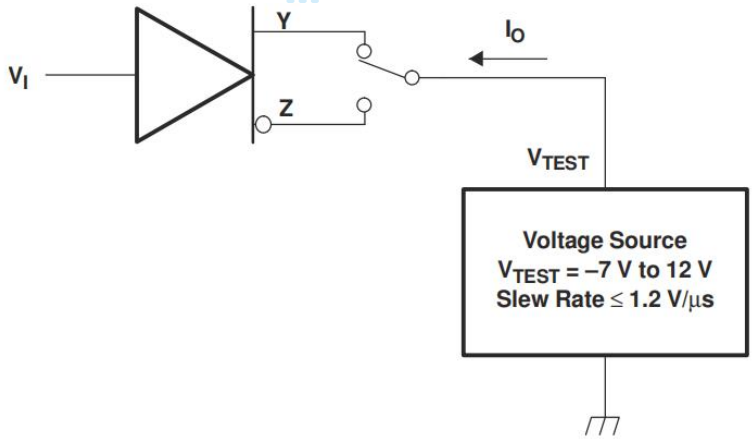


图 6-7. Test Circuit, Short-Circuit Output Current

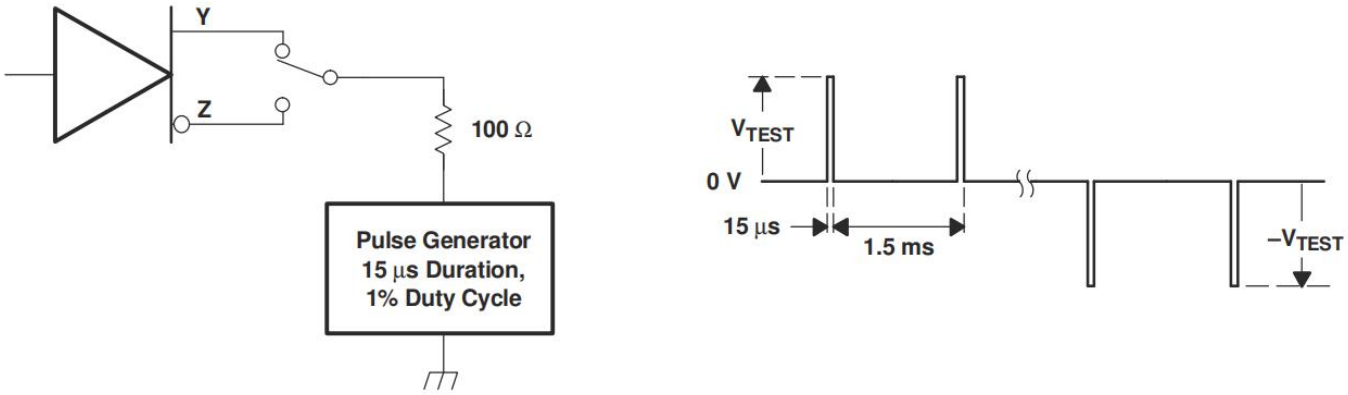


图 6-8. Test Circuit Waveform, Transient Overvoltage Test

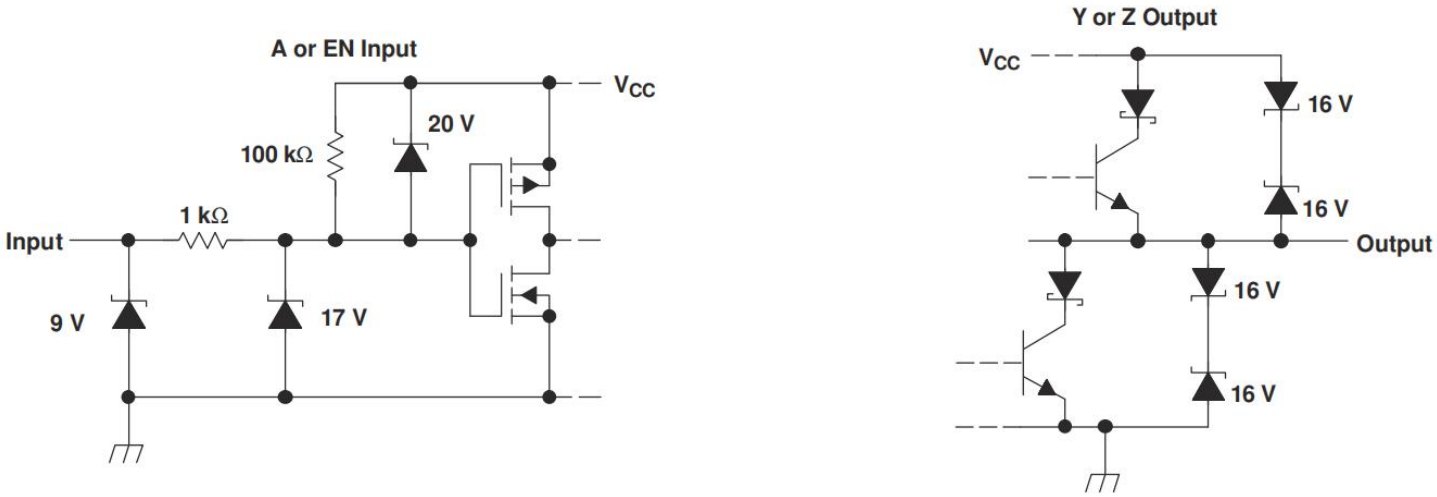
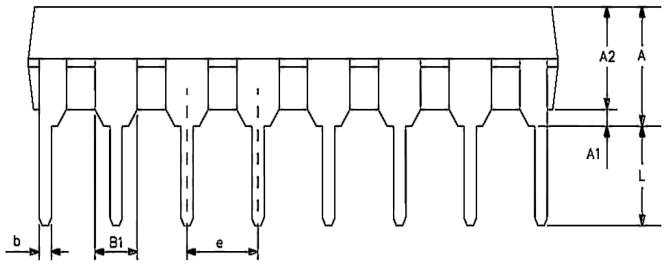


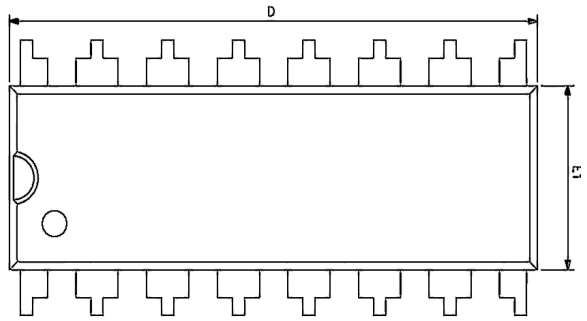
图 6-9. Equivalent Input and Output Schematic Diagrams

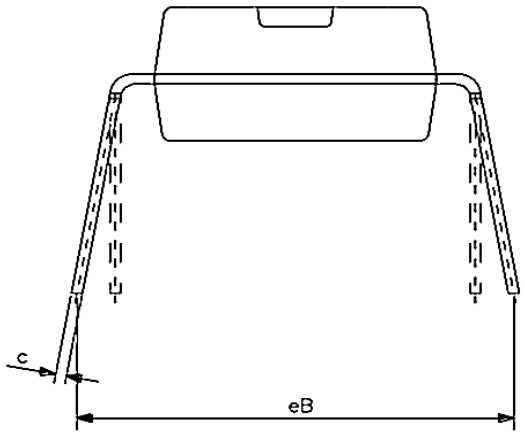
Order information

Order Number	Package	Package Quantity	Marking On The park
SN65LBC174AN-TUDI	DIP16	Tube,25,A box of 1000	SN65LBC174AN
SN65LBC174N-TUDI	DIP16	Tube,25,A box of 1000	SN65LBC174N
SN65LBC174AN-TUDI	DIP16	Tube,25,A box of 1000	SN65LBC174AN
SN65LBC174N-TUDI	DIP16	Tube,25,A box of 1000	SN65LBC174N

Package DIP16







SIZE / SYMBOL	MIN./mm	MAX./mm
A2	3.20	3.60
A1	0.51	___
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
C	0.20	0.36
eB	7.62	9.30
R	0.20TYP	
R1	0.30TYP	
θ	0°	8°
θ1	45°TYP	
02	12°TYP	
03	0°	8°
04	0°	10°

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