Low-Power, Programmable-Delay Supervisory Circuits

Features

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s
- Very Low Quiescent Current: 2.4μA (Typical)
- High Threshold Accuracy: 2.5% (Typical)
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.405V Are Available
- Manual Reset (MRB) Input
- Open-Drain RESETN Output
- -40°C to 125°C Operating Temperature Range
- Package
- SOT23-6L

Device comparison

AWS703808YYY Z AAA

Package type
STR:SOT23-6L

Reset time delay
C: 1.25ms to 10s for config the CT pin

Reset threshold
F09:0.84V
F12:1.12V
F125:1.16V
F15:1.40V
F18:1.67V
F19:1.77V
F25:2.33V
F30:2.79V
F33:3.07V
F50:4.65V
ADJ:0.4V to 5V

General Description

The AWS703808 family of microprocessor supervisory circuits monitors system voltages from 0.405V to 5V, asserting an open-drain RESETN signal when the SENSE voltage drops below a preset threshold or when the manual reset (MRB) pin drops to a logic low. The RESETN output remains low for the user-adjustable delay time after the SENSE voltage and manual reset (MRB) return above the respective thresholds. The AWS703808 device uses a precision reference to achieve 2.5% threshold accuracy for $V_{IT} \leq 3.3V$. The reset delay time can be set to 20ms by disconnecting the CT pin, 300ms by connecting the CT pin to VDD using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the CT pin to an external capacitor. The AWS703808 device has a very low typical quiescent current of 2.4μA, so it is well-suited to battery-powered applications. It is fully specified over a temperature range of -40°C to 125°C T_A.

Applications

- DSP or Microcontroller Applications
- Notebook and Desktop Computers
- PDAs and Hand-Held Products
- Portable and Battery-Powered Products
- FPGA and ASIC Applications

Application Circuit

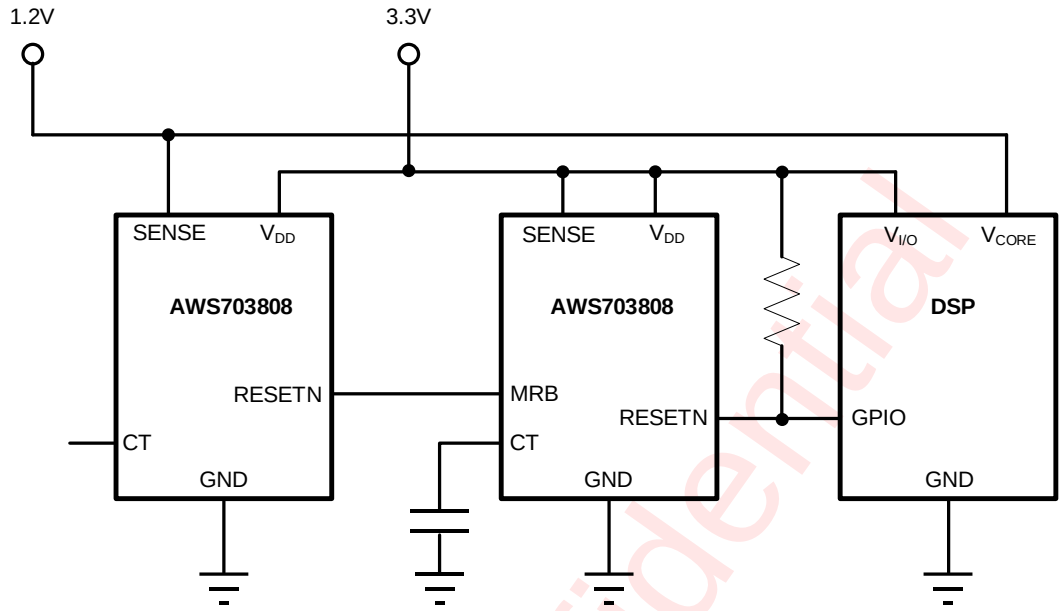
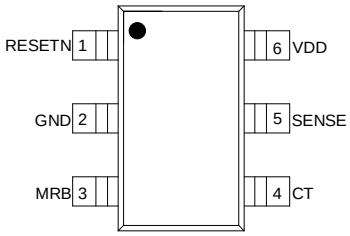


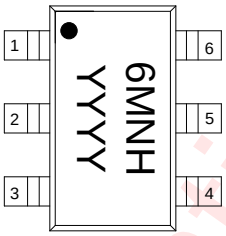
Figure 1 Typical Application Circuit of AWS703808

Pin Configuration and Top Mark

AWS703808ADJCSTR
（Top View）



AWS703808ADJCSTR
Marking
（Top View）



6MNH-AWS703808ADJCSTR
YYYY-Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	Pin Name	Description
1	RESETN	RESETN is an open drain output that is driven to a low-impedance state when RESETN is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the MRB pin is set to a logic low). RESETN remains low (asserted) for the reset period after both SENSE is above V_{IT} and MRB is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, and allows the reset pin to attain voltages higher than VDD.
2	GND	Ground.
3	MRB	Driving the manual reset pin (MRB) low asserts RESETN. MRB is internally tied to VDD by a 90kΩ pull-up resistor.
4	CT	Reset period programming pin. Connecting this pin to VDD through a 40kΩ to 200kΩ resistor or leaving it open results in fixed delay times (see Electrical Characteristics). Connecting this pin to a ground referenced capacitor ≥ 100pF gives a user-programmable delay time. See the ***SELECTING THE RESET DELAY TIME*** section for more information.
5	SENSE	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then RESETN is asserted.
6	VDD	Supply voltage. It is good analog design practice to place a 0.1μF ceramic capacitor close to this pin.

Functional Block Diagram

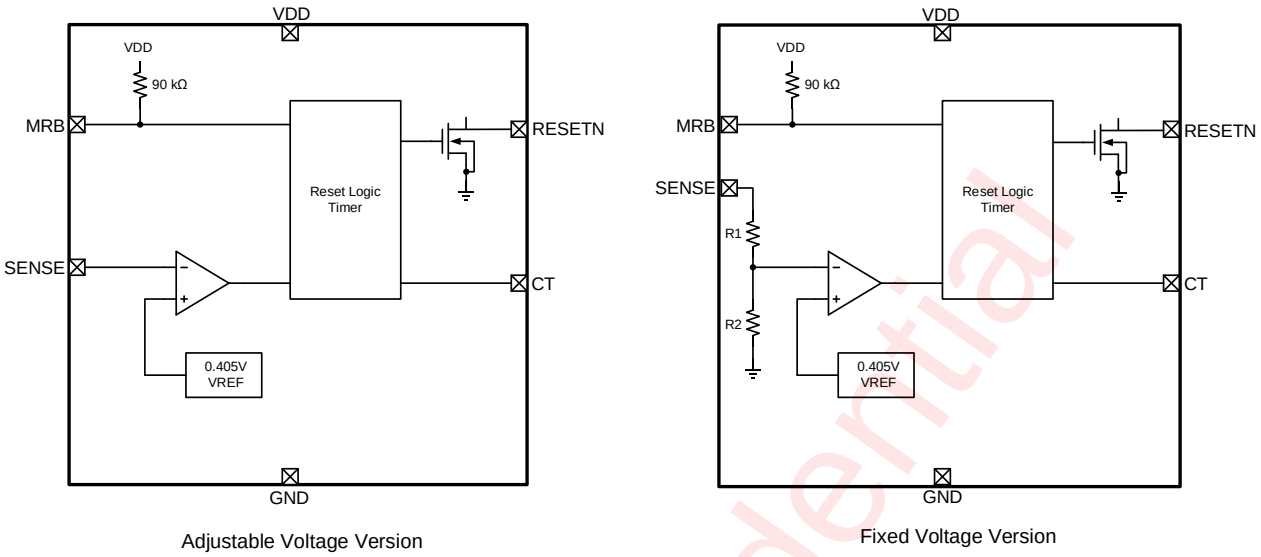


Figure 3 AWS703808 Function Block

Typical Application Circuits

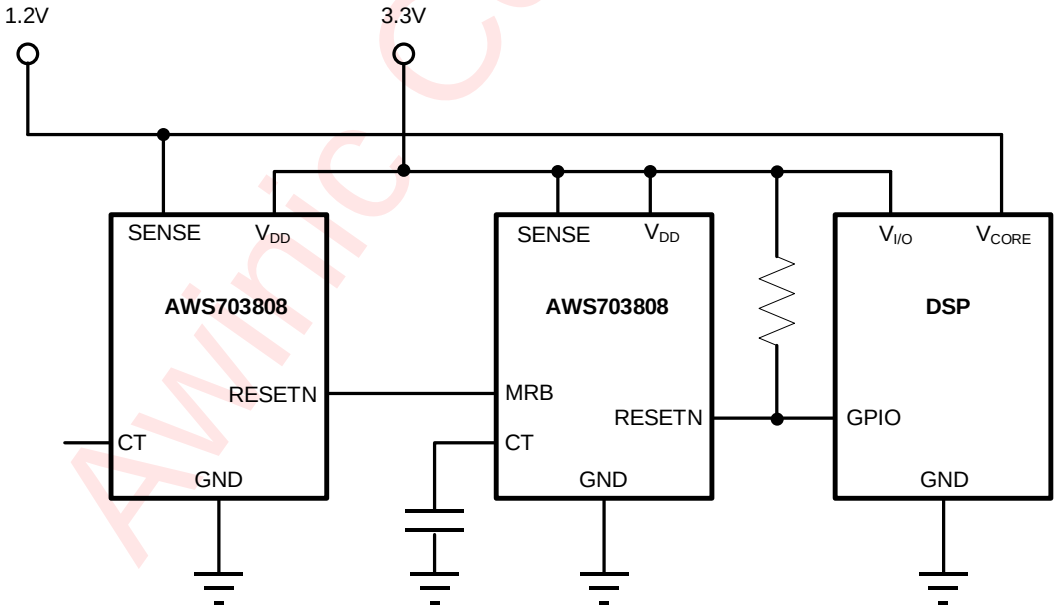


Figure 4 AWS703808 Application Circuit

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS703808ADJCSTR	-40°C～125°C	SOT23-6L	6MNH	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (NOTE1)

PARAMETERS		MIN	MAX	UNIT
Voltage	VDD	-0.3	6.0	V
	V_{CT}	-0.3	V_{DD}+0.3	V
	V_{SENSE}, V_{MRB}, V_{SENSE}	-0.3	6.0	V
Current	RESETN pin	-0.5	5	mA
Operating free-air temperature range		-40	125	°C
Maximum operating junction temperature T_{JMAX}(NOTE2)		-40	150	°C
Storage temperature T_{STG}		-65	150	°C

PARAMETERS	RANGE
ESD(Including CDM HBM MM)	
Human body model(All pins,per ESDA/JEDEC JS-001) (NOTE3)	±4KV
Charged device model(All pins,per ESDA/JEDEC JS-002) (NOTE4)	±2KV
Latch-up	
Test condition:JEDEC78E	±200mA

NOTE1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE2: As a result of the low dissipated power in this device, it is assumed that TJ = TA.

NOTE3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017

NOTE4: Test method: ESDA/JEDEC JS -002-2018

Thermal Information

THERMAL METRICS		AWS703808	UNIT
		SOT	
SYMBOL	PARAMETER	6PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	°C/W
$R_{\theta JC}$	Junction-to-case(top) thermal resistance	118	°C/W

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MIN	MAX	UNIT
V_{DD}	Input supply voltage	1.7	5.5	V
V_{SENSE}	SENSE pin voltage	0	5.5	V
V_{CT}	CT pin voltage		V_{DD}	V
V_{MRB}	MRB pin voltage	0	5.5	V
V_{RESETN}	RESETN pin voltage	0	5.5	V
I_{RESETN}	RESETN pin current	0	10	mA

Electrical Characteristics

DC Electrical Characteristics

1.7V ≤ V_{DD} ≤ 5.5V, $R_{LRESETN}$ = 100kΩ, C_{LRESET} = 50pF, over operating temperature range (T_A = -40°C to 125°C), unless otherwise noted. Typical values are at T_A = 25°C(NOTE1).

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range		-40°C < T_A < 125°C	1.7		5.5	V
			-40°C < T_A < 85°C	1.65		5.5	V
I_{DD}	Supply current (current into VDD pin)		V_{DD} = 3.3V, RESETN not asserted, MRB, RESETN, CT open		2.2	6	μA
			V_{DD} = 5.0V, RESETN not asserted, MRB, RESETN, CT open		2.4	7	μA
V_{OL}	Low-level output voltage		1.3V ≤ V_{DD} < 1.8V, I_{OL}=0.4mA			0.3	V
			1.8V ≤ V_{DD} ≤ 5.5V, I_{OL}=1.0mA			0.4	V
V_{POR}	Power-up reset voltage (NOTE2).		V_{OL}(max) = 0.2V, I_{RESETN} = 15μA			0.8	V
V_{IT}	Negative-going input threshold accuracy	AWS703808ADJ			±2.5%		
		V_{IT} ≤ 3.3V			±2.5%		
		3.3V < V_{IT} ≤ 5.0V			±2.5%		
V_{HYS}	Hysteresis on V_{IT} pin	AWS703808ADJ			1.5%		V_{IT}
		Fixed versions			1.0%		
R_{MRB}	MRB Internal pull-up resistance				90		kΩ
I_{SENSE}	Input current at SENSE pin	AWS703808ADJ	V_{SENSE} = V_{IT}			300	nA
		Fixed versions	V_{SENSE} = 5.5V		1.7		μA
I_{OH}	RESETN leakage current		V_{RESETN} = 5.5V, RESETN not asserted (Open Drain)			300	nA
V_{IL}	MRB logic low input					0.3V_{DD}	V
V_{IH}	MRB logic High input			0.7V_{DD}		5.5	V

NOTE1: $R_{LRESETN}$ and $C_{LRESETN}$ are the resistor and capacitor connected to the RESETN pin.

NOTE2: The lowest supply voltage (V_{DD}) at which RESETN becomes active.

Switching Characteristics

1.7V ≤ V_{DD} ≤ 5.5V, $R_{LRESETN}$ = 100kΩ, C_{LRESET} = 50pF, over operating temperature range (T_A = -40°C to 125°C), unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
t_W	Input pulse width to RESETN	SENSE	V_{IH} = 1.05V_{IT}, V_{IL} = 0.95V_{IT}		20		μs
		MRB	V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}		0.001		
t_d	RESETN delay time	CT = Open	as Figure 5	10	20	30	ms
		CT = V_{DD}		150	300	500	
		CT = 100pF		0.6	1.5	2	
		CT = 100nF		0.2	0.6	1	s

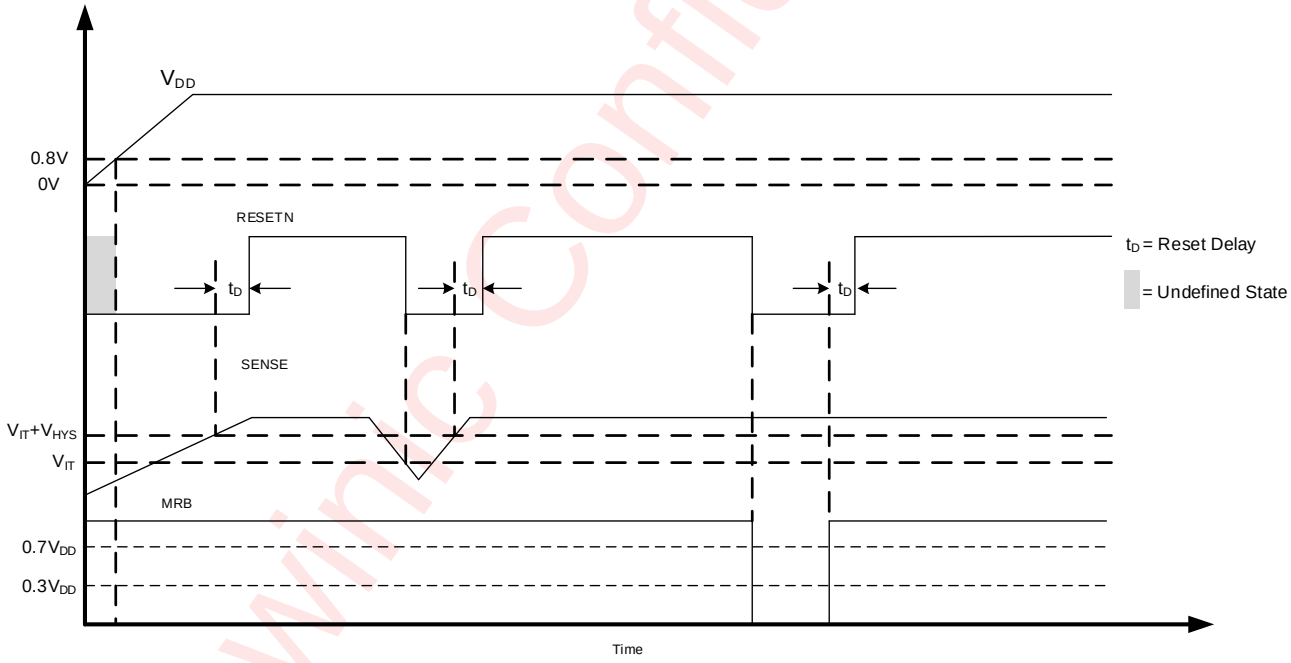
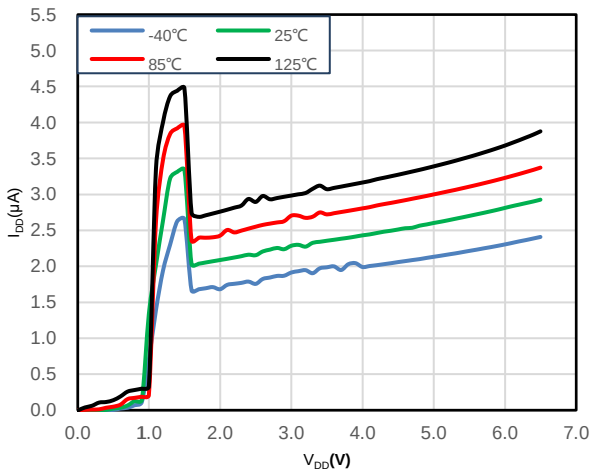


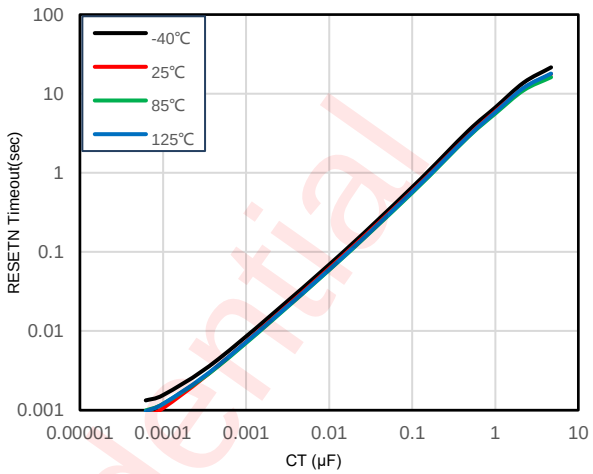
Figure 5 Timing Diagram Showing MRB and SENSE Reset Timing

Typical Characteristics

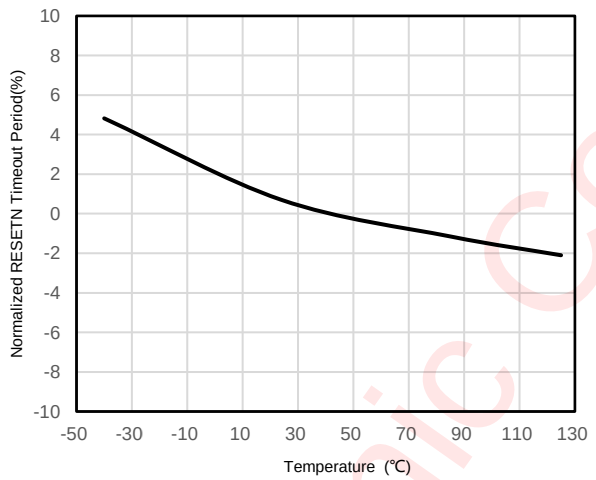
At T_A = 25°C, VDD = 3.3V, $R_{LRESETN}$ = 100kΩ, C_{LRESET} = 50pF, unless otherwise noted.



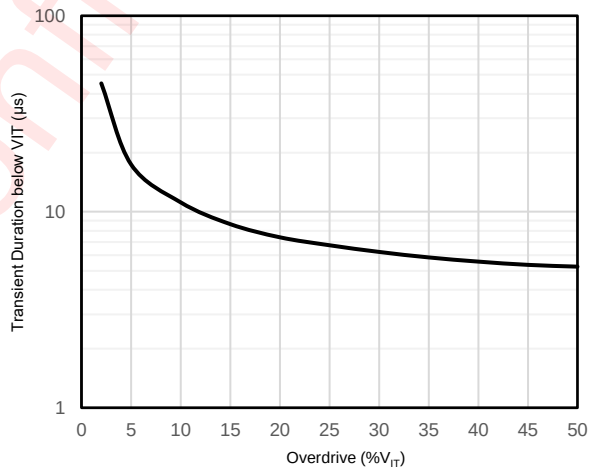
Supply Current vs Supply Voltage



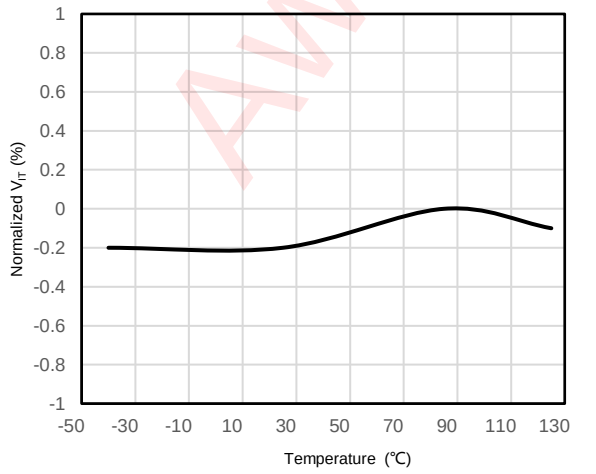
RESETN Time-Out Period vs CT



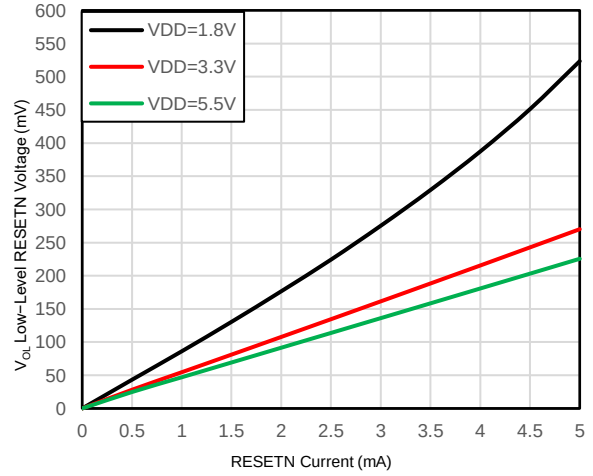
Normalized RESETN Time-Out Period vs Temperature (CT = Open)



Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage



Normalized Sense Threshold Voltage (V_{IT}) vs Temperature



Low-Level RESET Voltage vs RESET Current

Detailed Functional Description

The AWS703808 microprocessor supervisory product family is designed to assert a RESETN signal when either the SENSE pin voltage drops below V_{IT} or the manual reset (MRB) is driven low. The RESET output remains asserted for a user-adjustable time after both the manual reset (MRB) and SENSE voltages return above their respective thresholds.

Functional Block Diagram

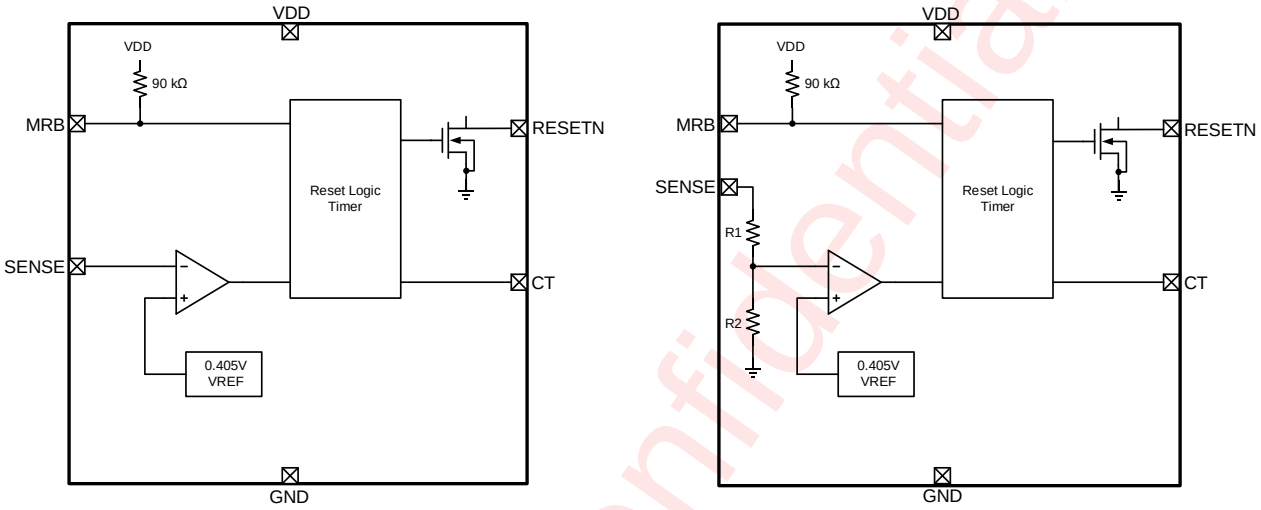


Figure 6 Functional Block Diagram

Feature Description

A broad range of voltage threshold and reset delay time adjustments are available for the AWS703808 device, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5V, while the AWS703808ADJ can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the CT pin to V_{DD} results in a 300ms reset delay, whereas leaving the CT pin open yields a 20ms reset delay. In addition, connecting a capacitor between CT and GND allows the designer to select any reset delay period from 1.25ms to 10s.

SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then RESETN is asserted. The comparator has a built-in hysteresis to ensure smooth RESETN assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitic. The AWS703808 device is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive. The AWS703808ADJ can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 7.

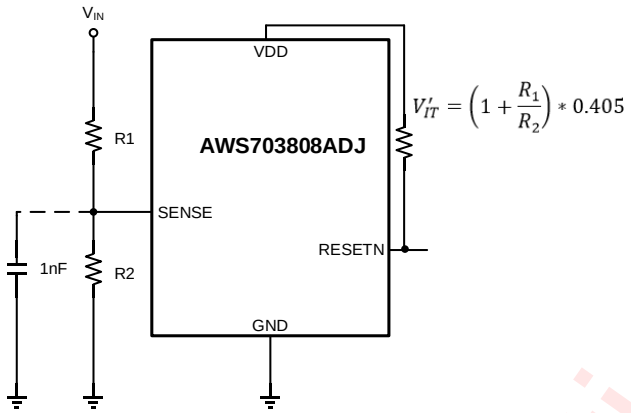


Figure 7 Using the AWS703808ADJ to Monitor a User-Defined Threshold Voltage

Selecting the RESET Delay Time

The AWS703808 has three options for setting the RESETN delay time as shown in Figure 8. Figure 8 (a) shows the configuration for a fixed 300ms typical delay time by tying CT to V_{DD}; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected by the choice of resistor. Figure 8 (b) shows a fixed 20ms delay time by leaving the CT pin open. Figure 8 (c) shows a ground referenced capacitor connected to CT for a user-defined program time between 1.25ms and 10s.

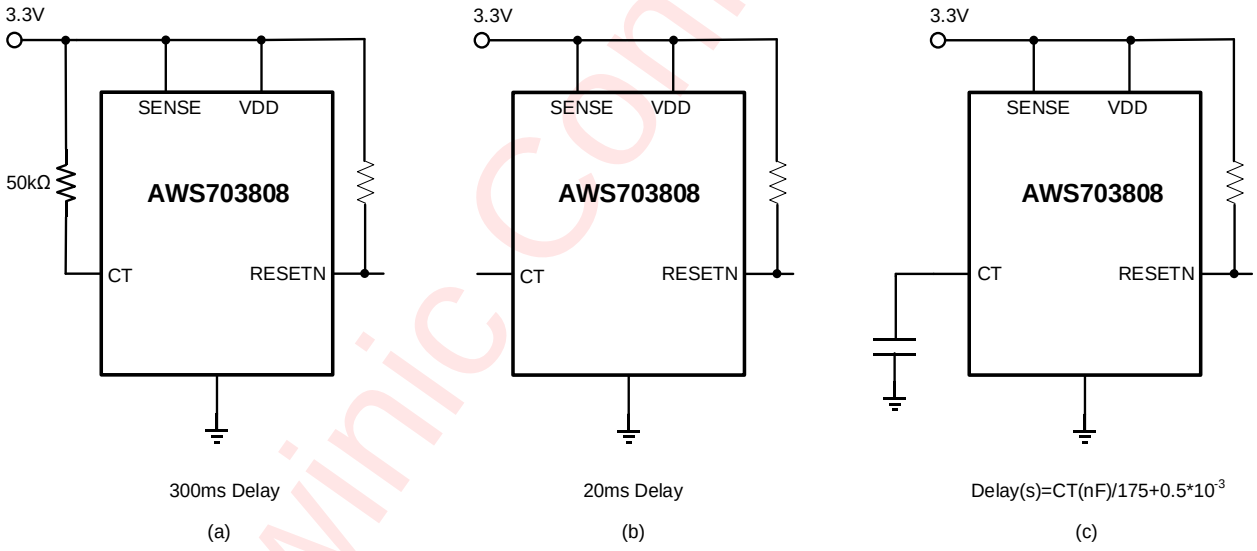


Figure 8 Configuration Used to Set the RESETN Delay Time

The capacitor CT should be ≥ 100pF nominal value in order for the AWS703808 to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using Equation.

$$C_T(nF) = [t_D(s) - 0.5 * 10^{-3}(s)] * 175$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.25V. When a RESETN is asserted, the capacitor is discharged. When the RESETN conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.25V, RESETN is deasserted. Note that a low-leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

Manual RESET (MRB) Input

The manual reset (MRB) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3VDD) on MRB causes RESETN to assert. After MRB returns to a logic high and SENSE is above its reset threshold, RESETN is de-asserted after the user-defined reset delay expires. Note that MRB is internally tied to VDD using a 90kΩ resistor, so this pin can be left unconnected if MRB is not used. See Figure 9 for how MRB can be used to monitor multiple system voltages. Note that if the logic signal driving MRB does not go fully to VDD, there is some additional current draw into VDD as a result of the internal pull-up resistor on MRB. To minimize current draw, a logic-level FET can be used as illustrated in Figure 10.

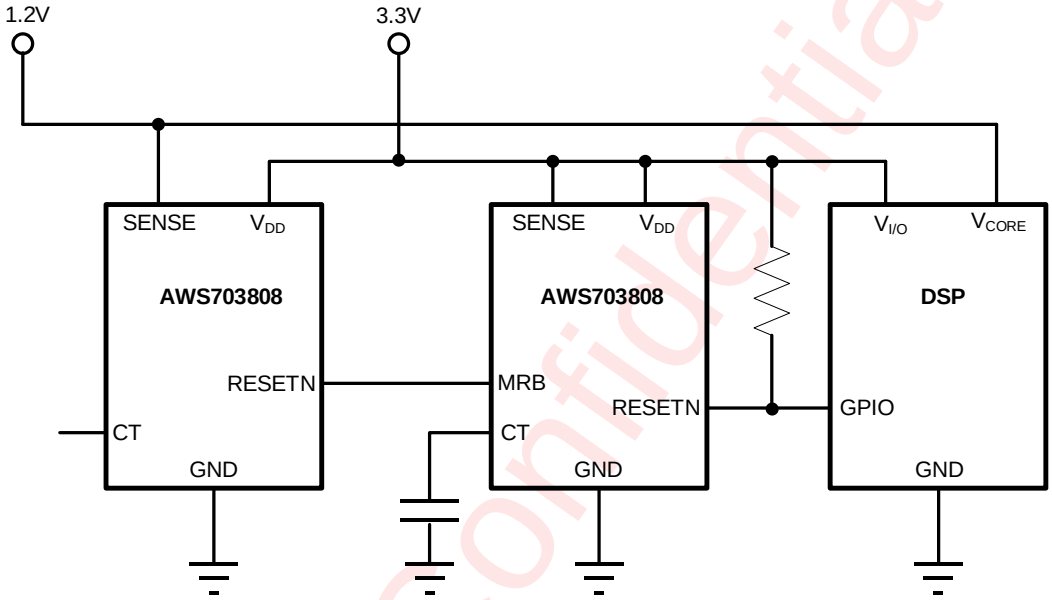


Figure 9 Using MRB to Monitor Multiple System Voltages

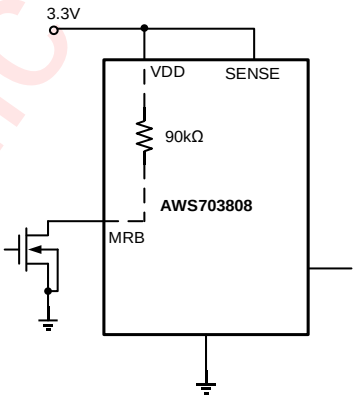


Figure 10 Using an External MOSFET to Minimize I_{DD} When MRB Signal Does Not Go to V_{DD}

RESENT Output

RESETN remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset (MRB) is logic high. If either SENSE falls below V_{IT} or MRB is driven low, RESETN is asserted, driving the RESETN pin to a low impedance. Once MRB is again logic high and SENSE is above V_{IT} + V_{HYS} (the threshold hysteresis), a delay circuit is enabled that holds RESETN low for a specified reset delay period. Once the reset delay has expired, the RESETN pin goes to a high impedance state.

Device Functional Modes

Table1 Truth Table

MRB	SENSE > V_{IT}	RESETN
L	0	L
L	1	L
H	0	L
H	1	H

Normal Operation (V_{DD} > $V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the RESETN signal is determined by the voltage on the SENSE pin and the logic state of MRB.

- MRB high: When the voltage on V_{DD} is greater than 1.7V for a time of the selected t_D, the RESETN signal corresponds to the voltage on SENSE relative to V_{IT}.
- MRB low: in this mode, RESETN is held low regardless of the value of the SENSE pin.

Above Power-On Reset but Less Than $V_{DD(min)}$ (V_{POR} < V_{DD} < $V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the RESETN signal is asserted and low impedance, respectively, regardless of the voltage on the SENSE pin.

Below Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) needed to internally pull the asserted output to GND, RESETN is undefined and should not be relied upon for proper device function.

Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

Typical Application

A typical application of the AWS703808 used with a 2.5V processor is shown in Figure 11. The open-drain RESET output is typically connected to the RESET input of a microprocessor. A pullup resistor must be used to hold this line high when RESET is not asserted. The RESETN output is undefined for voltage below 0.8V, but this characteristic is normally not a problem because most microprocessors do not function below this voltage.

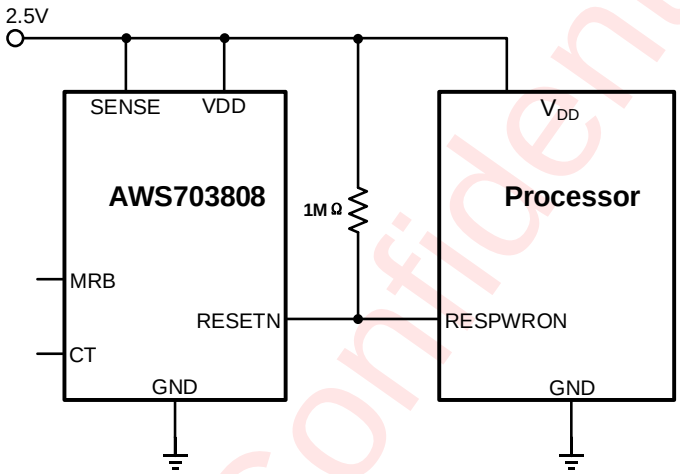


Figure 11 Typical Application of the AWS703808 With an Processor

Design Requirements

The AWS703808 is intended to drive the RESETN input of a microprocessor. The reset delay time is controlled by CT depending on the reset requirement times of the microprocessor. In this case, CT is left open for a typical reset delay time of 20ms.

Detailed Design Procedure

The primary constraint for this application is the reset delay time. In this case, because CT is open, it is set to 20ms. The MRB pin can be connected to an external signal if desired.

Immunity to SENSE Pin Voltage Transients

The AWS703808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive. Threshold overdrive is defined by how much the V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the RESETN response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation:

Overdrive = | (V_{SENSE} / V_{IT} – 1) × 100% |

where:

- V_{IT} is the threshold voltage.

PCB Layout Consideration

AWS703808 PCB layout should be considered. Here are some guidelines:

1. Make sure the connection to the VDD pin is low impedance. Place a 0.1μF ceramic capacitor near the VDD pin.
2. If no capacitor is connected to the CT pin, parasitic capacitance on this pin should be minimized so the RESETN delay time is not adversely affected.
3. The layout example in Figure 12 shows how the AWS703808 is laid out on a printed circuit board（PCB）for a 20ms delay.
4. The AWS703808ADJ can be used to monitor any voltage rail down to 0.405V using the circuit board(PCB) shown in Figure 13.

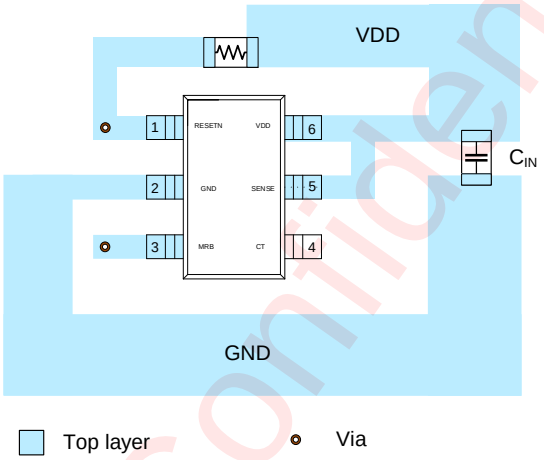


Figure 12 Layout example for a 20ms delay

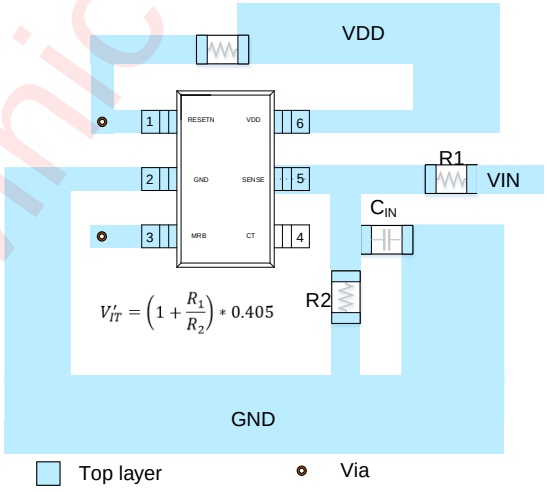
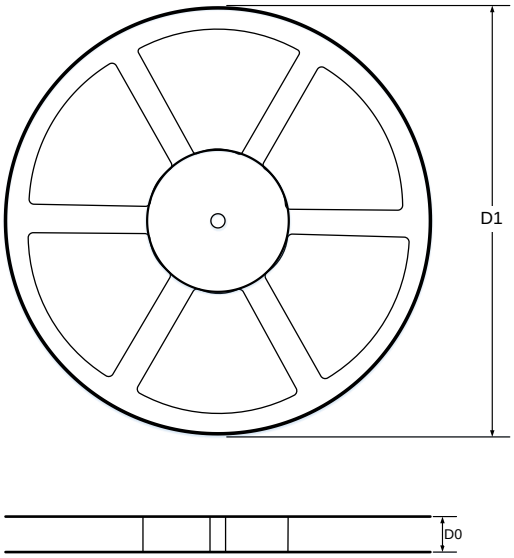


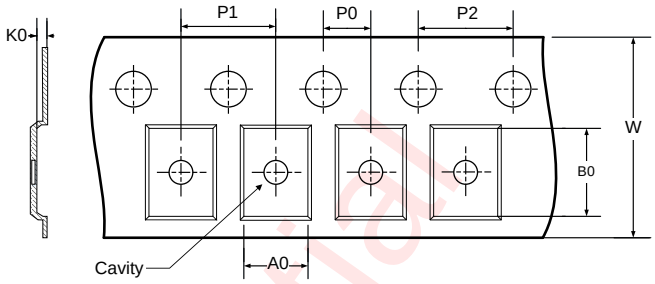
Figure 13 Layout example for V_{IT} can configuration

Tape And Reel Information

REEL DIMENSIONS

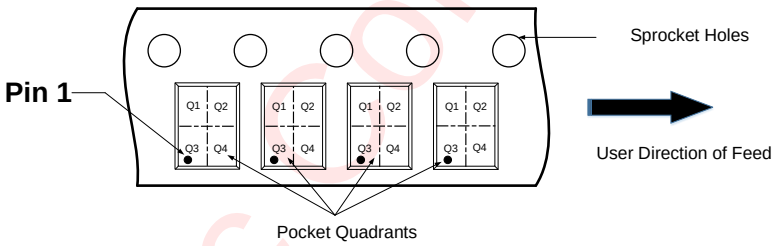


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



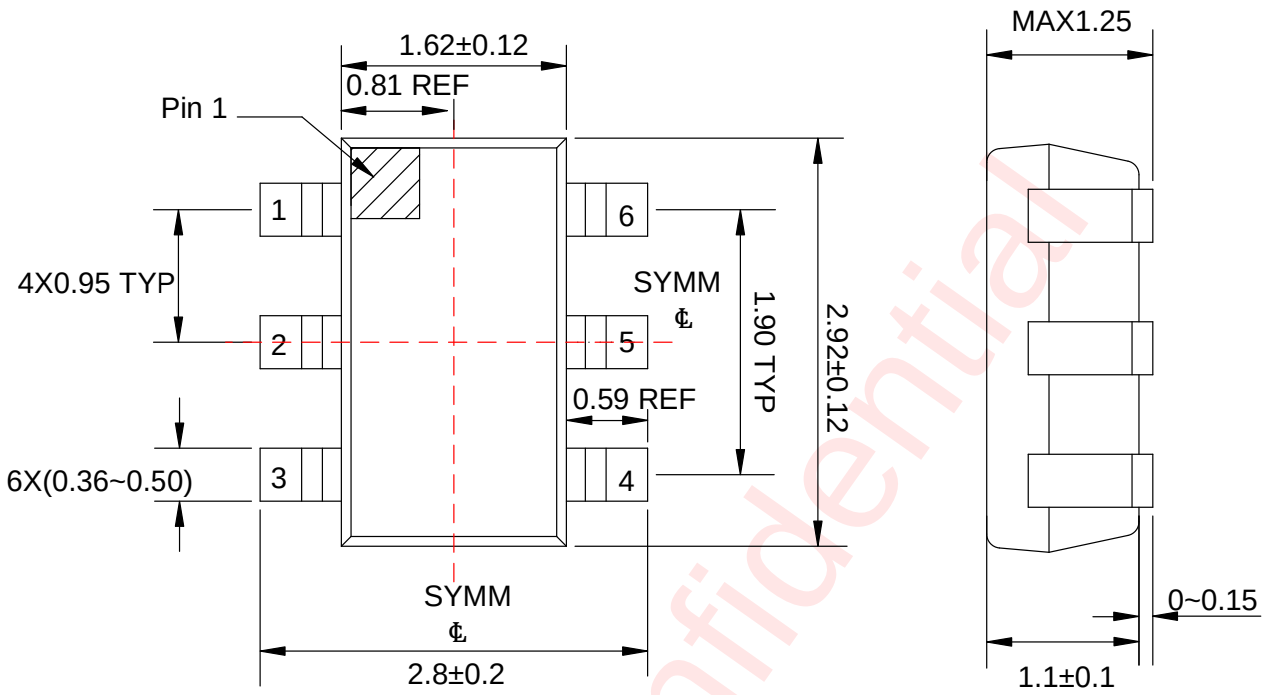
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

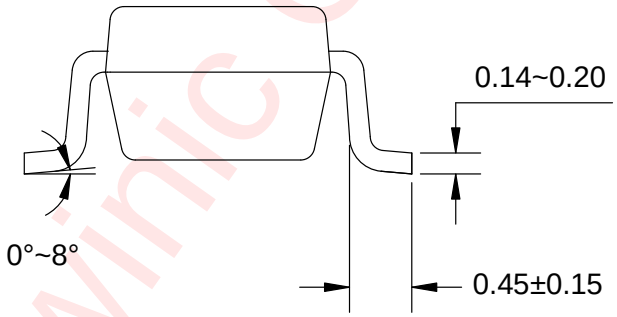
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178.0	8.4	3.3	3.2	1.4	2.0	4.0	4.0	8.0	Q3

All dimensions are nominal

Package Description(POD)



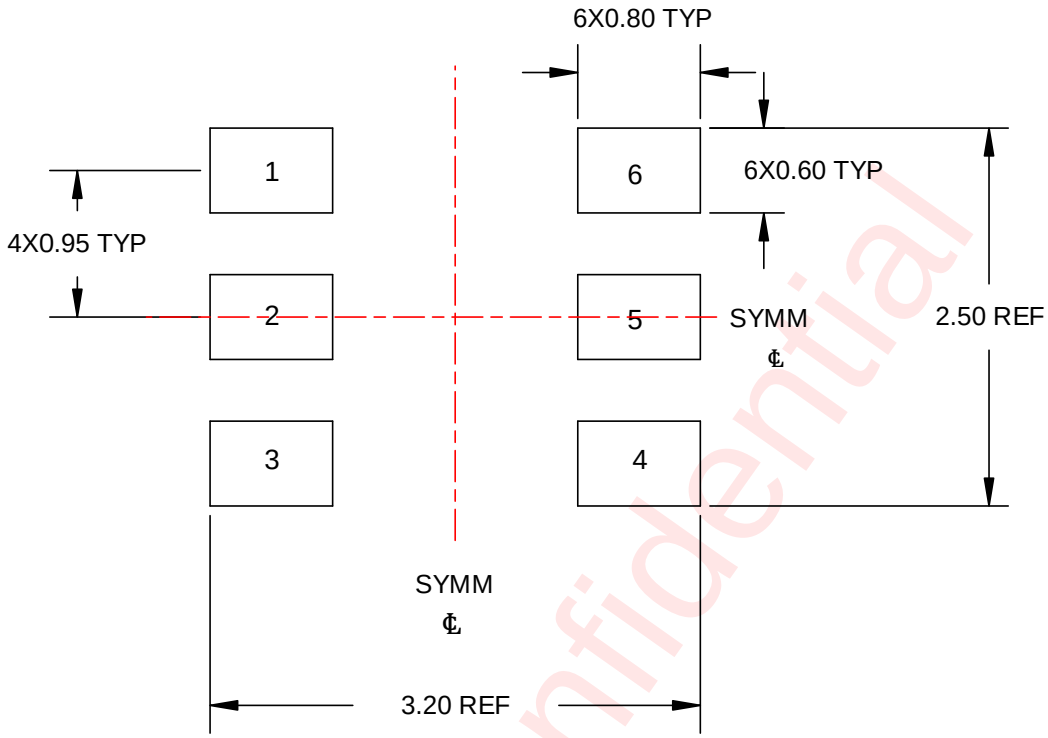
Top View **Side View**

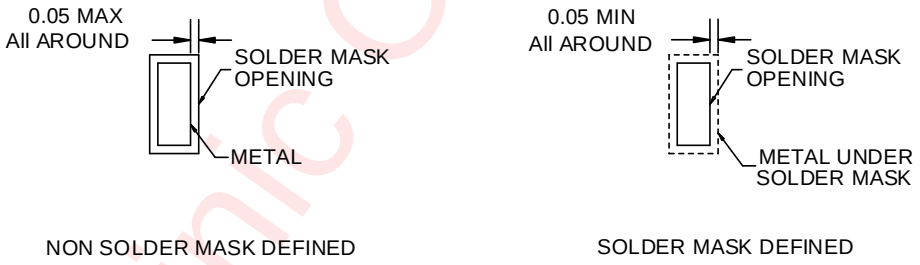


Side View

Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Nov. 2023	Datasheet V1.0 released.
V1.1	Nov. 2024	1. Update the typical Application Circuit(P2、P4、P11、P12、P14) 2. Update ESD(P5) 3. Update tape and reel information(P16) 4. Update package description(P17)
V1.2	Oct. 2025	1. Add parameters: $R_{\theta JA}$、$R_{\theta JC}$ (P6)

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