AW35615 Programmable USB Type-C PD Controller

FEATURES

- Dual-role functionality with autonomous DRP toggle
- Attach/Detach detection as either a host or a device based on what has been attached
- Operate as dedicated host, dedicated device or DRP by host software configuration
- Support USB PD 3.0 except Fast Role Swap function
- USB PD 3.0 certified (TID #8339)
- Integrate the several functionality of the CC Pins according to Type-C 1.2
- Integrate VCONN switch with configurable OCP and OTP
- VBUS detection and discharge control
- Dead Battery Support (SNK mode support when no power applied)
- Higher withstand voltage value of CC pins: 24V
- Support wake detection avoids CC voltage toggle to prevent electric corrosion
- BIST mode supported
- WBQFN 2.5 mm × 2.5 mm-14L package

APPLICATIONS

- Smartphones
- Power Adapters
- Tablets
- Automotive

GENERAL DESCRIPTION

The AW35615 is a programmable DRP/SRC/SNK USB Type-C controller that compiles with USB PD3.0 and Type-C 1.2 specifications, and it integrates a complete Type-C transceiver including the pull-up and pull-down resistors.

The AW35615 enables the USB Type-C detection including attach and orientation by autonomous DRP toggle. The CC logic block monitors the CC1/CC2 pin for pull-up or pull-down resistances to determine when a USB port has been attached, the orientation of the cable and the role detected. Furthermore, AW35615 supports wake detection without CC voltage toggle, which brings lower power and avoids electric corrosion due to voltage toggle.

The AW35615 integrates the physical layer of the USB BMC Power Delivery protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

The AW35615 supports VBUS voltage detection and discharge control by the discharge resistance integrated in VBUS channel. The withstand voltage value of CC pins is up to 24V.

TYPICAL APPLICATION CIRCUIT

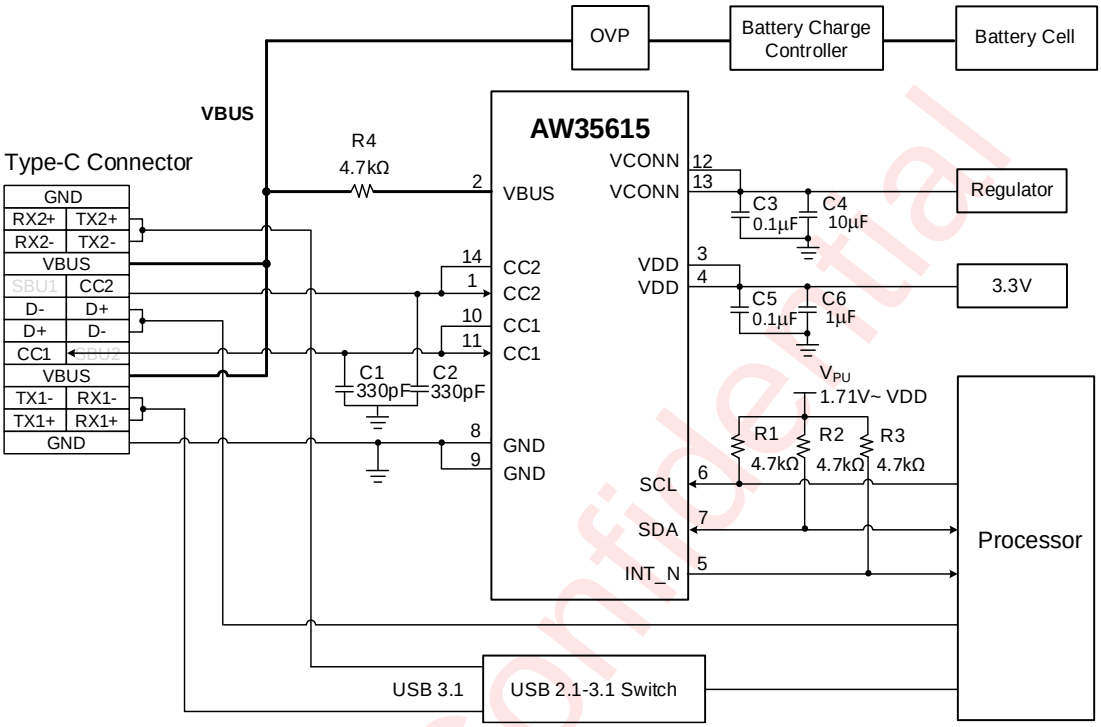


Figure 1 Typical Application Circuit of AW35615

PIN CONFIGURATION AND TOP MARK

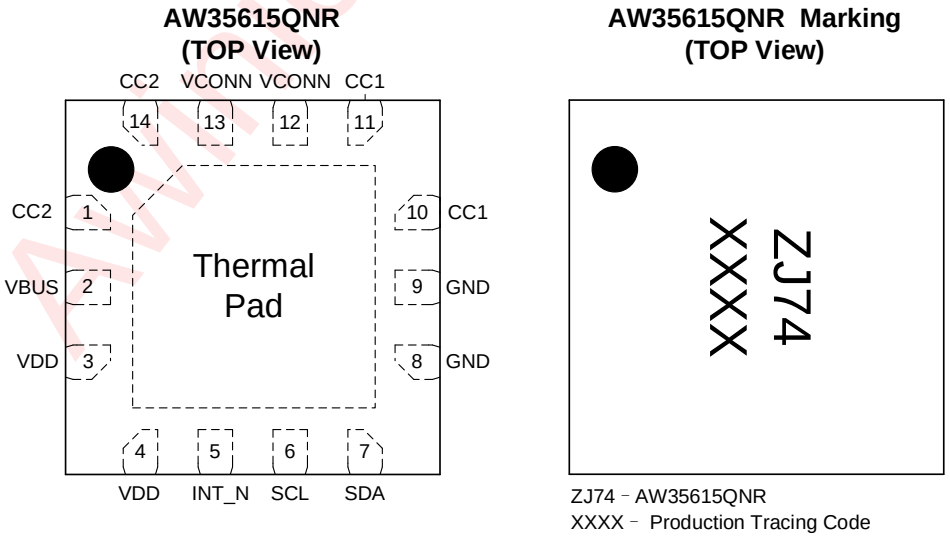


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1/14	CC2	Type-C Connector Configuration Channel (CC) pins. It determines Type-C attach status and CC orientation. CC pins implement different function base on power role. Function as host : 1. Sets the allowable charging current for VBUS. 2. Communicates with devices according to USB BMC Power Delivery. 3. Detects when a detach occurred. Function as device: Indicates the allowable sink current from the attached host and communicates with host according to USB BMC Power Delivery.
2	VBUS	VBUS input pin for attach and detach detection.
3/4	VDD	Input supply voltage.
5	INT_N	Open drain type interrupt output used to prompt the processor to read the registers.
6	SCL	I^2C serial clock signal to be connected to the I^2C master.
7	SDA	I^2C serial data signal to be connected to the I^2C master.
8/9	GND	Ground
10/11	CC1	Type-C Connector Configuration Channel (CC) pins. It determines Type-C attach status and CC orientation. CC pins implement different function base on power role. Function as host : 1. Sets the allowable charging current for VBUS. 2. Communicates with devices according to USB BMC Power Delivery. 3. Detects when a detach occurred. Function as device: Indicates the allowable sink current from the attached host and communicates with host according to USB BMC Power Delivery.
12/13	VCONN	Regulated input pin to be switched to correct CC pin as VCONN to power Type-C full-featured cables and other accessories.

Note: The thermal pad is GND

FUNCTIONAL BLOCK DIAGRAM

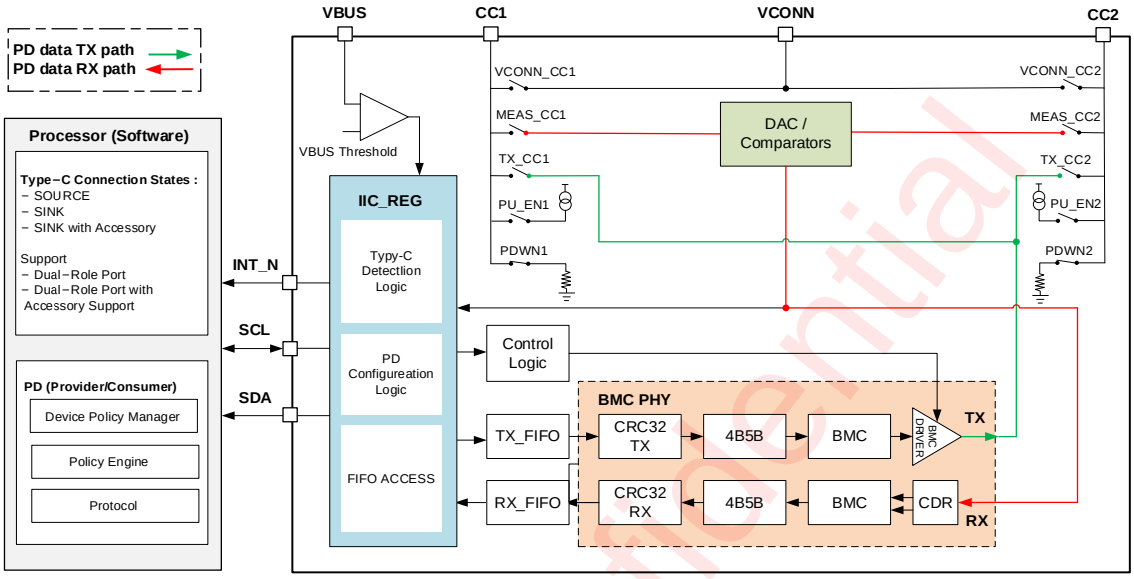


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUIT

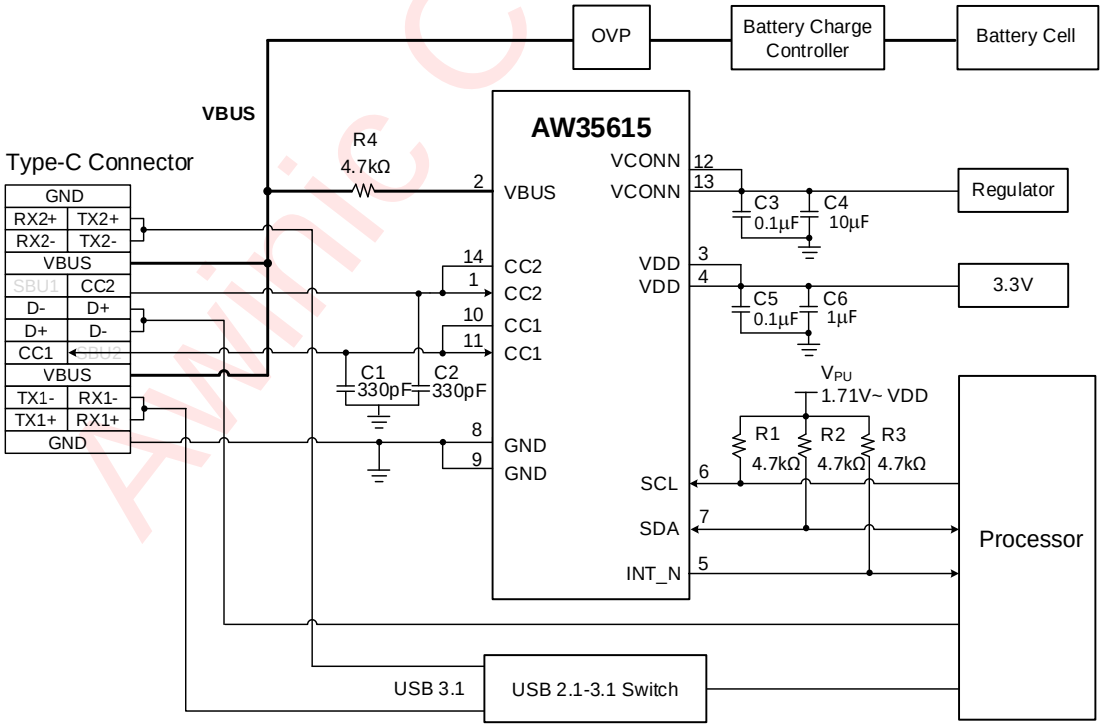


Figure 4 Typical Application Circuit of AW35615

Notice for typical application circuits:

1: SCL/SDA/INT_N is Open Drain output, so a 1K~10K pull-up resistance is needed for each pin.

2: Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1uF ceramic bypass capacitors are necessary between VDD and ground, placed close to the device, not far away from input trace.

3: The capacitance of CC pins will affect the quality of BMC, the recommended capacitance of the whole CC line is 200pF~600pF. The CC pins don't need additional capacitance when the equivalent capacitance of TVS is close to 600pF.

4: The R4 is for better for surge.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35615QNR	-40°C ~ 85°C	WBQFN 2.5mm × 2.5mm × 0.75mm – 14L	ZJ74	MSL1	RoHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range	VDD	-0.3V to 6V
	VCONN	-0.3V to 6V
	VBUS	-0.3V to 28V
I/O voltage range	CC1, CC2	-0.3V to 24V
	SCL,SDA	-0.3V to 6V
	INT_N	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		81.5°C /W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)		
HBM: ESDA/JEDEC JS-001(NOTE2)		±4.0kV

PARAMETERS	RANGE
CDM: ESDA/JEDEC JS-002(NOTE3)	±1.5kV
Latch-Up	
Test condition: JESD78E	±200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: All pins. Test Condition: ESDA/JEDEC JS 001 2017.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS 002 2018.

RECOMMEND OPERATING CONDITIONS

PARAMETERS		MIN	TYP	MAX	UNIT
Supply voltage range	VDD	2.7	3.3	5.5	V
	VCONN	2.7	–	5.5	V
	VBUS	4.0	5.0	21.0	V
Supply current range	VCONN	–	–	560	mA
Operating temperature T_A		−40	–	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, VDD = 3.3V for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PD SIGNAL						
UI	Unit interval		3.03	–	3.70	µs
PD TRANSMITTER						
z_{Driver}	Transmitter output impedance		33	–	75	Ω
V_{OH}	Logic high voltage		1.05	1.125	1.20	V
V_{OL}	Logic low voltage		0	–	75	mV
$t_{EndDriveBMC}$	Time to cease driving the line after the end of the last bit of the frame		–	–	23	µs
$t_{HoldLowBMC}$	Time to cease driving the line after the final high-to-low transition		1	–	–	µs
$t_{StartDrive}$	Time before the start of the first bit of the preamble when the transmitter shall start driving the line		−1	–	1	µs
t_{RISE_TX}	Rise time		300	–	–	ns
t_{FALL_TX}	Fall time		300	–	–	ns
PD RECEIVER						
$C_{Receiver}$	Receiver capacitance when driver isn't turned on		–	50	–	pF
Z_{BmcRx}	Receiver input impedance		1	–	–	MΩ

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{RxFilter}$	Rx bandwidth limiting filter		100	–	–	ns
TYPE-C CC SWITCH						
R_{SW_CCx}	R_{DSON} for VCONN switch	VCONN = 3V to 5.5V	–	0.9	1.2	Ω
I_{SW_CCx}	Over-Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range	VCONN = 3V to 5.5V PWR = 4'h1 VCONN_ CC1/2 = 1 OCP_RANGE = 1 OCP_CUR = 3'h7	600	800	1000	mA
$t_{SoftStart}$	Time taken for the VCONN switch to turn on during which Over-Current Protection is disabled	VCONN = 3V to 5.5V PWR = 4'h7 VCONN_ CC1/2=1	–	1.7	–	ms
I_{80_CCx}	SRC 80 µA CC current (Default)	PU_EN1/2 = 1 HOST_CUR = 2'b01	64	80	96	µA
I_{180_CCx}	SRC 180 µA CC current (1.5 A)	PU_EN1/2 = 1 HOST_CUR = 2'b10	166	180	194	µA
I_{330_CCx}	SRC 330 µA CC current (3 A)	PU_EN1/2 = 1 HOST_CUR = 2'b11	304	330	356	µA
V_{UFPDB}	SNK pull-down voltage in Dead Battery under all pull-up SRC Loads	VDD = 0V	–	–	2.18	V
R_{DEVICE}	Device pull-down resistance	PDWN1/2 = 1	4.6	5.1	5.6	kΩ
z_{OPEN}	CC resistance for disabled state	PU_EN1/2 = 0 PDWN1/2 = 0	126	–	–	kΩ
$WAKE_{Low}$	Wake threshold for CC pins SRC or SNK LOW value	PWR = 4'h1 WAKE_EN = 1 MEAS_CC1/2 = 1	–	0.25	–	V
$WAKE_{high}$	Wake threshold for CC pins SRC or SNK HIGH value	PWR = 4'h1 WAKE_EN = 1 MEAS_CC1/2 = 1	–	1.45	–	V
V_{BC_LVLhys}	Hysteresis on the Ra and Rd Comparators		–	20	–	mV
V_{BC_LVL}	CC pin thresholds BC_LVL = 2'b00 BC_LVL = 2'b01	PWR = 4'h7 PDWN1/2 = 1 MEAS_CC1/2 = 1	 0.15 0.61	 0.20 0.66	 0.25 0.70	V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
	BC_LVL = 2'b10		1.16	1.23	1.31	
$V_{MDACstepCC}$	Measure block MDAC step size for each code in MDAC[5:0]	PWR = 4'h7 MEAS_CC1/2 = 1 MDAC = X	–	42	–	mV
$V_{MDACstepVBUS}$	Measure block MDAC step size for each code in MDAC[5:0] for VBUS measurement	PWR = 4'h7 MEAS_CC1/2= 0 MEAS_VBUS = 1 MDAC = X	–	420	–	mV
$V_{VBUSthr}$	VBUS threshold at which I_VBUSOK interrupt is triggered.	PWR = 4'h7 INT_MASK = 0	–	–	4.0	V
t_{TOG1}	When TOGGLE = 1, time at which internal versions of PU_EN1 = PU_EN2 = 0 and PDWN1 = PDWN2 = 1 selected to present externally as a SNK in the DRP toggle	PWR = 4'h1 TOGGLE = 1	30	45	60	ms
t_{TOG2}	When TOGGLE = 1, time at which internal versions of PU_EN1 = PU_EN2 = 1 and PDWN1 = PDWN2 = 0 selected to present externally as a SRC in the DRP toggle	PWR = 4'h1 TOGGLE = 1	20	30	40	ms
t_{DIS}	Disable time after a full toggle (t_{TOG1} + t_{TOG2}) cycle so as to save power TOG_SAVE_PWR = 00 TOG_SAVE_PWR = 01 TOG_SAVE_PWR = 10 TOG_SAVE_PWR = 11	PWR = 4'h1 TOG_SAVE_PWR = 00/01/10/11 TOGGLE = 1	– – – –	0 40 80 160	– – – –	ms
T_{shut}	Temp. for VCONN switch off	PWR = 4'h3 VCONN_ CC1/2 = 1	–	145	–	°C
T_{hys}	Temp. hysteresis for VCONN switch turn on	PWR = 4'h3 VCONN_ CC1/2 = 1	–	10	–	°C
CURRENT CONSUMPTION						

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{disable}$	The CC pins expose Rd and disables all function expect I^2C function	Nothing attached PWR[3:0] = 4'h0	–	0.37	5	μA
I_{SB_SNK}	Sink current consumption in cable attached, and enable PD clock	Attached a SRC in SNK mode, and PWR=4'hF	0.5	0.9	1.8	mA
I_{idle_SNK}	Sink current consumption in cable attached	Attached a SRC in SNK mode, and PWR=4'h7	30	53	90	μA
I_{SB_SRC}	Source current consumption in cable attached, and enable PD clock	Attached a SNK in SRC mode, and PWR=4'hF	0.5	1.3	2.5	mA
I_{idle_SRC}	Source current consumption in cable attached	Attached a SNK in SRC mode, and PWR=4'h7	100	385	500	μA
I_{tog}	Unattached (standby) toggle current	Nothing attached TOGGLE = 1 PWR[3:0] = 4'h1 WAKE_EN = 0 TOG_SAVE_PWR = 2'b01	–	30	60	μA
I_{VCONN}	VCONN current consumption when VCONN without supply to CC	VCONN port connect 5V power	2	5	10	μA
USB PD SPECIFIC PARAMETERS						
$t_{HardReset}$	If a Soft Reset message fails, a Hard Reset is sent after $t_{HardReset}$	PWR = 4'hF MEAS_CC1/2= 1 TX_CC1/2= 1 AUTO_HARD_RESET= 1 AUTO_SOFT_RESET= 1 AUTO_ RETRY= 1	–	–	5	ms
$t_{HardReset\ Complete}$	If it cannot send a Hard Reset within $t_{HardResetComplete}$ because of a busy line, then a I_HARDFAIL interrupt is triggered	PWR = 4'hF SEND_HARD_RESET= 1	–	–	5	ms

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{Receive}$	The CRCReceiveTimer is started upon the last bit of the EOP of the transmitted packet	PWR = 4'hF MEAS_CC1/2 = 1 TX_CC1/2 = 1 AUTO_RETRY = 1	0.9	–	1.1	ms
t_{Retry}	Once the CRCReceiveTimer expires, a retry packet has to be sent out within t_{Retry} time. This time is hard to separate externally from $t_{Receive}$ since they both happen sequentially with no visible difference in the CC output	PWR = 4'hF MEAS_CC1/2 = 1 TX_CC1/2 = 1 AUTO_ RETRY = 1	–	–	75	µs
$t_{SoftReset}$	If a GoodCRC packet is not received within $t_{Receive}$ for NRETRIES then a Soft Reset packet is sent within $t_{SoftReset}$ time	PWR = 4'hF MEAS_CC1/2= 1 TX_CC1/2= 1 AUTO_SOFT_RESET= 1 AUTO_ RETRY= 1	–	–	5	ms
$t_{Transmit}$	From receiving a packet, we have to send a GoodCRC in response within $t_{Transmit}$ time. It is measured from the last bit of the EOP of the received packet to the first bit sent of the preamble of the GoodCRC packet	PWR = 4'hF MEAS_CC1/2 = 1 TX_CC1/2 = 1 AUTO_ CRC = 1	–	–	195	µs
HOST INTERFACE PINS (INT_N)						
V_{OLINTN}	Output low voltage	I_{OL} = 4 mA	–	–	0.4	V
T_{INT_Mask}	Time from global interrupt mask bit cleared to when INT_N goes LOW		50	–	–	µs
I²C INTERFACE PINS						
V_{ILI2C}	Low-level input voltage	SCL, SDA	–	–	0.51	V
V_{IHI2C}	High-level input voltage	SCL, SDA	1.32	–	–	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	SCL, SDA	94	–	–	mV
I_{I2C}	Input current of SDA and SCL pins	Input Voltage 0.26 V to 2.0 V	−1	–	1	µA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OLSDA}	Low-level output voltage (Open-Drain)	I_{OL} = 2 mA	0	–	0.35	V
I_{OLSDA}	Low-level output current (Open-Drain)	V_{OLSDA} = 0.4 V	20	–	–	mA
C_I	Capacitance for each I/O pin		–	5	–	pF

Note: I^2C pull up voltage is required to be between 1.71 V and VDD.

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

The AW35615 is a programmable DRP/SRC/SNK USB Type-C controller that compiles with USB PD3.0 and Type-C 1.2 specifications, which integrates a complete Type-C transceiver including the pull-up and pull-down resistors. The AW35615 supports USB Type-C detection including attach, detach and orientation. The AW35615 supports USB BMC Power Delivery protocol to allow up to 100 W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

POWER UP, INITIALIZATION AND RESET

When power is first applied through VDD, the AW35615 is reset and registers are initialized to the default values shown in the register map. The AW35615 can be reset through host software by programming the SW_RESET bit in the RESET register. All the USB PD logic can be reset by programming the PD_RESET bit in the RESET register. If no power applied to VDD then the SRC can recognize the AW35615 as a sink.

CONFIGURATION CHANNEL SWITCH

The AW35615 integrates the Type-C detection functionality, which works as SRC (host), SNK (device) or Dual-role port (DRP). The function including:

- SNK Port Pull-Down (Rd);
- SRC Port Pull-Up (Ip);
- VCONN Power Switch with OCP for Full Featured USB3.1 Cables;
- USB BMC Power Delivery Physical Layer;
- Configuration Channel (CC) Threshold Comparators;

CC1 and CC2 pin have flexible switch matrix that allows the host software to control the power role of Type-C. The switches on CC are show in Figure 5.

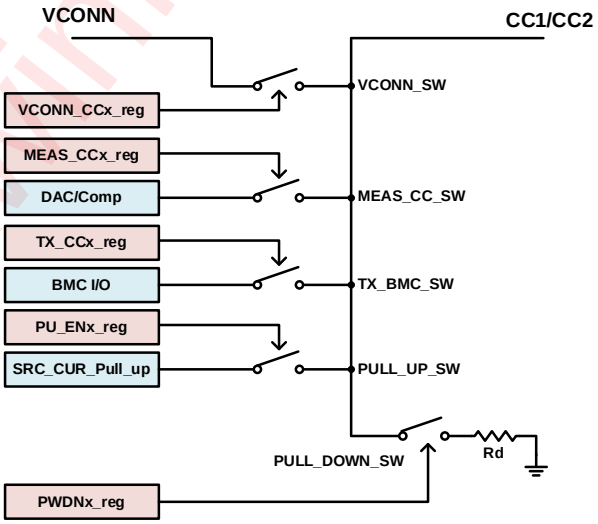


Figure 5 Configuration Channel Switch Functionality

The VCONN_SW determine the voltage of VCONN connect to CC1 or CC2 port, which controlled by bit[4] (VCONN_CC1 Bit) and bit[5] (VCONN_CC2 Bit) in register SWITCHES0. VCONN connect to CC1 (CC2) when VCONN_CC1 (VCONN_CC2) bit is set to “1”.

The MEAS_CC_SW enable measure voltage of CC1/CC2, which controlled by bit[2] (MEAS_CC1 Bit) and bit[3] (MEAS_CC2 Bit) in register SWITCHES0. Type-C function can detect connect, and PD received BMC message through CC1 (CC2) when MEAS_CC1 (MEAS_CC2) bit is set to “1”.

The TX_BMC_SW determine the BMC message is sent by CC1 or CC2, which controlled by bit[0] (TX_CC1 Bit) and bit[1] (TX_CC2 Bit) in register SWITCHES1. BMC message is sent by CC1 (CC2) when TX_CC1 (TX_CC2) bit is set to “1”.

The PULL_UP_SW control the Type-C role as SRC(host), which controlled by bit[6] (PU_EN1 Bit) and bit[7] (PU_EN2 Bit) in register SWITCHES0. CC port work as SRC when PU_EN1 and PU_EN2 bit is set to “1”.

The PULL_DOWN_SW control the Type-C role as SNK(device), which controlled by bit[0] (PDWN1 Bit) and bit[1] (PDWN2 Bit) in register SWITCHES0. CC port work as SNK when PDWN1 and PDWN2 bit is set to “1”.

TYPE-C DETECTION

The AW35615 supports Type-C detection as SRC, SNK or DRP. The AW35615 integrates three fixed threshold comparators and a programmable DAC that can be used by host software to detection the CC voltage and VBUS voltage. The host software judge the Type-C state is attach, detach or charging current with those information.

The three fixed threshold comparators are used to detect the three charging current levels of source which matched the USB Type-C specification.

COMPARATOR OF CC DETECTION

When the state of CC changes, the fixed threshold comparators cause BC_LVL interrupt, and the comparators result is indicated by bit[1:0] (BC_LVL[1:0] Bit) in register STATUS0 (address 0x40). In addition, the 6 bit DAC comparator can measure the CC states accurately. The threshold of DAC is controlled by bit[5:0] (MDAC [5:0]) in register MEASURE (address 0x04). The DAC comparator result is indicated by bit[5] (CMP Bit) in register STATUS0 (address 0x40). The change of DAC detection result will trigger I_COMP interruption.

COMPARATOR OF VBUS DETECTION

The AW35615 has a fixed threshold comparator to determine whether VBUS has reached a valid threshold. The programable 6 bit DAC can also measure voltage of VBUS, when bit[6] (MEAS_VBUS) in register MEASURE (address 0x04) is set to “1”. The DAC can measure voltage of VBUS up to 20V. The host software can determine VBUS voltage to the threshold occurred as expected based on PD or other communication methods to charging level.

AUTOMATIC DETECTION MODE

The AW35615 supports automatic Type-C detection and manual Type-C detection, which controlled by bit[0] (TOGGLE_EN Bit) in register CONTROL2 (address 0x08).

The AW35615 enables automatic detection when the bit TOGGLE_EN is set to “1”. The AW35615 automatically controls the PU_EN, PDWN and MEAS_CC to detect in auto detection mode. The AW35615 supports SNK, SRC and DRP power role, and controlled by bit[2:1] (MODE[1:0] Bit) in register CONTROL2 (address 0x08). The

AW35615 detects the connection of SRC as SNK, when the bit MODE[1:0] is set to “2’b10”. All power role configuration refer to CONTROL2 register description. The processor should initially write HOST_CUR = 2’b01 (for default current) in automatic detection mode. The host software confirms the detection with I_TOGDONE, and determines the type of detection and orientation by reading bit[5:3] (TOGSS Bit) in register STATUS1A (address 0x3D).

TOGSS	Description
3'b000	Toggling
3'b001	Toggle stop SRC on CC1, detect a SNK in CC1 termination
3'b010	Toggle stop SRC on CC2, detect a SNK in CC2 termination
3'b101	Toggle stop SNK on CC1, detect a SRC in CC1 termination
3'b110	Toggle stop SNK on CC2, detect a SRC in CC2 termination
3'b111	Toggle stop Audio, detect Ra both in CC1 and CC2 termination

MANUAL DETECTION MODE

The AW35615 detects connection in manual mode when the bit TOGGLE_EN is set to “0”. The host software controls the bit PU_EN[1:0] and bit PDWN[1:0] to set the power role by I2C, and controls bit MEAS_CC[1:0] to enable measure CC port. The AW35615 confirms the detection according the I_COMP, I_BC_LVL and I_VBUSOK.

The AW35615 detects connection as SNK when PDWN[1:0] is set to “2’b11”. The SNK must monitor VBUS interrupt to determine if it is attached or detached. The SNK can determine SRC current level of CC termination after detect connection, according to BC_LVL and COMP status. Following table shows the result of SNK detection.

Status Type	Interrupt Status				Meaning
	BC_LVL[1:0]	COMP	COMP Setting	VBUSOK	
CC Detection	2'b00	NA	NA	1	vRa
	2'b01	NA	NA	1	vRd, Connect and vRd-USB
	2'b10	NA	NA	1	vRd, Connect and vRd-1.5A
	2'b11	0	6'h34(2.05V)	1	vRd, Connect and vRd-3.0A
Attach	NA	NA	NA	1	SRC Attached, VBUS Valid
Detach	NA	NA	NA	0	SRC Detached, VBUS Invalid

The AW35615 can confirm the connection of CC termination, and the distinguish the type of connection, according the status of comparators and DAC. In addition, the AW35615 supports three charging current capabilities, which is controlled by bit[3:2] (HOST_CUR[1:0] Bit) in register CONTROL0 (address 0x06). If the HOST_CUR bits are change before attach, the AW35615 automatically indicates the current capability after a SNK is connected, otherwise, the AW35615 immediately changes the CC port to current capability.

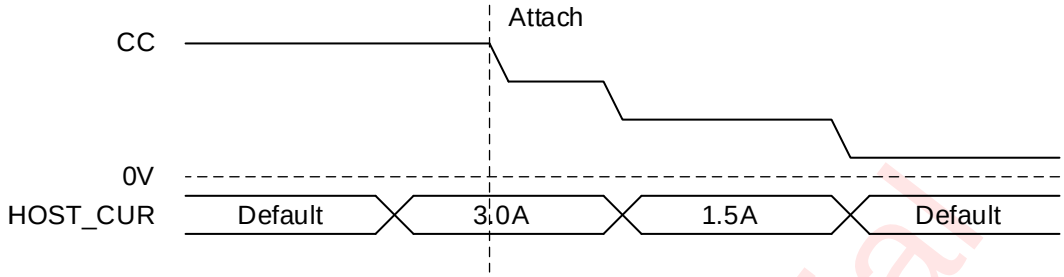


Figure 6 HOST_CUR Changed Before Attach

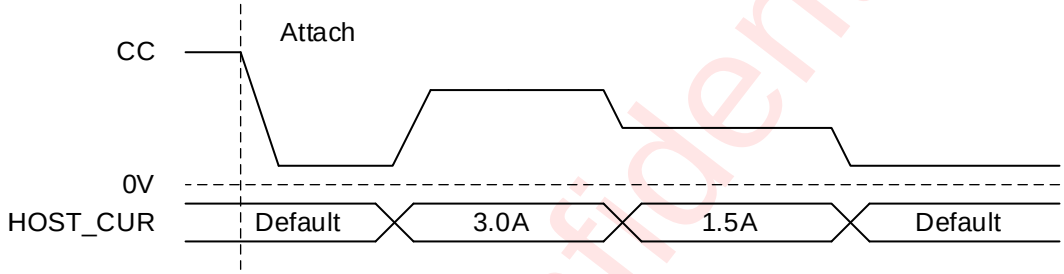


Figure 7 HOST_CUR Changed After Attach

SRC detection threshold is different in different source current level, according the Type-C specification. The host software need adjust the DAC threshold to match the HOST_CUR. SRC can distinguish the CC termination is Ra or Rd when SRC detect attach. The following table summarized connection as SRC according the result of BC_LVL and COMP and HOST_CUR settings.

Termination	HOST_CUR[1:0]	Interrupt Status			Attach/Detach
		BC_LVL[1:0]	COMP	COMP Setting	
Ra	2'b01	2'b00	NA	NA	NA
	2'b10	2'b01	0	6'h0A(0.42V)	
	2'b11	2'b10	0	6'h13(0.8V)	
Rd	2'b01, 2'b10	NA	0	6'h26(1.6V)	Attach
		NA	1	6'h26(1.6V)	Detach
	2'b11	NA	0	6'h3E(2.6V)	Attach
		NA	1	6'h3E(2.6V)	Detach

The Type-C specification allows CC port to be both a SNK and SRC base on type of connection. It is similar to USB OTG ports with the current USB connectors, which is also called Dual Role Port(DRP). The CC port periodically toggles between SRC and SNK in DRP mode. The AW35615 supports the DRP function, and the toggle time is controlled by host software.

VBUS DISCHARGE FUNCTION

The AW35615 supports VBUS discharge for VBUS port. The AW35615 has two types discharge resistance, which is controlled by bit[4:3] (VBUS_DIS_SEL[1:0] Bit) in register CONTROL5 (address 0x11). The AW35615 enables 660 Ω resistance to discharge when VBUS_DIS_SEL is set to “2’b01”. It enables 10 kΩ resistance to discharge when VBUS_DIS_SEL is set to “2’b10”. The AW35615 enables VBUS discharge function after set bit[1] (EN_PAR_CFG Bit) to “1” in register CONTROL4 (address 0x10).

BMC POWER DELIVERY

OVERVIEW

The Type-C connector allows USB Power Delivery (PD) communication over the connected CC pin between two ports. The communication method is the BMC PD protocol and is used for many different reasons with the Type-C connector. Possible uses are outlined below.

- Negotiating and controlling charging power levels
- Alternative Interfaces such as MHL, Display Port
- Role swap for dual-role ports
- Vendor specific interfaces for use with custom docks oraccessories
- Communication with USB3.1 full featured cables

The AW35615 integrates a thin BMC PD client which includes the BMC physical layer and packet FIFOs(48 bytesfor transmit and 80 bytes for receive). The FIFOs allows packets to be sent and received by the host software through I²C accesses. The AW35615 allows host software to implement all features of USB BMC PD through writes and reads of the FIFO and control of the AW35615 physical interface.

The AW35615 uses tokens to control the transmission of BMC PD packets. These tokens are written to the transmit FIFO and control how the packet is transmitted on the CC pin. The tokens are designed to be flexible and support all aspects of the USB PD specification. The AW35615 additionally enables control of the BMC transmitter through tokens. Through burst writing specific token to the FIFO, the transmitter allows faster packet processing with all the information required to transmit a packet.

The AW35615 receiver stores the received data and the received CRC in the receive FIFO when a valid packet is received on the CC pin. The BMC receiver automatically enables the internal oscillator when an activity is sensed on the CC pin and load to the FIFO when a packet is received. The I_ACTIVITY and I_CRC_CHK interrupts alert the host software that a valid packet was received.

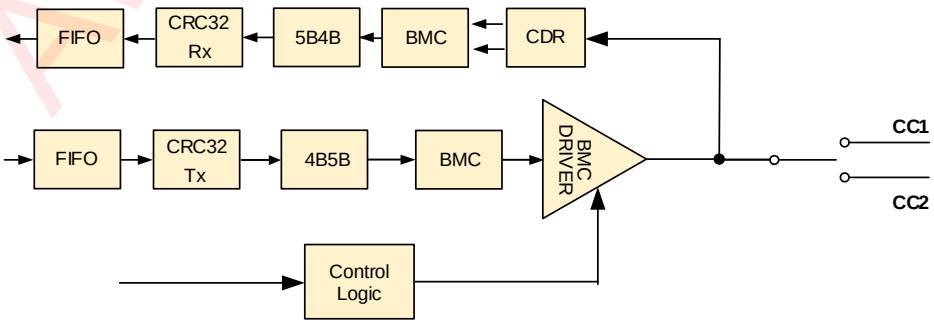


Figure 8 USB BMC Power Delivery Blocks

POWER LEVEL CONFIRMATION

The Type-C specification outlines the prioritization of power level confirmation, covering power levels from the basic USB 2.0 level to the highest level of USB PD. The host software is expected to follow the USB Type-C specification based on charge current priority based on feedback from AW35615 detection, any USB PD communication and external BC1.2 detection. The AW35615 does not integrate BC1.2 charger detection, which is assumed to be available in the USB transceiver or USB charger in the system.

PD AUTOMATICALLY RESPONSE GOODCRC

When the calculated CRC is correct, the Power Delivery packets require a GoodCRC acknowledge packet to be sent for each received packet. This calculation is done by the AW35615 and triggers the I_CRC_CHK interrupt if the CRC is good. If the bit[2](AUTO_CRC) in the SWITCHES1 Register(0x03) is 1 and bit[1](AUTO_PRE) in the CONTROL0 Register(0x06) is 0, then the AW35615 will automatically send the GoodCRC control message in response to reduce the pressure of local processor for responding quickly to the received packet.

PD AUTOMATICALLY SEND RETRIES

If GoodCRC packet is not received and bit[0](AUTO_RETRY) in the CONTROL3 Register(0x09) is 1, then a retry of the same message that was in the TxFIFO written by the processor is executed within t_{Retry} and is repeated for N_RETRIES(bit[2:1] in the CONTROL3 Register(0x09)) times.

The AW35615 implements part of the PD protocol layer for sending packets in an autonomous way.

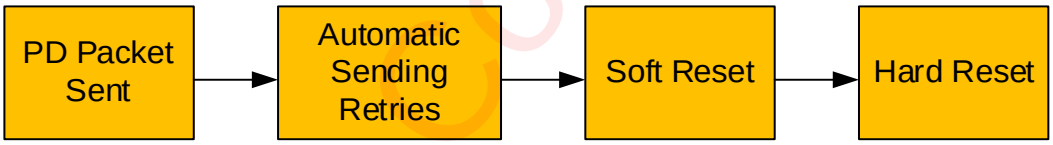


Figure 9 Order of PD automatically send retries

If the correct GoodCRC packet is still not received for all retries then I_RETRYFAIL interrupt is triggered and if bit[3](AUTO_SOFTRESET) in the CONTROL3 Register(0x09) is 1, then a Soft Reset packet is prepared. If Soft Reset is sent successfully where a GoodCRC control message is received with a Message ID of 0, then I_TXSENT interrupt occurs. Otherwise, this Soft Reset packet is retried NRETRIES(bit[2:1] in the CONTROL3 Register(0x09)) times if a GoodCRC acknowledge packet is not received within CRC Receive Timer expiring(1.1ms max). If all retries fail, then I_SOFTFAIL interrupt is triggered.

If all retries of the soft reset packet fail and bit[4](AUTO_HARDRESET) in the CONTROL3 Register(0x09) is 1, then a Hard Reset ordered set is sent by loading up the TxFIFO with RESET1,RESET1,RESET1,RESET2. Note only one Hard Reset is sent since the typical retry mechanism doesn't apply. The processor's policy engine firmware is responsible for retrying the Hard Reset if it doesn't receive GoodCRC.

FLUSH RX-FIFO WITH BIST TEST DATA

During PD compliance testing, BIST test packets are used to test physical layer of the PD interface. One BIST test data packet has 7 data objects(including CRC). The BIST data can arrive continuously from a tester, which could cause the AW35615 RxFIFO to overflow and the PD protocol layer to stop sending GoodCRC messages unless the FIFO is read or cleared quickly.

By setting bit[2](RX_FLUSH) to a '1' in the CONTROL3 Register(0x09), AW35615 enters into BIST_TMODE, all the data received next will be flushed from the RxFIFO automatically and the PD protocol layer will keep sending GoodCRC messages back. Besides, tester needs to send a Hard Reset to exit BIST_TMODE.

I²C INTERFACE

The AW35615 supports the I²C protocol. The frequency supported by the I²C is 400 kHz and 1 MHz. Particully, 1MHz is supported in fast mode plus condition. The pull-up resistor for the SDA and SCL can be selected from 1 to 10kΩ. Usually, 4.7 kΩ is recommended for 400 kHz I²C, 1 kΩ is recommended for 1 MHz I²C. The voltage from 1.8 to 3.3V is allowed for the I²C interface. Additionally, the I²C chip supports continuous read and write operations.

DEVICE ADDRESS

The I²C device address is 7-bit (A7~A1), followed by the bit R/W (A0). Set A0 to "0" for writing and "1" for reading. The device address is 0x22.

A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	1	0	R/W

I²C START/STOP

All transactions begin with a START and are terminated by a STOP sent by master to slave. A high-to-low transition on the SDA input/output while the SCL input is high defines a START condition. A low-to-high transition on the SDA input/output while the SCL input is high defines a STOP condition.

In particular, the bus stays busy when a repeated START (Sr) is generated instead of a STOP signal corresponding to the latest START (S). Sr and S are usually regarded as equivalent.

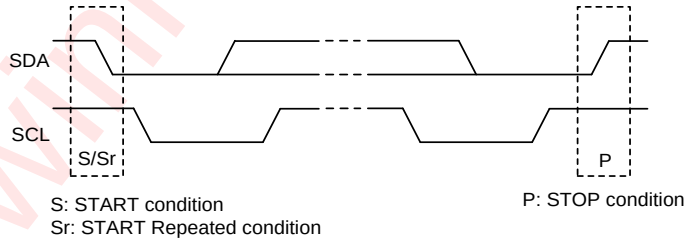


Figure 10 I²C START/STOP Condition Timing

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level. Each SCL pulse corresponds to one bit data transaction.

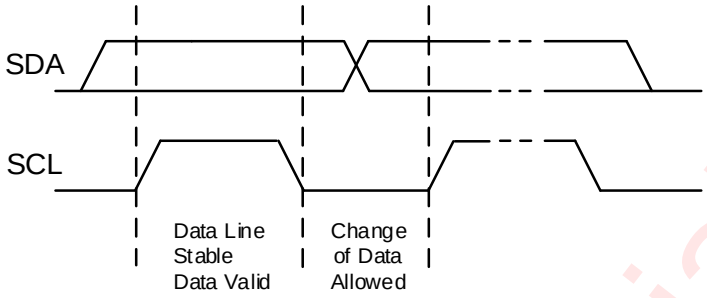


Figure 11 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transaction of I²C bus data. During writing cycle, after master sends 8-bit data, SDA must be released by master and SDA is pulled down to GND by slave chip when slave sends ACK.

During reading cycle, after slave chip sends 8-bit data, slave releases the SDA and waits for ACK from master. If master sends ACK, slave chip sends the next data. If master sends NACK, slave chip stops sending data and waits for I²C stop.

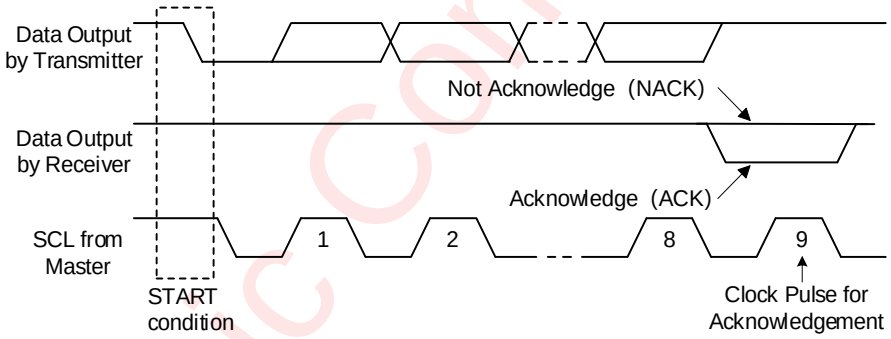


Figure 12 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line aborts the current transaction during the high state of the SCL. New data should be sent to SDA bus during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits and is transferred with the most significant bit first. After each byte, an ACK signal must follow.

In a write process, the following steps should be followed:

1. Master chip generates START condition. The "START" signal is generated by pulling down the SDA signal while the SCL signal is high.

2. Master chip sends slave address (7-bit) and the data direction bit R/W=0.
3. Slave chip sends acknowledge signal if the slave address is correct.
4. Master sends control register address (8-bit).
5. Slave sends acknowledge signal.
6. Master sends data byte to write to the addressed register.
7. Slave sends acknowledge signal.
8. If master send more data bytes, the control register address will be incremented by one after acknowledge signal (repeat step 6 and 7).
9. Master generates STOP condition to indicate write cycle ends.

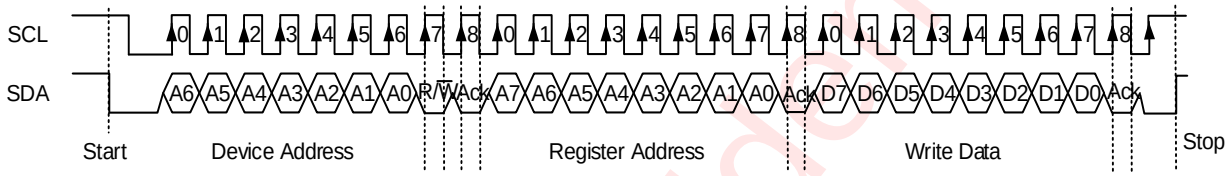


Figure 13 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

1. Master chip generates START condition
2. Master chip sends slave address (7-bit) and the data direction bit (R/W = 0).
3. Slave chip sends acknowledge signal if the slave address is correct.
4. Master sends control register address (8-bit)
5. Slave sends acknowledge signal
6. Master generates STOP condition followed with STOP-START condition or REPEAT START condition
7. Master chip sends slave address (7-bit) and the data direction bit (R/W = 1).
8. Slave chip sends acknowledge signal if the slave address is correct.
9. Slave sends data byte from addressed register.
10. If the master chip sends acknowledge signal, the slave chip will increase the control register address by one, then send the next data from the new addressed register.
11. If the master chip generates STOP condition, the read cycle ends.

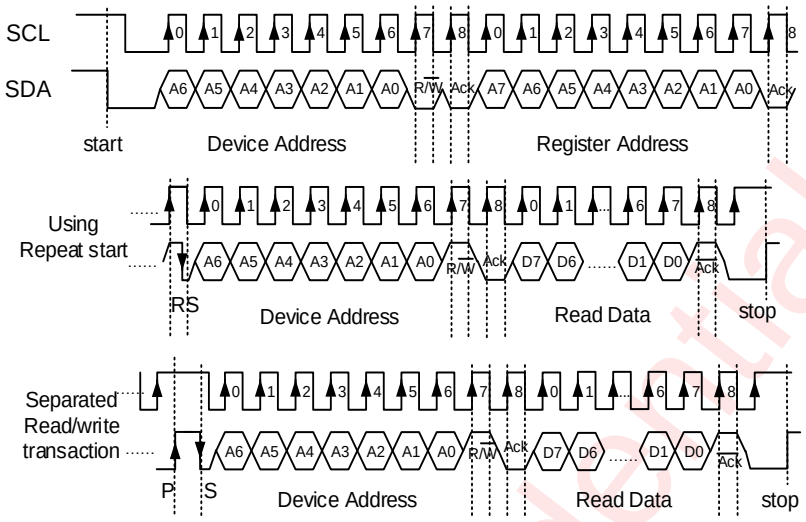


Figure 14 I²C Read Byte Cycle

I²C INTERFACE TIMING

PARAMETER		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	-	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	-	-	μs
$T_{SU:DAT}$	Data setup time	100	-	50	-	ns
T_R	Rising time of SDA and SCL	20	300	-	120	ns
T_F	Falling time of SDA and SCL	20*(VDD/5.5V)	300	20*(VDD/5.5V)	120	ns
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs

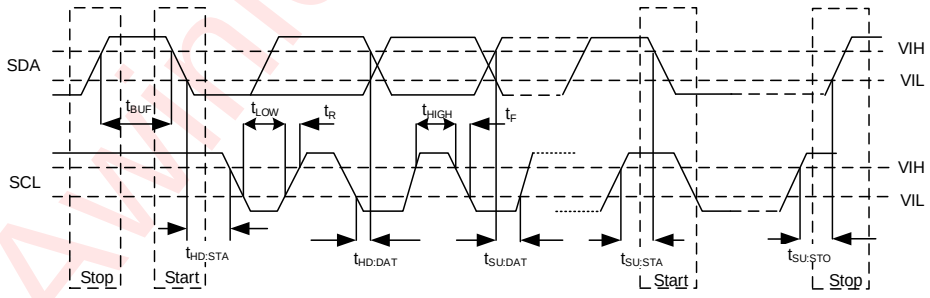


Figure 15 I2C Interface Timing

TRANSMIT DATA TOKENS

Transmit data tokens provide in-sequence transmit control and data for the transmit logic. Note that the token codes, and their equivalent USB PD K-Code are not the same. Tokens are read one at a time when they reach the end of the TxFIFO. For example, the specified token action is performed before the next token is read from the TxFIFO. The tokens are defined as follows:

Code	Name	Size (Bytes)	Description
111x_xxxx（0xA1）	TXON	1	Alternative method for starting the transmitter with the TX−START bit. This is not a token written to the TxFIFO but a command much like TX_START but it is more convenient to write it while writing to the TxFIFO in one contiguous write operation. It is preferred that the TxFIFO is first written with data and then TXON or TX_START is executed. It is expected that A1h will be written for TXON not any other bits where x is non-zero such as B1h, BFh, etc
0x12	SOP1	1	When reaching the end of the FIFO causes a Sync−1 symbol to be transmitted
0x13	SOP2	1	When reaching the end of the FIFO causes a Sync−2 symbol to be transmitted
0x1B	SOP3	1	When reaching the end of the FIFO causes a Sync−3 symbol to be transmitted
0x15	RESET1	1	When reaching the end of the FIFO causes a RST−1 symbol to be transmitted
0x16	RESET2	1	When reaching the end of the FIFO causes a RST−2 symbol to be transmitted
0x80	PACKSYM	1+N	This data token must be immediately followed by a sequence of N packed data bytes. This token is defined by the 3 MSB's being set to 3'b100. The 5 LSB's are the number of packed bytes being sent Note: N cannot be less than 2 since the minimum control packet has a header that is 2 bytes and N cannot be greater than 30 since the maximum data packet has 30 bytes (2 byte header + 7 data objects each having 4 bytes) Packed data bytes have two 4 bit data fields. The 4 LSB's are sent first, after 4b5b conversion etc in the chip
0xFF	JAM_CRC	1	Causes the CRC, calculated by the hardware, to be inserted into the transmit stream when this token reaches the end of the TxFIFO
0x14	EOP	1	Causes an EOP symbol to be sent when this token reaches the end of the TxFIFO
0xFE	TXOFF	1	Turn off the transmit driver. Typically the next symbol after EOP

RECEIVE DATA TOKENS

Receive data tokens provide in-sequence receive control and data for the receive logic. The RxFIFO can absorb as many packets as the number of bytes in the RxFIFO (80 bytes). The tokens are defined as follows:

Code	Name	Size (Bytes)	Description
111x_xxxx	SOP	1	First byte of a received packet to indicate that the packet is an SOP packet (“x” is undefined and can be any bit)
110x_xxxx	SOP1	1	First byte of a received packet to indicate that the packet is an SOP’ packet and occurs only if bit[0](ENSOP1) in the CONTROL1 Register(0x07) is ‘1’ (“x” is undefined and can be any bit)
101x_xxxx	SOP2	1	First byte of a received packet to indicate that the packet is an SOP” packet and occurs only if bit[1](ENSOP2) in the CONTROL1 Register(0x07) is ‘1’ (“x” is undefined and can be any bit)
100x_xxxx	SOP1DB	1	First byte of a received packet to indicate that the packet is an SOP’_DEBUG packet and occurs only if bit[5](ENSOP1DB) in the CONTROL1 Register(0x07) is ‘1’ (“x” is undefined and can be any bit)
011x_xxxx	SOP2DB	1	First byte of a received packet to indicate that the packet is an SOP”_DEBUG packet and occurs only if bit[6](ENSOP2DB) in the CONTROL1 Register(0x07) is ‘1’ (“x” is undefined and can be any bit)
010x_xxxx/ 001x_xxxx/ 000x_xxxx	Do Not Use	1	These can be used in future versions of this device and should not be relied on to be any special value. (“x” is undefined and can be any bit)

REGISTER CONFIGURATION

Register List

Name	ADDR	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def
DEVICE_ID	01h	R	VERSION_ID				PRODUCT_ID		REVISION_ID		9xh
SWITCHES0	02h	R/W	PU_EN2	PU_EN1	VCONN_CC2	VCONN_CC1	MEAS_CC2	MEAS_CC1	PDWN2	PDWN1	03h
SWITCHES1	03h	R/W	POWERROLE	SPECREV		DATAROLE		AUTO_CRC	TX_CC2	TX_CC1	20h
MEASURE	04h	R/W		MEAS_VBUS	MDAC						31h
SLICE	05h	R/W	SDAC_HYS		SDAC						60h
CONTROL0	06h	R/W/C		TX_FLUSH	INT_MASK		HOST_CUR		AUTO_PRE	TX_START	24h
CONTROL1	07h	R/W/C		ENSOP2DB	ENSOP1DB	BIST_MODE2		RX_FLUSH	ENSOP2	ENSOP1	00h
CONTROL2	08h	R/W	TOG_SAVE_PWR		TOG_RD_ONLY		WAKE_EN	MODE		TOGGLE	02h
CONTROL3	09h	R/W		SEND HARD RESET	BIST_TMODE	AUTO HARDRESET	AUTO SOFTRESET	N_RETRIES		AUTO_RETRY	06h
MASK	0Ah	R/W	M_VBUSOK	M_ACTIVITY	M_COMP_CHNG	M_CRC_CHK	M_ALERT	M_WAKE	M_COLLISION	M_BC_LVL	00h
POWER	0Bh	R/W					PWR				01h
RESET	0Ch	W/C							PD_RESET	SW_RESET	00h
OCPREG	0Dh	R/W					OCP_RANGE	OCP_CUR			0Fh
MASKA	0Eh	R/W	M_OCP_TEMP	M_TOGDONE	M_SOFTFAIL	M_RETRYFAIL	M_HARDSENT	M_TXSENT	M_SOFTRST	M_HARDRST	00h
MASKB	0Fh	R/W						M_VCONN_OK	M_CC_OV	M_GCRCSENT	00h
CONTROL4	10h	R/W							EN_PAR_CFG	TOG_EXIT_AUD	00h
CONTROL5	11h	R/W				VBUS_DIS_SEL			CC_OV_TH	EN_PD3_MSG	00h
VDL	3Ah	R	LSB_VENDOR_ID								4Fh
VDH	3Bh	R	MSB_VENDOR_ID								34h
STATUS0A	3Ch	R	VCONN_OK	CC_OV	SOFTFAIL	RETRYFAIL	POWER3	POWER2	SOFTRST	HARDRST	00h
STATUS1A	3Dh	R		CABLERST	TOGSS3	TOGSS2	TOGSS1	RXSOP2DB	RXSOP1DB	RX_SOP	00h
INTERRUPTA	3Eh	R/C	I_OCP_TEMP	I_TOGDONE	I_SOFTFAIL	I_RETRYFAIL	I_HARDSENT	I_TXSENT	I_SOFTRST	I_HARDRST	00h
INTERRUPTB	3Fh	R/C						I_VCONN_OK	I_CC_OV	I_GCRCSENT	00h
STATUS0	40h	R	VBUSOK	ACTIVITY	COMP	CRC_CHK	ALERT	WAKE	BC_LVL		01h
STATUS1	41h	R	RXSOP2	RXSOP1	RX_EMPTY	RX_FULL	TX_EMPTY	TX_FULL	OVRTEMP	OCP	28h
INTERRUPT	42h	R/C	I_VBUSOK	I_ACTIVUTY	I_COMP_CHNG	I_CRC_CHK	I_ALERT	I_WAKE	I_COLLISION	I_BC_LVL	00h
FIFOS	43h	R/W	TX_RX_FIFO								00h

ATTENTIONS:

1. Do not use registers that are blank.
2. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers.
3. FIFOs register is serially read/written without auto address increment.

Register Detailed Description

DEVICE_ID (Address: 01h)

Bit	Name	R/W	Description	Default
7:4	VERSION_ID	R	Chip version ID: 1001	1001
3:2	PRODUCT_ID	R	Chip Product ID: 00	00
1:0	REVISION_ID	R	Chip Revision ID: 01	01

SWITCHES0 (Address: 02h)

Bit	Name	R/W	Description	Default
7	PU_EN2	R/W	Pull-up current to CC2 pin as SRC. 0: Disable 1: Enable	0
6	PU_EN1	R/W	Pull-up current to CC1 pin as SRC. 0: Disable 1: Enable	0
5	VCONN_CC2	R/W	Control the switch of VCONN current to CC2 pin. 0: Disable 1: Enable	0
4	VCONN_CC1	R/W	Control the switch of VCONN current to CC1 pin. 0: Disable 1: Enable	0
3	MEAS_CC2	R/W	Control the switch of measure block to monitor or to measure the voltage on CC2. 0: Disable 1: Enable	0
2	MEAS_CC1	R/W	Control the switch of measure block to monitor or to measure the voltage on CC1. 0: Disable 1: Enable	0
1	PDWN2	R/W	Pull-down on CC2 as SNK. 0: Disable 1: Enable	1
0	PDWN1	R/W	Pull-down on CC1 as SNK. 0: Disable 1: Enable	1

SWITCHES1 (Address: 03h)

Bit	Name	R/W	Description	Default
7	POWERROLE	R/W	For constructing the GoodCRC acknowledge message. It corresponds to the Port Power Role bit in the message header if an SOP packet is received: 0: SNK if SOP 1: SRC if SOP	0
6:5	SPECREV	R/W	For constructing the GoodCRC acknowledge packet. It corresponds to the Specification Revision bits in the message header: 00: Revision 1.0 01: Revision 2.0 10: Revision 3.0 11: Do Not Use	01
4	DATAROLE	R/W	For constructing the GoodCRC acknowledge packet. It corresponds to the Port Data Role bit in the message header. 0: UFP if SOP 1: DFP if SOP	0
3	RESERVED	N/A	RESERVED	0
2	AUTO_CRC	R/W	Control the transmitter to send a GoodCRC packet automatically when a message with a GoodCRC is received. 0: Disable 1: Enable	0
1	TX_CC2	R/W	Control the switch of BMC PHY to transmit packets on CC2 pin. 0: Disable 1: Enable	0
0	TX_CC1	R/W	Control the switch of BMC PHY to transmit packets on CC1 pin. 0: Disable 1: Enable	0

MEASURE (Address: 04h)

Bit	Name	R/W	Description	Default
7	RESERVED	N/A	RESERVED	0

Bit	Name	R/W	Description	Default
6	MEAS_VBUS	R/W	Select the input of MDAC/comparator block to measure VBUS voltage or to measure CC voltage. 0: MDAC/comparator block measures CC voltage, and MEAS_CC1/CC2 bits control MDAC/comparator block. 1: Measure VBUS with the MDAC/comparator block and MEAS_CC1/CC2 bits need to be 0.	0
5:0	MDAC	R/W	Measure Block DAC data input. LSB is equivalent to 42mV of voltage which is compared to the measured CC voltage. The measured CC is selected by MEAS_CC2, or MEAS_CC1 bits. **MDAC[5:0] MEAS_VBUS=0 MEAS_VBUS=1 Unit** 00_0000 0.042 0.420 V 00_0001 0.084 0.840 V 11_0000 2.058 20.58 V 11_0011 2.184 21.84 V 11_1110 2.646 26.46 V 11_1111 > 2.688 26.88 V	11 0001

SLICE（Address: 05h）

Bit	Name	R/W	Description	Default
7:6	SDAC_HYS	R/W	There are now two SDAC thresholds. The lower threshold is always the value programmed by SDAC[5:0] and the higher threshold that is: 00: No hysteresis, higher threshold = SDAC 01: 85 mV hysteresis, higher threshold = SDAC + 5h 10: 170 mV hysteresis, higher threshold = SDAC + Ah 11: 255 mV hysteresis, higher threshold= SDAC + 20h	01
5:0	SDAC	R/W	BMC Slicer DAC data input. Allows for a programmable threshold to meet the BMC receive mask under all noise conditions.	10 0000

CONTROL0 (Address: 06h)

Bit	Name	R/W	Description	Default
7	RESERVED	N/A	RESERVED	0
6	TX_FLUSH	W/C	Self-clearing bit to clear TxFIFO. 0: Don't clear TxFIFO 1: Clear TxFIFO	0

Bit	Name	R/W	Description	Default
5	INT_MASK	R/W	The mask of all interrupts 0: Don't mask any interrupt 1: Mask all interrupts	1
4	RESERVED	N/A	RESERVED	0
3:2	HOST_CUR	R/W	Control the host pull-up current enabled by PU_EN[2:1]: 00: No current 01: 80 μA – Default USB power 10: 180 μA – Medium Current Mode: 1.5 A 11: 330 μA – High Current Mode: 3 A	01
1	AUTO_PRE	R/W	Control PD logic to transmit preamble automatically after a message with a GoodCRC is received. It allows the host software to take 300 μs to respond after I_CRC_CHK interrupt occurs. Internal timer waits for approximately 170 μs before starting the transmitter and transmitting preamble. 0: Feature disabled 1: Feature enabled	0
0	TX_START	W/C	Start to transmit the data of TxFIFO. Preamble is started first and the transmit data can be written to the TxFIFO during the preamble period. Self-clearing bit. 0: None 1: Start to transmit the data of TxFIFO	0

CONTROL1 (Address: 07h)

Bit	Name	R/W	Description	Default
7	RESERVED	N/A	RESERVED	0
6	ENSOP2DB	R/W	Enable SOP"_DEBUG type packets. Allows PD logic to receive and respond SOP"_DEBUG packets. 0: Ignore SOP"_DEBUG (SOP double prime debug) packets 1: Enable SOP"_DEBUG (SOP double prime debug) packets	0
5	ENSOP1DB	R/W	Enable SOP'_DEBUG type packets. Allows PD logic to receive and respond SOP'_DEBUG packets. 0: Ignore SOP'_DEBUG (SOP prime debug) packets 1: Enable SOP'_DEBUG (SOP prime debug) packets	0
4	BIST_MODE2	R/W	Enter BIST MODE2 and send 01s code for testing. 0: Disable 1: Enable	0

Bit	Name	R/W	Description	Default
3	RESERVED	N/A	RESERVED	0
2	RX_FLUSH	W/C	Self-clearing bit to clear RxFIFO. 0: Don't clear RxFIFO 1: Clear RxFIFO	0
1	ENSOP2	R/W	Enable SOP" type packets. Allows PD logic to receive and respond SOP" packets. 0: Ignore SOP" (SOP double prime) packets 1: Enable SOP" (SOP double prime) packets	0
0	ENSOP1	R/W	Enable SOP' type packets. Allows PD logic to receive and respond SOP' packets. 0: Ignore SOP' (SOP prime) packets 1: Enable SOP' (SOP prime) packets	0

CONTROL2 (Address: 08h)

Bit	Name	R/W	Description	Default
7:6	TOG_SAVE_PWR	N/A	Set the DISABLE time between toggle cycles. 00: Disable 01: Wait for 40 ms between toggle cycles 10: Wait for 80 ms between toggle cycles 11: Wait for 160 ms between toggle cycles	00
5	TOG_RD_ONLY	R/W	Set Toggle Rd Only mode: 1: Only Rd values cause the TOGGLE state machine to stop toggling and trigger I_TOGDONE interrupt when TOGGLE = 1. 0: Rd and Ra values cause the TOGGLE state machine to stop toggling when TOGGLE = 1.	0
4	RESERVED	N/A	RESERVED	0
3	WAKE_EN	R/W	Control wake detection if the power state is correct. 0: Disable 1: Enable	0
2:1	MODE	R/W	Set DRP/SNK/SRC polling function in TOGGLE Mode. 00: Disable 01: Enable DRP polling function if TOGGLE=1 10: Enable SNK polling function if TOGGLE=1 11: Enable SRC polling function if TOGGLE=1	01
0	TOGGLE	R/W	Set DRP/SNK/SRC toggle and enables autonomous detecting function. 0: Disable 1: Enable	0

CONTROL3 (Address: 09h)

Bit	Name	R/W	Description	Default
7	RESERVED	N/A	RESERVED	0
6	SEND_ HARDRESET	W/C	Control PD logic to transmit a HARD RESET packet and the HARD RESET packet has highest priority. 0: Disable 1: Enable	0
5	BIST_TMODE	R/W	Enter BIST TMODE and RxFIFO is cleared immediately after sending GoodCRC response. 0: Disable BIST_TMODE 1: Enable BIST_TMODE	0
4	AUTO_ HARDRESET	R/W	Sending HARD RESET packet automatically if soft reset fail. 0: Disable 1: Enable	0
3	AUTO_ SOFTRESET	R/W	Sending SOFT RESET packet automatically if retries fail. 0: Disable 1: Enable	0
2:1	N_RETRIES	R/W	Set the number of packets retries： 00: No retries (Similar to disabling auto retry) 01: One retry of packet (two total packets sent) 10: Two retries of packet (three total packets sent) 11: Three retries of packet (four total packets sent)	11
0	AUTO_RETRY	R/W	Enable automatic packet retries if GoodCRC is not received in time. 0: Disable 1: Enable	0

MASK (Address: 0Ah)

Bit	Name	R/W	Description	Default
7	M_VBUSOK	R/W	Mask of the I_VBUSOK interrupt 0: Do not mask 1: Mask	0
6	M_ACTIVITY	R/W	Mask of the I_ACTIVITY interrupt 0: Do not mask 1: Mask	0
5	M_COMP_CHNG	R/W	Mask of the I_COMP_CHNG interrupt 0: Do not mask 1: Mask	0
4	M_CRC_CHK	R/W	Mask of the I_CRC_CHK interrupt 0: Do not mask 1: Mask	0

Bit	Name	R/W	Description	Default
3	M_ALERT	R/W	Mask of the I_ALERT interrupt 0: Do not mask 1: Mask	0
2	M_WAKE	R/W	Mask of the I_WAKE interrupt 0: Do not mask 1: Mask	0
1	M_COLLISION	R/W	Mask of the I_COLLISION interrupt 0: Do not mask 1: Mask	0
0	M_BC_LVL	R/W	Mask of the I_BC_LVL interrupt 0: Do not mask 1: Mask	0

POWER (Address: 0Bh)

Bit	Name	R/W	Description	Default
7:4	RESERVED	N/A	RESERVED	0000
3:0	PWR	R/W	Power enables of analog blocks: Bit0: Enable Bandgap and wake circuit power Bit1: Enable receiver and current references for measure Bit2: Enable Measure block power Bit3: Enable internal oscillator	0001

RESET (Address: 0Ch)

Bit	Name	R/W	Description	Default
7:2	RESERVED	N/A	RESERVED	00 0000
1	PD_RESET	W/C	Reset the PD functional blocks of transmitter and receiver. 0: Do not Reset 1: Reset	0
0	SW_RES	W/C	Reset all functional blocks of AW35615 including the I2C registers. 0: Do not Reset 1: Reset	0

OCPREG (Address: 0Dh)

Bit	Name	R/W	Description	Default
7:4	RESERVED	N/A	RESERVED	0000
3	OCP_RANGE	R/W	Set the range of over-current protection. 1: OCP range from 100 to 800 mA. 0: OCP range from 10 to 80 mA.	1
2:0	OCP_CUR	R/W	Set the threshold of over-current protection. 000: 1 × max_range / 8 001: 2 × max_range / 8 010: 3 × max_range / 8 011: 4 × max_range / 8 100: 5 × max_range / 8 101: 6 × max_range / 8 110: 7 × max_range / 8 111: max_range (See the definition of OCP_RANGE)	111

MASKA (Address: 0Eh)

Bit	Name	R/W	Description	Default
7	M_OCP_TEMP	R/W	Mask of the I_OCP_TEMP interrupt 0: Do not mask 1: Mask	0
6	M_TOGDONE	R/W	Mask of the I_TOGDONE interrupt 0: Do not mask 1: Mask	0
5	M_SOFTFAIL	R/W	Mask of the I_SOFTFAIL interrupt 0: Do not mask 1: Mask	0
4	M_RETRYFAIL	R/W	Mask of the I_RETRYFAIL interrupt 0: Do not mask 1: Mask	0
3	M_HARDSENT	R/W	Mask of the I_HARDSENT interrupt 0: Do not mask 1: Mask	0
2	M_TXSENT	R/W	Mask of the I_TXSENT interrupt 0: Do not mask 1: Mask	0
1	M_SOFTRST	R/W	Mask of the I_SOFTRST interrupt 0: Do not mask 1: Mask	0

Bit	Name	R/W	Description	Default
0	M_HARDRST	R/W	Mask of the I_HARDRST interrupt 0: Do not mask 1: Mask	0

MASKB (Address: 0Fh)

Bit	Name	R/W	Description	Default
7:3	RESERVED	N/A	RESERVED	0 0000
2	M_VCONN_OK	R/W	Mask of the I_VCONN_OK interrupt 0: Do not mask 1: Mask	0
1	M_CC_OV	R/W	Mask of the I_ CC_OV interrupt 0: Do not mask 1: Mask	0
0	M_ GCRCSENT	R/W	Mask of the I_ GCRCSENT interrupt 0: Do not mask 1: Mask	0

CONTROL4 (Address: 10h)

Bit	Name	R/W	Description	Default
7:2	RESERVED	N/A	RESERVED	00 0000
1	EN_PAR_CFG	R/W	Enable configuration of CONTROL5 register (11h). 0: Disable 1: Enable	0
0	TOG_EXIT_AUD	R/W	In Rd only Toggle mode, stop Toggle at Audio accessory (Detect Ra on both CC). 0: Disable 1: Enable	0

CONTROL5 (Address: 11h)

Bit	Name	R/W	Description	Default
7:5	RESERVED	N/A	RESERVED	000

Bit	Name	R/W	Description	Default
4:3	VBUS_DIS_SEL	R/W	VBUS discharge resistance selection. 00: Disable VBUS discharge resistance. 01: 660 Ω 10: 10 kΩ 11: Reserved	00
2	RESERVED	N/A	RESERVED	0
1	CC_OV_TH	R/W	Selecting the overvoltage threshold of CC1/CC2: 0: 5.9 V 1: 5.5 V	0
0	EN_PD3_MSG	R/W	USB PD protocol configuration: 0: Only Supports USB PD2.0 protocol. 1: Supports USB PD3.0 protocol.	0

VDL (Address: 3Ah)

Bit	Name	R/W	Description	Default
7:0	LSB_VENDOR_ID	R	Low byte of the unique vendor ID authorized by the USB IF: 0x344F	0x4F

VDH (Address: 3Bh)

Bit	Name	R/W	Description	Default
7:0	MSB_VENDOR_ID	R	High byte of the unique vendor ID authorized by the USB IF: 0x344F	0x34

STATUS0A (Address: 3Ch)

Bit	Name	R/W	Description	Default
7	VCONN_OK	R	Indicate that VCONN switch is opened and VCONN voltage transitions through 2.4V. 0: Not happened 1: Happened	0
6	CC_OV	R	Indicate that overvoltage has happened in CC1 or CC2. 0: Not happened 1: Happened	0

Bit	Name	R/W	Description	Default
5	SOFTFAIL	R	All soft reset packets with retries have failed to get a GoodCRC acknowledge. This status can be cleared when a TX_START, TXON or SEND_HARD_RESET is executed. 0: Not happened 1: Happened	0
4	RETRYFAIL	R	All packet retries have failed to get a GoodCRC acknowledge. This status is cleared when a START_TX, TXON or SEND_HARD_RESET is executed. 0: Not happened 1: Happened	0
3:2	POWER3: POWER2	R	Indicate internal power state when the power state is controlled by internal logic. POWER3 corresponds to PWR3 bit and POWER2 corresponds to PWR2 bit. The power state is the higher of both PWR[3:0] and {POWER3, POWER2, PWR[1:0]}. If one is 03 and the other is F, the internal power state is F.	00
1	SOFTRST	R	Indicate that one of the packets received was a soft reset packet. 0: Not happened 1: Happened	0
0	HARDRST	R	Indicate that Hard Reset PD ordered set has been received. 0: Not happened 1: Happened	0

STATUS1A (Address: 3Dh)

Bit	Name	R/W	Description	Default
7	RESERVED	N/A	RESERVED	0
6	CABLERST	R	Indicate CABLE RESET pockets have been received: 0: Has not received CABLE RESET pockets. 1: Has received CABLE RESET pockets.	0

Bit	Name	R/W	Description	Default
5:3	TOGSS	R	The toggle status indicates attach and orientation after toggle stopping. 000: Toggle logic running (Processor has previously written TOGGLE=1) 001: Toggle ends as SRC in CC1 (STOP_SRC1 state) 010: Toggle ends as SRC in CC2 (STOP_SRC2 state) 101: Toggle ends as SNK in CC1 (STOP_SNK1 state) 110: Toggle ends as SNK in CC2 (STOP_SNK2 state) 111: Toggle has detected Audio Accessory with Ra on both CC1 and CC2 (STOP_SRC1 state) Otherwise: Not defined (do not interpret)	000
2	RXSOP2DB	R	Indicates the type of last packet in the RxFIFO is SOP”_DEBUG.	0
1	RXSOP1DB	R	Indicates the type of last packet in the RxFIFO is SOP’_DEBUG.	0
0	RXSOP	R	Indicates the type of last packet in the RxFIFO is SOP.	0

INTERRUPTA (Address: 3Eh)

Bit	Name	R/W	Description	Default
7	I_OCP_TEMP	R/C	Interrupt indicates that over-current on one of VCONN switches or over-temperature. 0: Interrupt not triggered 1: Interrupt triggered	0
6	I_TOGDONE	R/C	Interrupt indicates that the TOGGLE function was terminated due to a device has been detected. 0: Interrupt not triggered 1: Interrupt triggered	0
5	I_SOFTFAIL	R/C	Interrupt indicates that automatic soft reset packets with retries have failed. 0: Interrupt not triggered 1: Interrupt triggered	0
4	I_RETRYFAIL	R/C	Interrupt indicates that automatic packet retries have failed. 0: Interrupt not triggered 1: Interrupt triggered	0
3	I_HARDSENT	R/C	Interrupt indicates sending a hard reset ordered set successfully. 0: Interrupt not triggered 1: Interrupt triggered	0

Bit	Name	R/W	Description	Default
2	I_TXSENT	R/C	Interrupt to alert that AW35615 sent a packet that was acknowledged with a GoodCRC packet. 0: Interrupt not triggered 1: Interrupt triggered	0
1	I_SOFTRST	R/C	Interrupt indicates that a soft reset packet has received. 0: Interrupt not triggered 1: Interrupt triggered	0
0	I_HARDRST	R/C	Interrupt indicates that a hard reset packet has received. 0: Interrupt not triggered 1: Interrupt triggered	0

INTERRUPTB (Address: 3Fh)

Bit	Name	R/W	Description	Default
7:3	RESERVED	N/A	RESERVED	0 0000
2	I_VCONN_OK	R/C	Interrupt occurs when VCONN transitions through 2.4V. 0: Interrupt not triggered 1: Interrupt triggered	0
1	I_CC_OV	R/C	Indicate an over-voltage has occurred on the CC1/CC2 0: Interrupt not triggered 1: Interrupt triggered	0
0	I_GCRCSENT	R/C	Sent a GoodCRC acknowledge packet in response to an incoming packet with correct CRC check. 0: Interrupt not triggered 1: Interrupt triggered	0

STATUS0 (Address: 40h)

Bit	Name	R/W	Description	Default
7	VBUSOK	R	Indicate that VBUS voltage transitions through the threshold. 0: Not happened 1: Happened	0
6	ACTIVITY	R	Transmissions are detected on the active CCx line. This bit goes high after a minimum of 3 CC transitions, and goes low with no transitions. 0: Not happened 1: Happened	0

Bit	Name	R/W	Description	Default
5	COMP	R	Indicate that measured CC1/CC2/VBUS input is higher than reference level driven from the MDAC. 0: Not happened 1: Happened	0
4	CRC_CHK	R	Indicate the last received packet had the correct CRC. 0: Not happened 1: Happened	0
3	ALERT	R	Indicate an error has occurred when TxFIFO is full or RxFIFO is full. 0: Not happened 1: Happened	0
2	WAKE	R	Voltage on CC indicates a device attempts to attach. 0: Not happened 1: Happened	0
1:0	BC_LVL	R	Indicate current voltage status of the measured CC pins and host current levels: 00: < 200 mV 01: > 200 mV, < 660 mV 10: > 660 mV, < 1.23 V 11: > 1.23 V Notes: the host software must measure these at an appropriate time, while there is no signaling activity on the selected CC line. BC_LVL is only defined when Measure block is on which is when register bits PWR[2]=1 and either MEAS_CC1=1 or MEAS_CC2=1.	01

STATUS1 (Address: 41h)

Bit	Name	R/W	Description	Default
7	RXSOP2	R	Indicate the type of last packet in the RxFIFO is SOP” 0: Not happened 1: Happened	0
6	RXSOP1	R	Indicate the type of last packet in the RxFIFO is SOP’. 0: Not happened 1: Happened	0
5	RX_EMPTY	R	Indicate the RxFIFO is empty 0: RxFIFO is not empty 1: RxFIFO is empty	1
4	RX_FULL	R	Indicate the RxFIFO is full 0: RxFIFO is not full 1: RxFIFO is full	0

Bit	Name	R/W	Description	Default
3	TX_EMPTY	R	Indicate the TxFIFO is empty 0: TxFIFO is not empty 1: TxFIFO is empty	1
2	TX_FULL	R	Indicate the TxFIFO is full 0: TxFIFO is not full 1: TxFIFO is full	0
1	OVRTEMP	R	Indicate that device temperature is too high. 0: Not happened 1: Happened	0
0	OCP	R	Indicate an over-current or short condition has occurred on the VCONN switch 0: Not happened 1: Happened	0

INTERRUPT (Address: 42h)

Bit	Name	R/W	Description	Default
7	I_VBUSOK	R/C	Interrupt indicates that VBUS voltage transitions through 4.5 V. 0: Interrupt not triggered 1: Interrupt triggered	0
6	I_ACTIVITY	R/C	Interrupt indicates that transmission is in progress on CC line and the CC is busy. 0: Interrupt not triggered 1: Interrupt triggered	0
5	I_COMP_CHNG	R/C	Interrupt indicates that the value of COMP has changed and the selected CC line has reached the threshold programmed into the MDAC. 0: Interrupt not triggered 1: Interrupt triggered	0
4	I_CRC_CHK	R/C	Interrupt indicates the last value of CRC_CHK is valid and the incoming packet has been CRC checked successfully. 0: Interrupt not triggered 1: Interrupt triggered	0
3	I_ALERT	R/C	Interrupt indicates an error caused by full TxFIFO or full RxFIFO. 0: Interrupt not triggered 1: Interrupt triggered	0

Bit	Name	R/W	Description	Default
2	I_WAKE	R/C	Voltage on CC indicated a device attempting to attach. The host software must power up the clock and receiver blocks. 0: Interrupt not triggered 1: Interrupt triggered	0
1	I_COLLISION	R/C	Interrupt Indicates the collision between receiving and transmitting packets. 0: Interrupt not triggered 1: Interrupt triggered	0
0	I_BC_LVL	R/C	Indicate the current level of CC lines has changed. 0: Interrupt not triggered 1: Interrupt triggered	0

FIFOS (Address: 43h)

Bit	Name	R/W	Description	Default
7:0	Tx / RxFIFO	R/W	Writing token to TxFIFO or reading messages from RxFIFO by accessing address 43h.	0x00

APPLICATION INFORMATION

VCONN POWER

The AW35615 supports the USB 3.1 full-featured cables and accessories. The AW35615 controls the VCONN connect to CCx, should power VCONN Port first.

SOFTWARE FLOW

The AW35615 detects ports connection, and provides interruption. It needs the cooperation of host software to implement Type-C detection. Those are the high level software flow diagram for a Type-C SNK, SRC and DRP detection.

SNK SOFTWARE FLOW

The software flow of the AW35615 as SNK detection is shown in Figure 16.

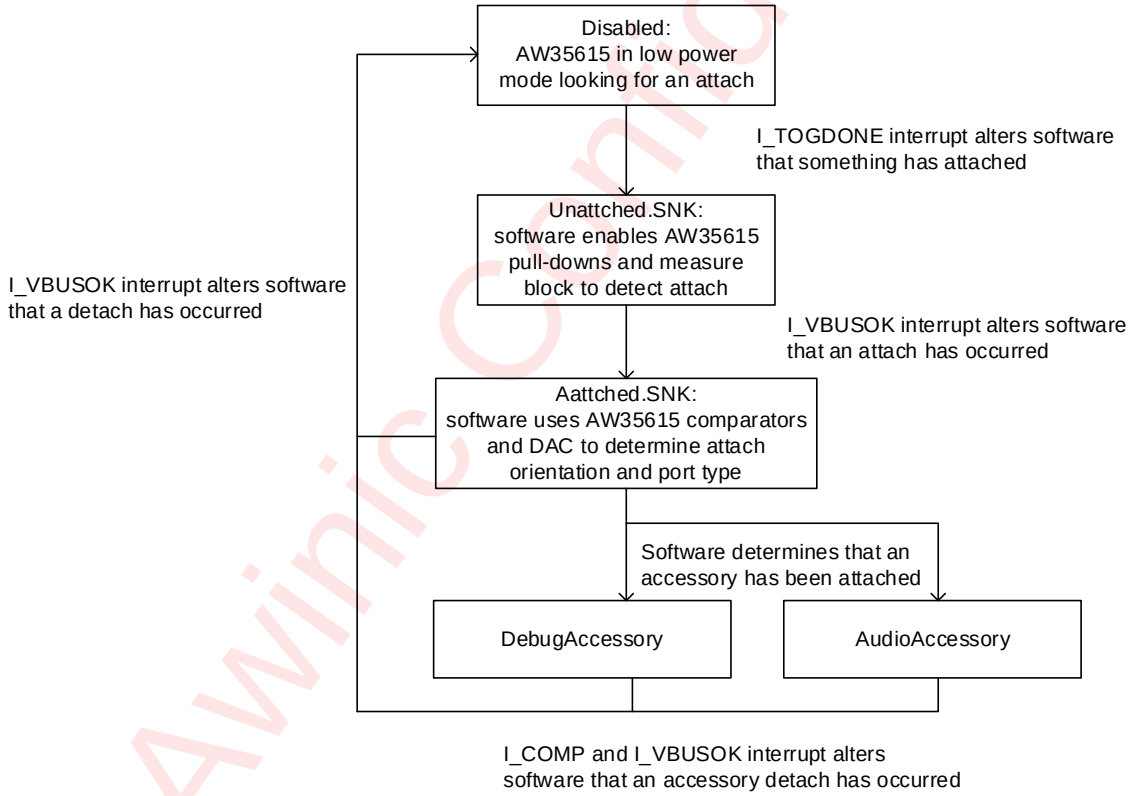


Figure 16 SNK Software Flow

SRC SOFTWARE FLOW

The software flow of the AW35615 as SRC detection is shown in Figure 17.

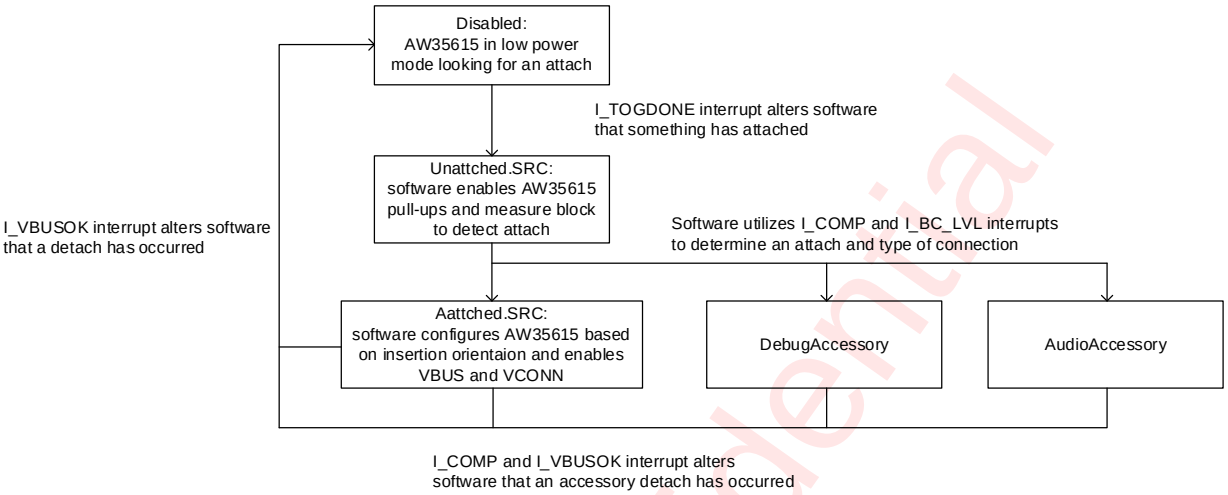


Figure 17 SRC Software Flow

DRP SOFTWARE FLOW

The software flow of the AW35615 as DRP detection is shown in Figure 18.

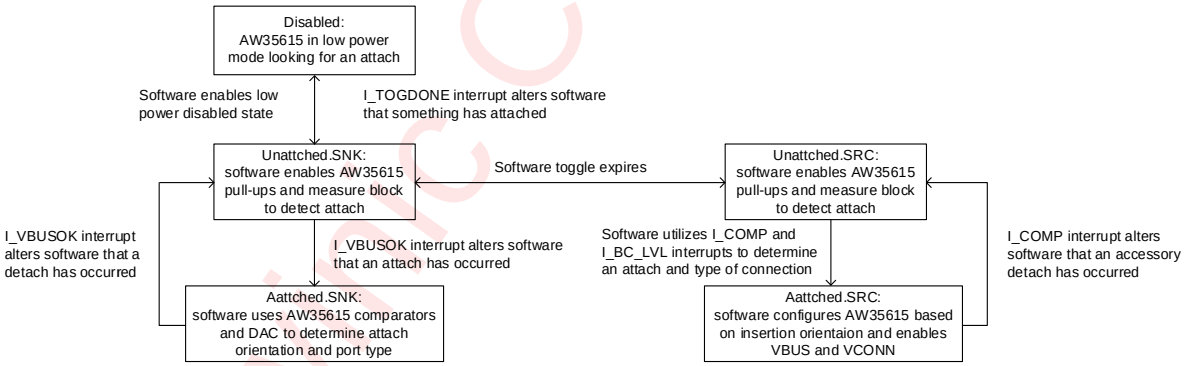


Figure 18 DRP Software Flow

RECOMMENDED COMPONENTS LIST

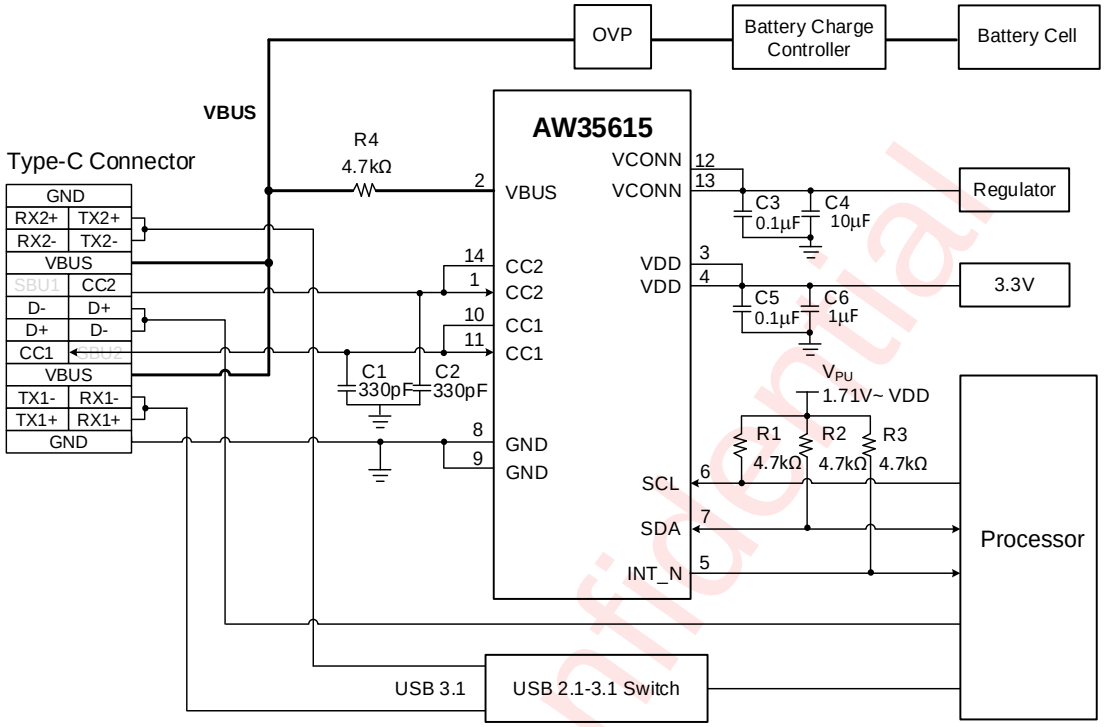


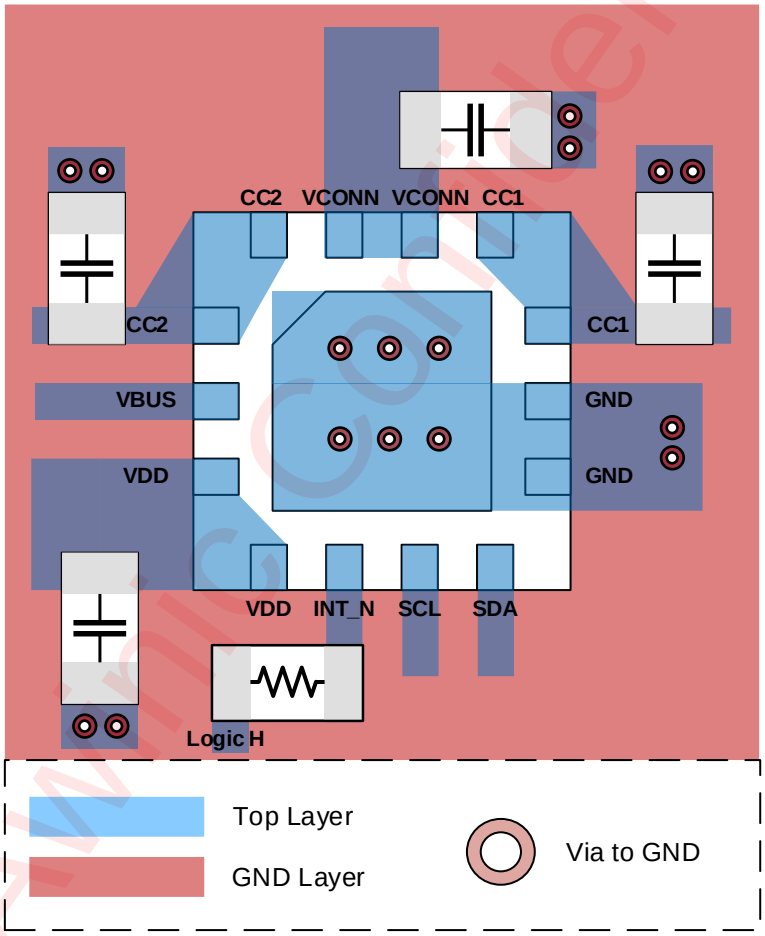
Figure 19 Recommended Application Circuit

RECOMMENDED COMPONENT VALUES FOR REFERENCE SCHEMATIC

Symbol	Parameter	Recommended Value			Unit
		Min	Typ	Max	
C1	CC1 receiver capacitance	200	–	600	pF
C2	CC2 receiver capacitance	200	–	600	pF
C3	VCONN decoupling capacitance	–	0.1	–	μF
C4	VCONN source bulk capacitance	10	–	220	μF
C5	VDD decoupling capacitance	–	0.1	–	μF
C6	VDD decoupling capacitance	–	1.0	–	μF
R1	I^2C SCL pull-up resistors	–	4.7	–	kΩ
R2	I^2C SDA pull-up resistors	–	4.7	–	kΩ
R3	INT_N pull-up resistor	1.0	4.7	–	kΩ
R4	Resistor for VBUS surge	-	4.7	-	kΩ
V_{PU}	I^2C pull-up voltage	1.71	–	VDD	V

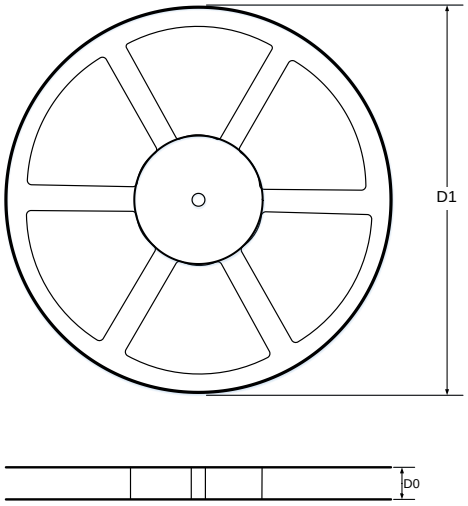
PCB LAYOUT CONSIDERATION

1. A 0.1 μF capacitor should be placed as close as possible to AW35615 VDD pin.
2. A 0.1 μF capacitor should be placed as close as possible to AW35615 VCONN pin.
3. A 200-600pF capacitor is recommended to be used on the CC line.
4. The INT_N pin requires an external $R_{pull-up}$ resistor.
5. According to PD Compliance Test Specification, during the power supply process, the voltage drop on GND from SRC PD Phy to SNK PD Phy should not exceed 250mV, which ensures the correct decoding of PD packets. Therefore, it is suggested in PCB design that the GND traces or planes between PD PHY and the Type-C connector should be as wide as possible for the lowest impedance. If not, the SDAC register can also be adjusted for compensation.

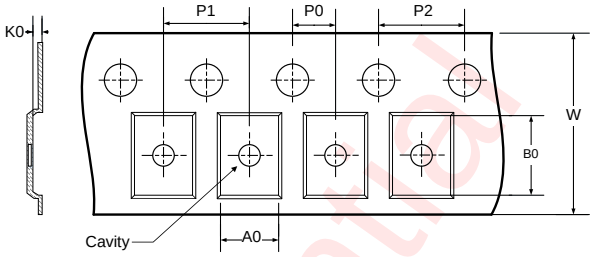


TAPE AND REEL INFORMATION

REEL DIMENSIONS

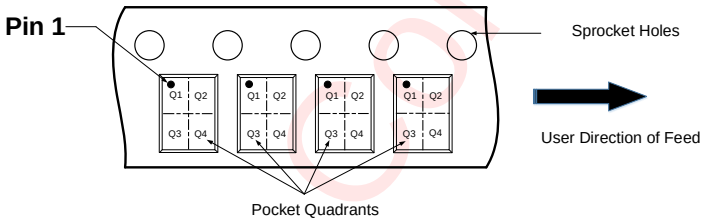


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



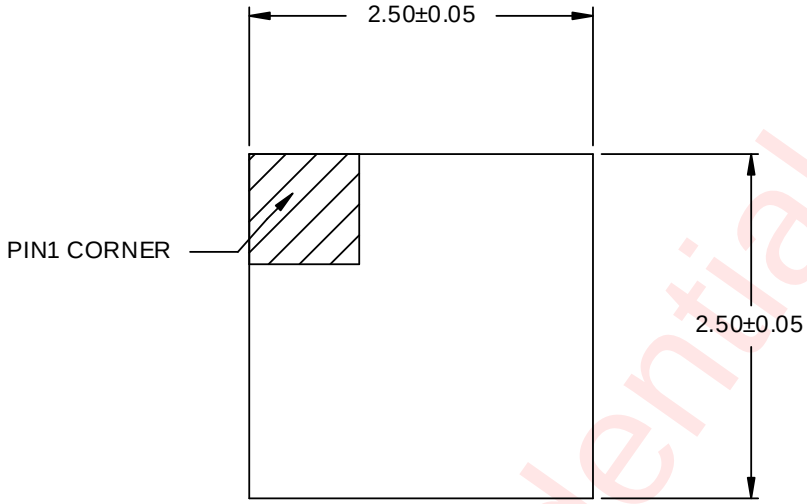
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

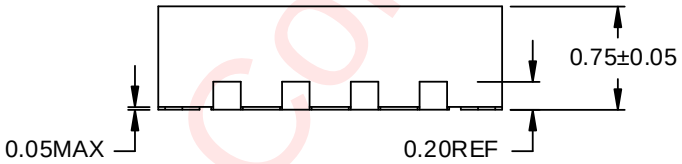
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.7	2.7	0.9	2	4	4	8	Q1

All dimensions are nominal

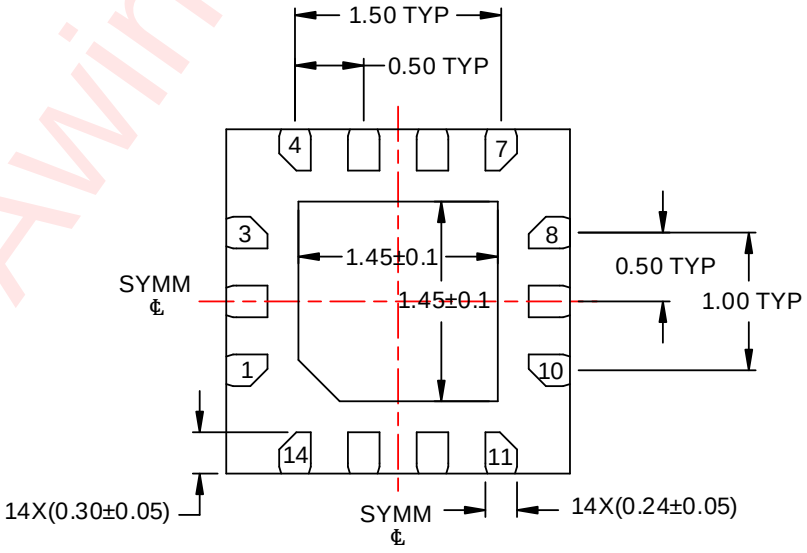
PACKAGE DESCRIPTION



Top View



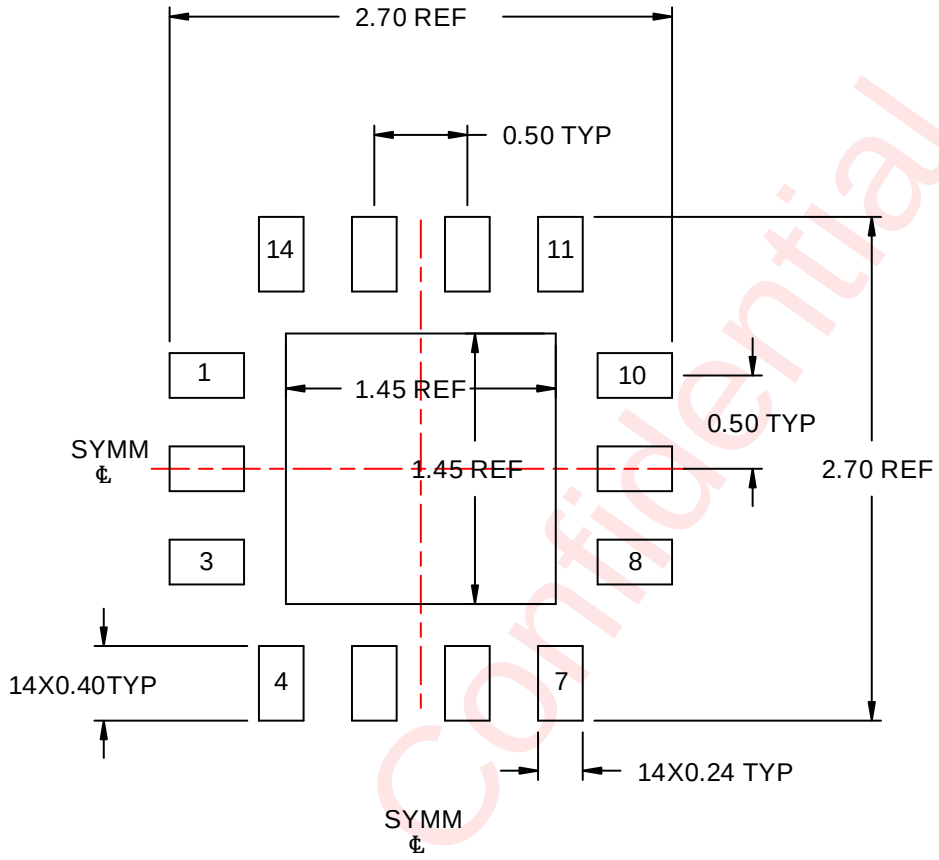
Side View

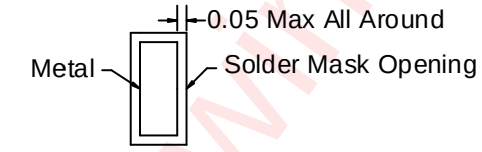


Bottom View

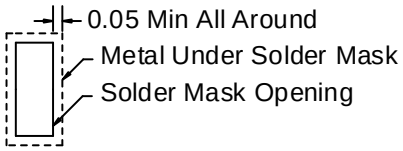
Unit:mm

LAND PATTERN DATA





Non-solder Mask Defined



Solder Mask Defined

Unit: mm

REVISION HISTORY

Version	Date	Change Record	
V1.0	Nov. 2021	Officially released	
V1.2	Nov. 2022	Modify the typical application circuit Modify the relationship between description and figure Add the notes for PCB layout consideration	- page 2 - page 43 - page 46
V1.3	May.2024	Improve the description of BIST MODE	- page 18

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